DATA SHEET

GPL10B

7KB LCD Controller/Driver

May 29, 2014

Version 1.5

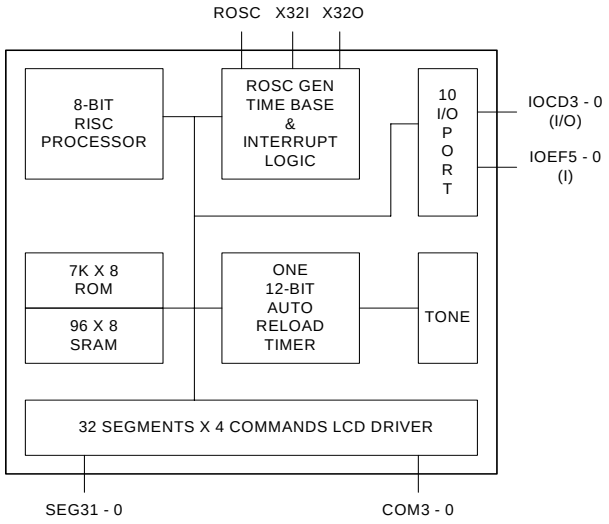
Table of Contents

7KB LCD CONTROLLER / DRIVER

1. GENERAL DESCRIPTION

The GPL10B is a CMOS 8-bit single chip micro-controller which contains LCD drivers, ROM, SRAM, I/O, timer/counter and tone output for directly driving buzzer on a single chip. The GPL10B is designed to drive LCD directly and performs efficient controller function as well as arithmetic function. With the on chip crystal oscillator, the real time clock can be easily implemented. For power saving, a software controllable standby switch is also built-in. The GPL10B is widely used in electronic products requiring very low power consumption, e.g. multi-function watch, calendar, calculator, and thermometer or LCD game with audio output.

2. BLOCK DIAGRAM



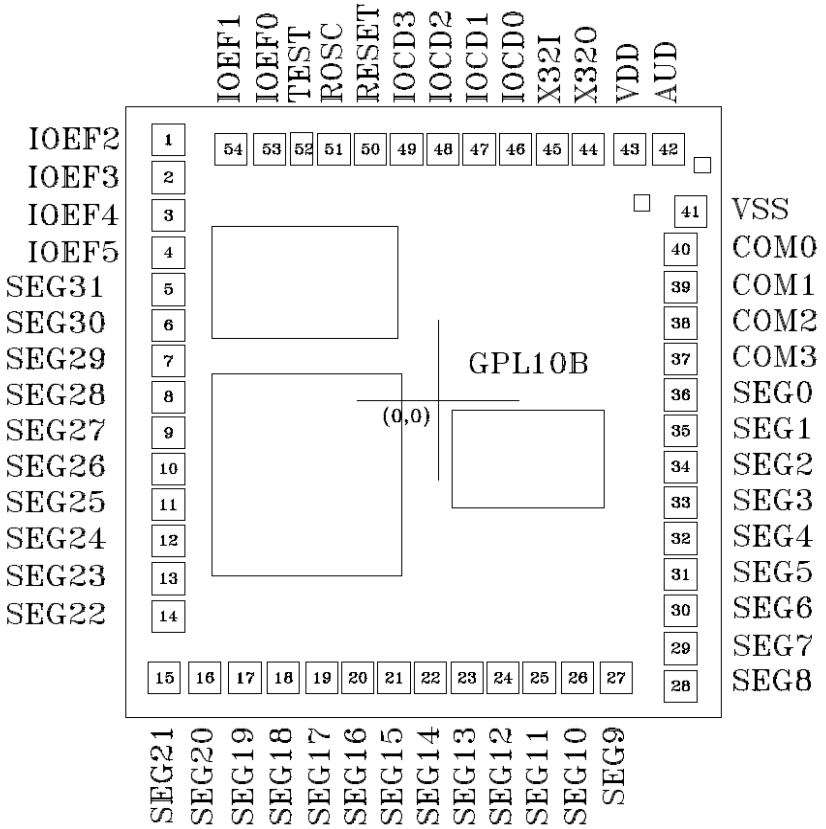
3. FEATURES

- Built-in 8-bit CPU
- Operating voltage: 2.0V to 5.5V
- Max. CPU clock: 2.0MHz @ 2.0V
- ROM capacity: 7K x 8 bits
- RAM capacity: 96 x 8 bits
- Direct Driver for LCD: 4 Commons x 32 Segments
  (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
- Input Port: Six input pins with key wakeup function with four different configurations (mask option)
- I/O Port: Four special purpose I/O for implement thermometer
- Timer/Counter: one 12-bit timer/counter
- Six Interrupt sources:
  . External Interrupt
  . Timer Interrupt
  . 2KHz Interrupt
  . LCD Service Interrupt (in LCD share mode)
  . 128Hz Interrupt
  . 2Hz Interrupt
- Dual Clock System: One built-in RC oscillator that selects internal or external resistor (mask option) for CPU. The other built-in crystal oscillator or RC oscillator (mask option) for LCD scanning.
- Tone Output: Tone output for directly driving buzzer
- System Reset: External Reset, Watchdog Reset and Low Voltage Reset (2.0V) are built-in
- Low Operating Current:
  Typical current < 8uA @ 3.0V for timepiece products

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG31 - 0	5 - 36	O	LCD driver segment output
COM3 - 0	37- 40	O	LCD driver common output
IOEF5 - 2 IOEF1 - 0	4 - 1 54 - 53	I	INPUT port (also for key wake-up input)
IOCD3 - 0	49 - 46	I/O	I/O port
ROSC	51	I	R-OSC input, connect to VDD through a resistor
RESET	50	I	External reset input
AUD	42	O	Tone output
X32I	45	I	32.768KHz crystal input/R oscillator input
X32O	44	O	32.768KHz crystal output
TEST	52	I	Test input
VDD	43	I	Power input
VSS	41	I	Ground input

4.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1uF capacitor between VDD and VSS should be placed to IC as close as possible.

5. FUNCTIONAL DESCRIPTIONS

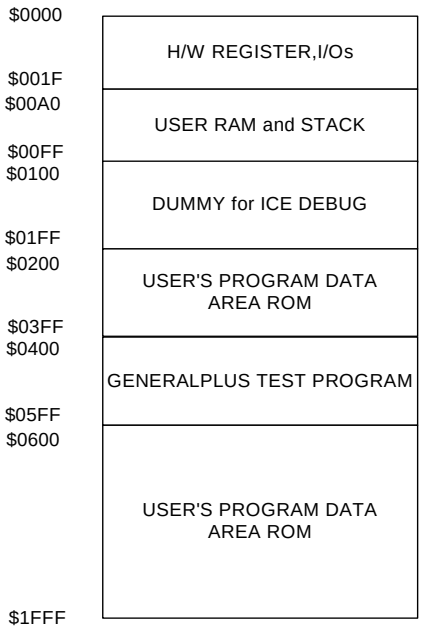
5.1. ROM

The GPL10B provides 7.5K bytes ROM size of which 7K bytes for program and data. The other 0.5K bytes are for GENERALPLUS internal test use, ranged from $0200 to $1FFF.

5.2. RAM

The GPL10B provides 96 bytes RAM. The RAM is for both stack and data storage, ranged from $00A0 to $00FF.

5.3. Memory and I/O Map

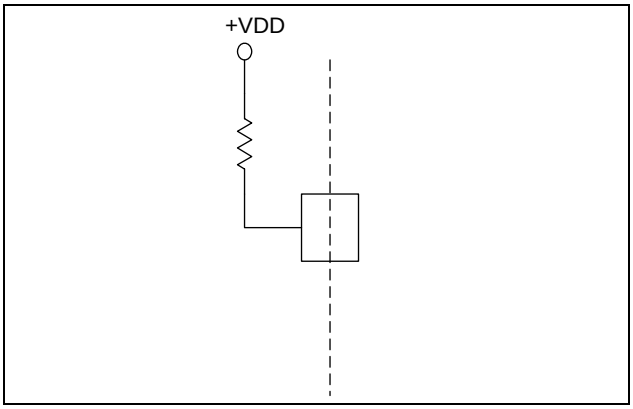


5.4. Oscillators

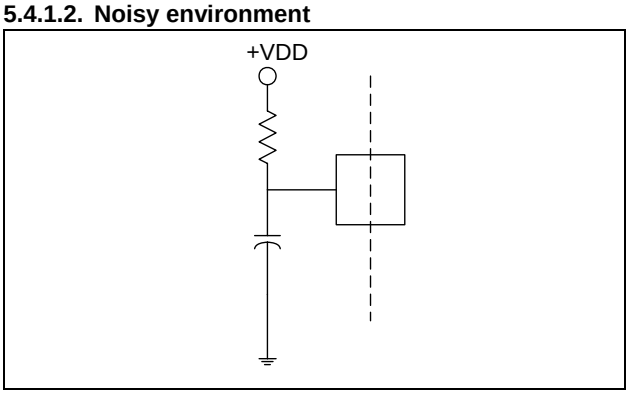
The GPL10B is a dual clock system. One clock is for the CPU and system and the other is for the LCD scanning and interrupt sources.

5.4.1. R Oscillator for the CPU and system clock

5.4.1.1. Normal case

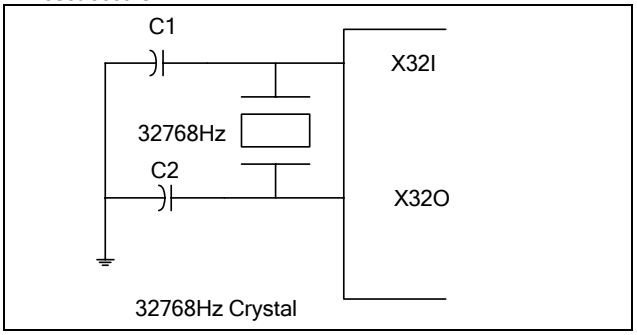


5.4.1.2. Noisy environment

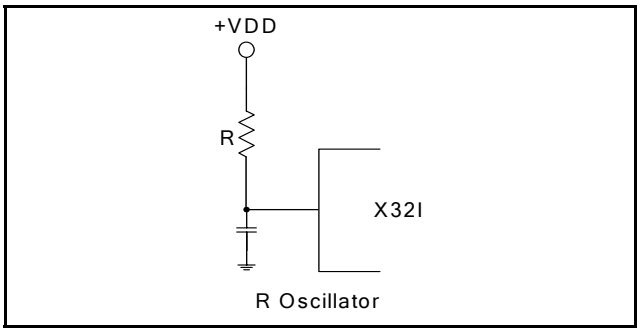


Note: Length of the wiring for ROSC pin should be minimized because the oscillator frequency varies due to coupling from other signal lines.

1). 32768Hz crystal oscillator or R oscillator (mask option) for LCD scanning and interrupt sources (2KHz, LCDL for LCD service, 128Hz, 2Hz). We suggest enabling 32768Hz crystal in strong mode for a few seconds and then switch to weak mode when reset occurs.



Note: Since each crystal has its own characteristics, Generalplus recommends users consult the crystal vendor for appropriate C1/C2 values.



Note: Length of the wiring for X32I and X32O should be as short as possible.

5.5. Stop Clock Mode

The GPL10B supports the power saving mode for those applications needing very low standby current. The user can simply enable the wake-up sources and then stop the CPU clock by writing the STOP CLOCK register ($09). The CPU will enter standby and the RAM and I/O remain their previous states until wake-up. There are three sources of wake-up in this chip, PORT IOEF wake-up, TIMER 0 wake-up and 2Hz wake-up. After the chip is wakening up, the internal CPU will go to the RESET state and the RAM and I/O are not affected by the wake-up reset. The standby current of timepiece product typically is less than 8uA @ 3.0V by using this mode and 32768Hz clock source in weak mode.

For non-timepiece products, 32768Hz crystal driver or R oscillator (mask option) generates the 32768Hz clock source that also can be turned off to stop the chip operation. The standby current of the GPL10B is less than 1uA @ 3.0V. In this mode, IOEF port can be used to wake up the chip.

5.6. Timer/Counter

The GPL10B contains one 12-bit timer/counter, TM0. In timer mode, TM0 is reloadable up-counter. When timer overflows from $0FFF to $0000, the carry signal will generate the INTERRUPT signal if the corresponding bit is enabled in INT ENABLE register ($0D), and the timer will be auto reloaded to the user's setup value and count up again. If TM0 is being specified as a counter, the user may reset the counter by loading 0 into register $14 and $1C. After the counter being activated, the count value can also be read from above registers on-the-fly, the read instruction will not affect the counter's value or reset it.

The clock source of the timer/counter are selectable as the following:

Timer/Counter		Addr.	Clock Source
TM0	12 BIT TIMER	$0014 $001C	CPU CLOCK (T) or T/4
	12 BIT COUNTER	$0014 $001C	T/128, T/256, T/2048 or EXT CLK
MODE SELECT REGISTER		$000B	Select TM0 timer or counter
TIMER CLOCK SELECTOR		$001C	Select T or T/4

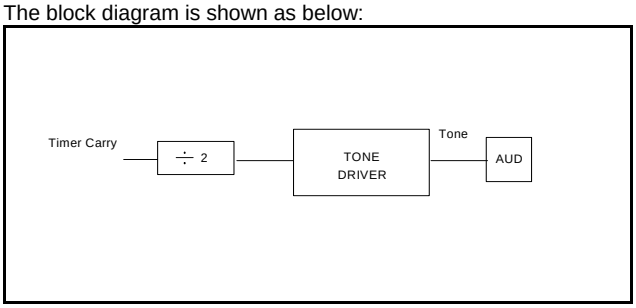
5.7. Interrupts

The GPL10B has six interrupt sources - INT0 (interrupt from TIMER 0), 2KHz INT, LCDL INT (LCD service in share mode, due to LCD registers is shared with the TIMER/COUNTER), 128Hz INT, EXT INT (external INTERRUPT from IOCD1), 2Hz INT. The 2KHz INT, LCDL INT (256 Hz in 1/3, 1/4 duty; 128 Hz in 1/2 duty), 128Hz INT, 2Hz INT, all are derived from 32768Hz Crystal Oscillator by division.

5.8. Tone Output

The GPL10B provides TONE output that can directly drive BUZZER. It is a full-swing (VDD and VSS) signal and its frequency source is the frequency of TIMER Carry divided by 2.

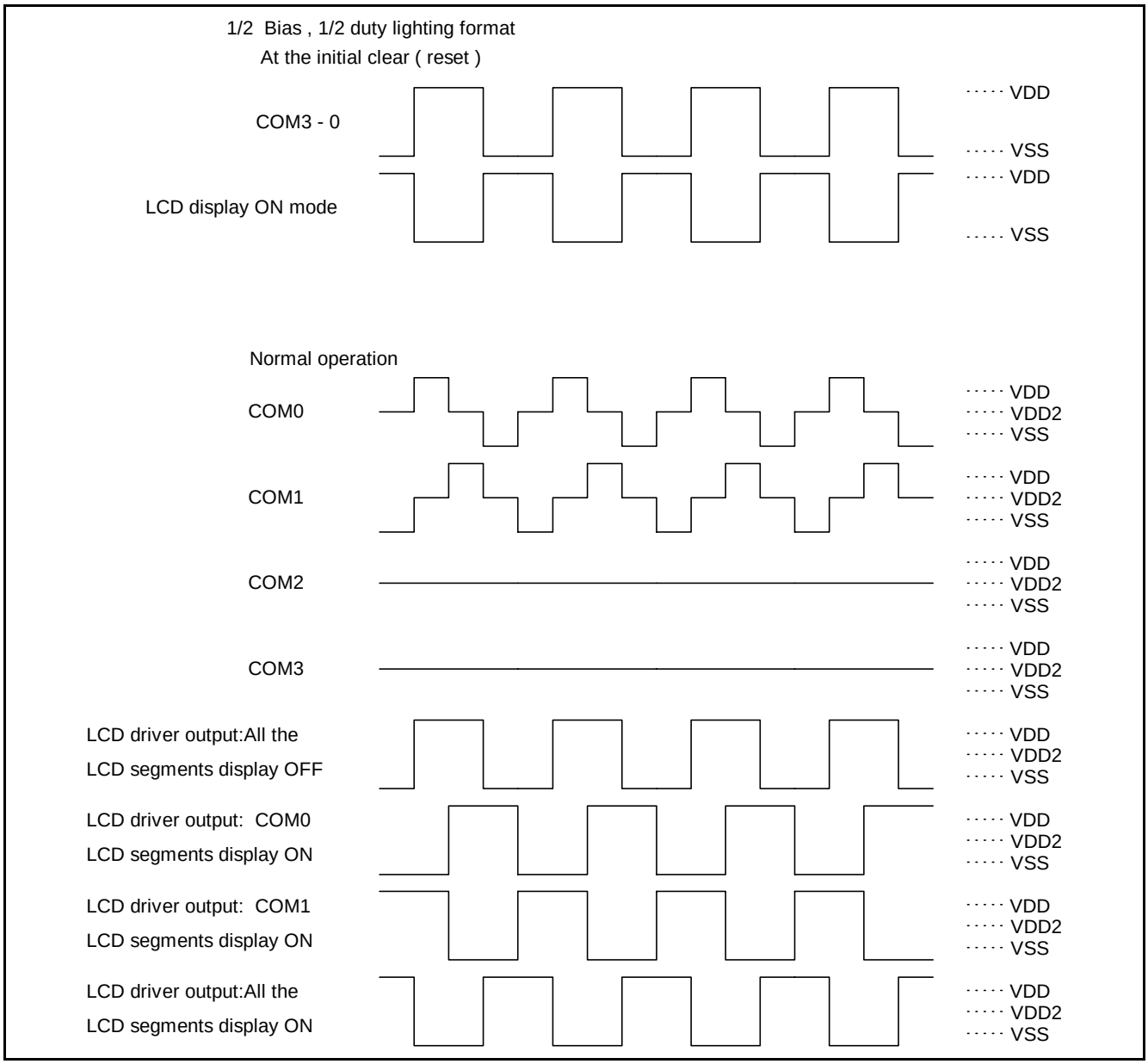
The block diagram is shown as below:

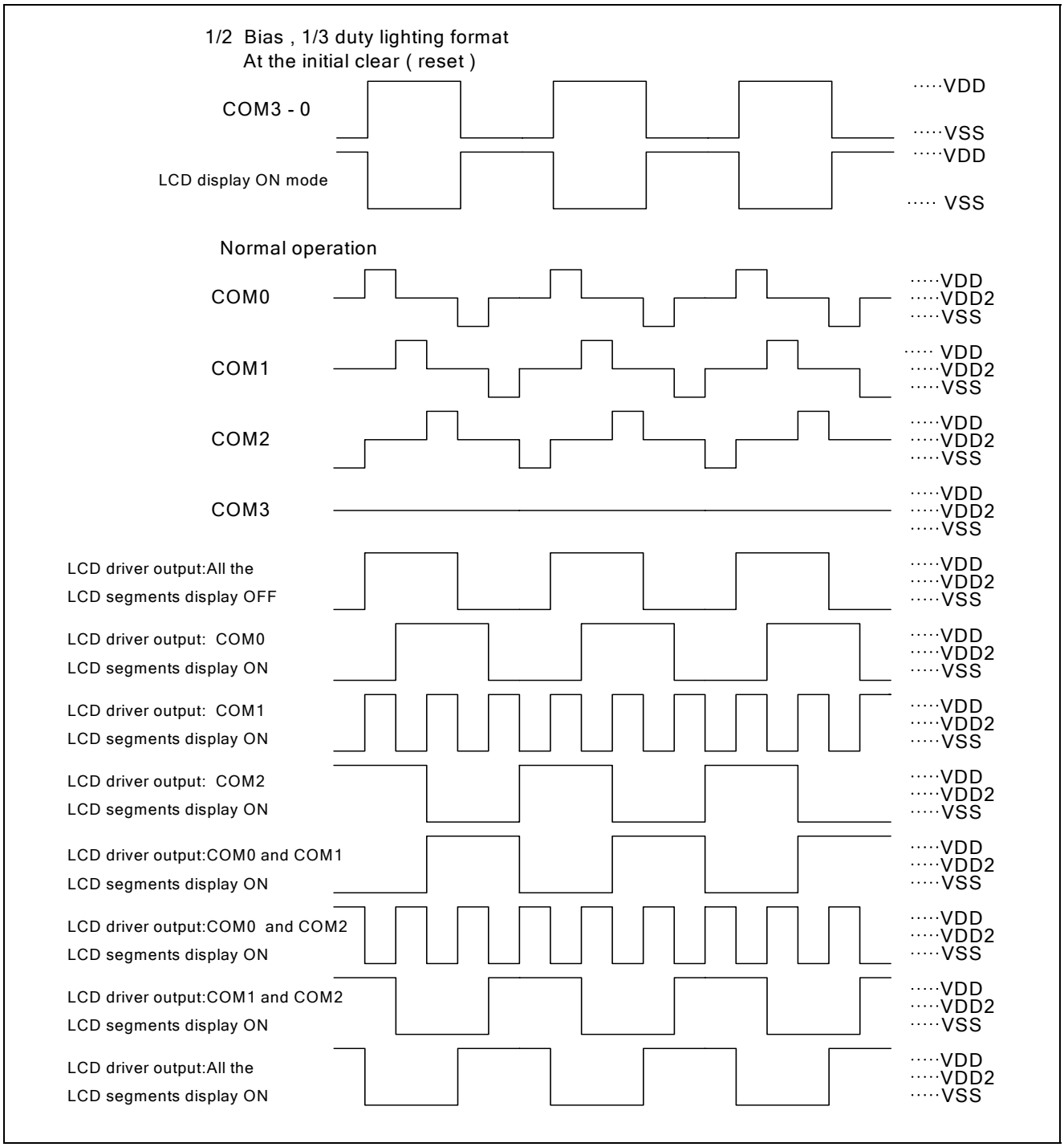


5.9. Liquid Crystal Display

The GPL10B can directly drive the liquid crystal display (LCD) panel of 1/2 duty, 1/3 duty, and 1/4 duty with 1/2 bias or 1/3 bias. It has 4 commons and 32 segments signal pins. In share mode (Timer/Counter is used), the LCD is refreshed by LCDL interrupt. The INT routine will read the number of common which is under serving, and send the next common's pattern to LCD port ($10 - $13) from RAM buffer. If the Timer/the counter is not used, hardware mechanism will auto refresh the LCD after writing OPTION register ($1F).

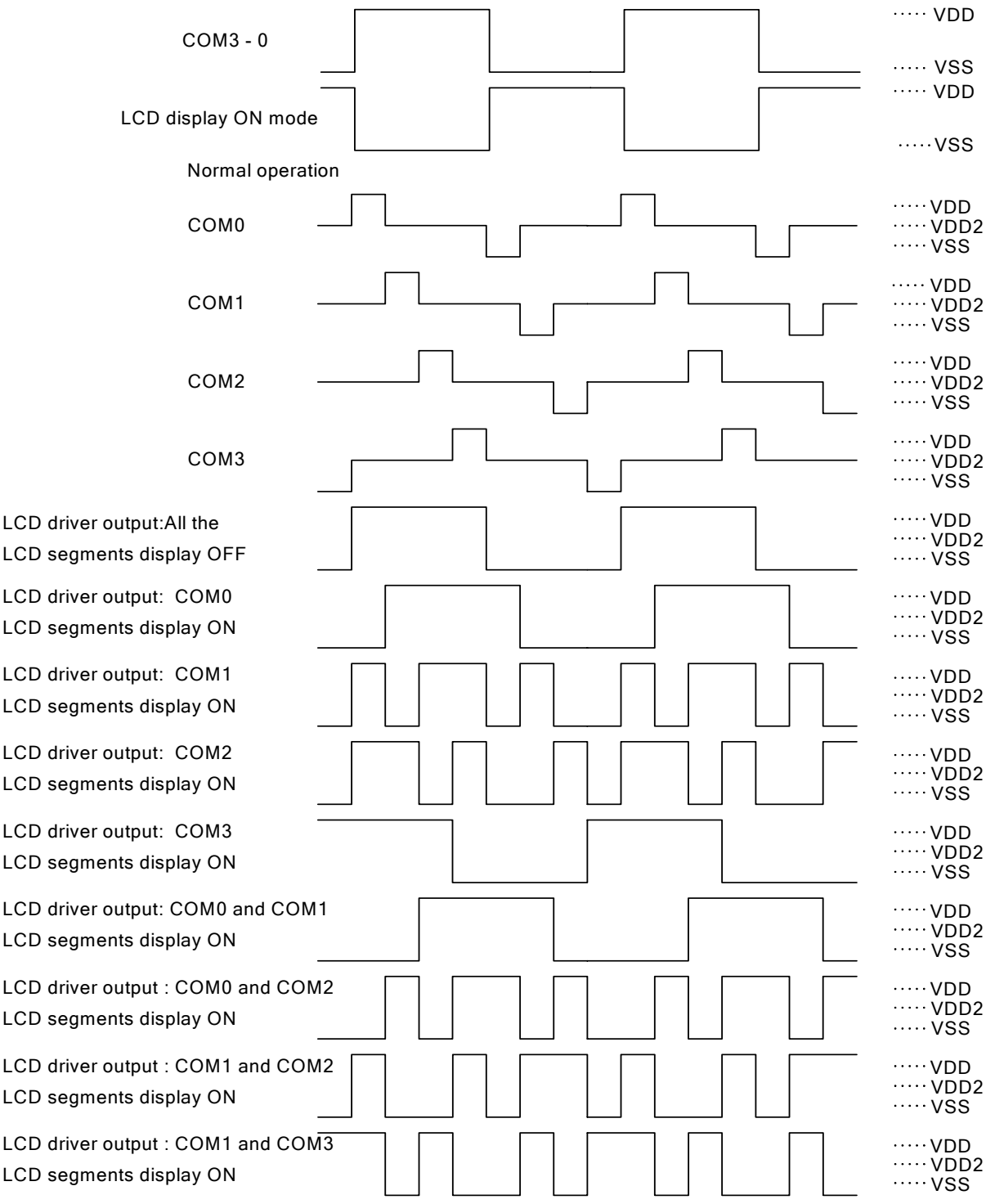
5.10. Output Waveform of the LCD Driver




1/2 Bias , 1/3 duty lighting format
At the initial clear (reset)
COM3 - 0
LCD display ON mode
·····VDD
·····VSS
·····VDD
····· VSS
Normal operation
COM0
COM1
COM2
COM3
·····VDD
·····VDD2
·····VSS
LCD driver output:All the
LCD segments display OFF
LCD driver output: COM0
LCD segments display ON
LCD driver output: COM1
LCD segments display ON
LCD driver output: COM2
LCD segments display ON
LCD driver output:COM0 and COM1
LCD segments display ON
LCD driver output:COM0 and COM2
LCD segments display ON
LCD driver output:COM1 and COM2
LCD segments display ON
LCD driver output:All the
LCD segments display ON

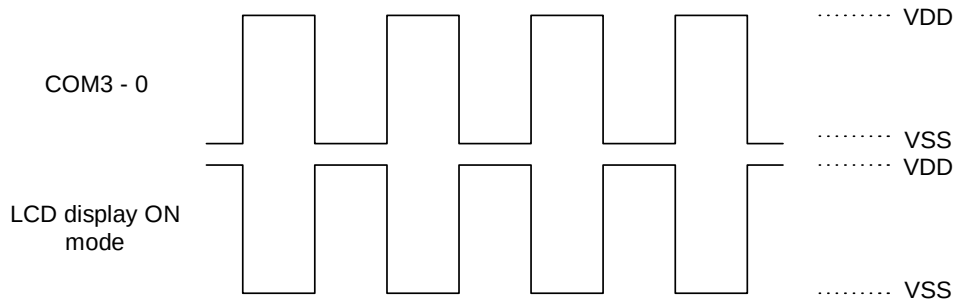
1/2 Bias , 1/4 duty lighting format

At the initial clear (reset)

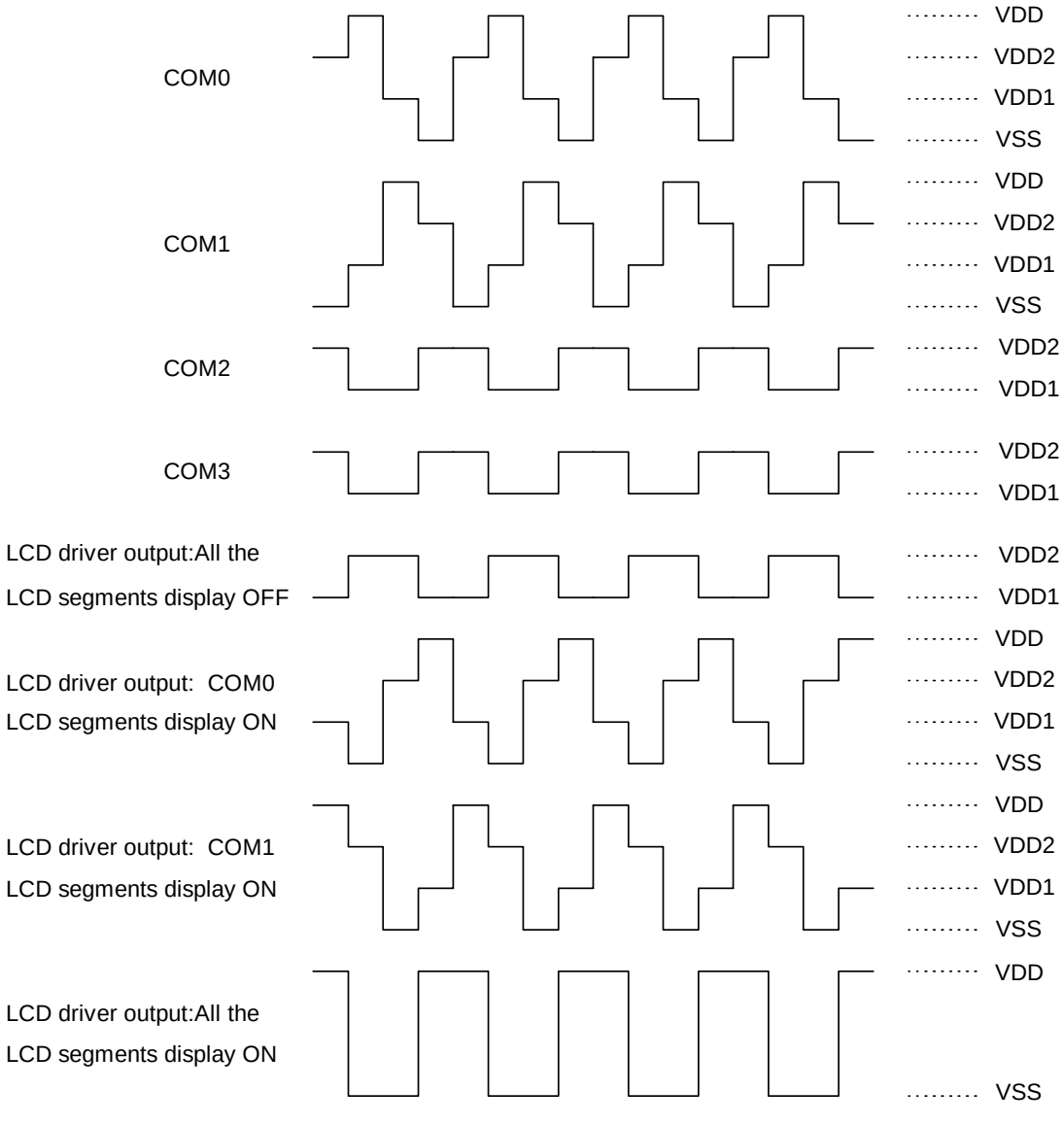


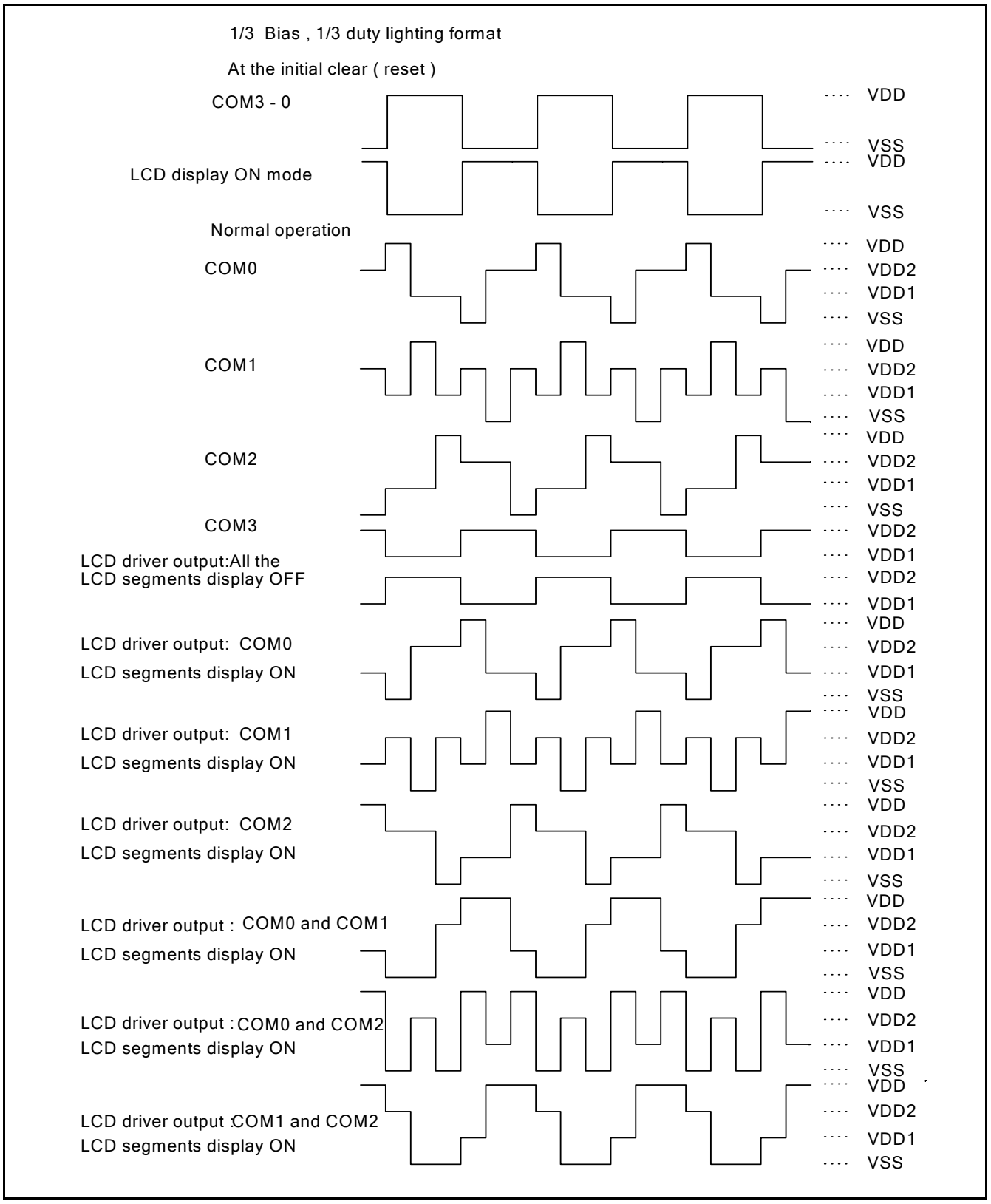
1/3 Bias , 1/2 duty lighting format

At the initial clear (reset)



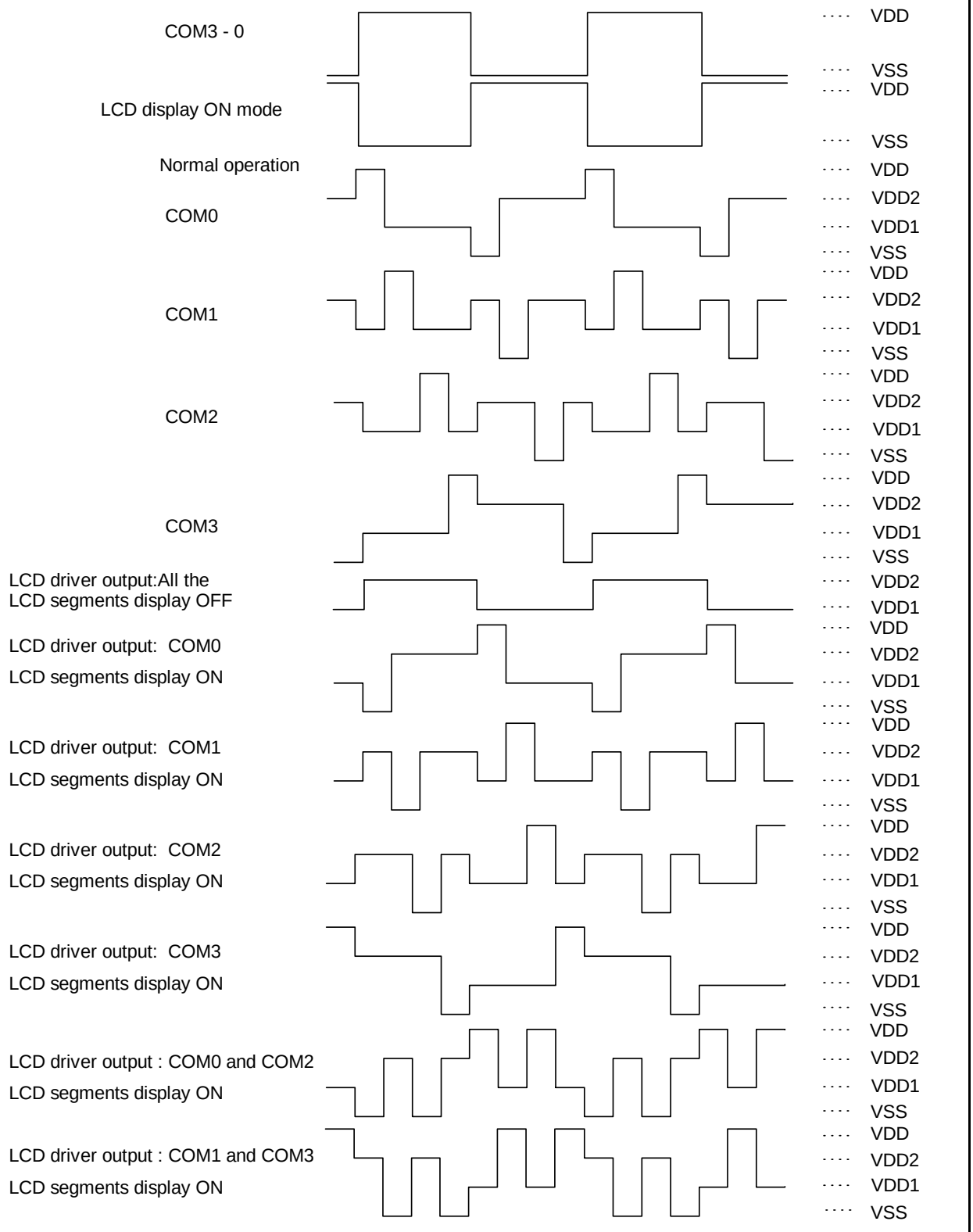
Normal operation




1/3 Bias , 1/3 duty lighting format
At the initial clear (reset)
COM3 - 0
LCD display ON mode
Normal operation
COM0
COM1
COM2
COM3
LCD driver output:All the LCD segments display OFF
LCD driver output: COM0 LCD segments display ON
LCD driver output: COM1 LCD segments display ON
LCD driver output: COM2 LCD segments display ON
LCD driver output : COM0 and COM1 LCD segments display ON
LCD driver output : COM0 and COM2 LCD segments display ON
LCD driver output : COM1 and COM2 LCD segments display ON
VDD
VSS
VDD2
VDD1

1/3 Bias , 1/4 duty lighting format

At the initial clear (reset)



5.11. Reset Function

The GPL10B can be reset by setting the RESET pin to ground voltage and its operation starts when this pin is set to power voltage. Also an automatic reset function (internal reset function) operates when power is turned on.

5.12. Watchdog Function

The GPL10B provides a watchdog timer. The watchdog timer must be reset when 2Hz wake-up by writing $0F; otherwise, it will reset the system.

5.13. Mask Option

The following type mask option is available.

4MHz R Oscillator clock Resistor: Select one of A, B

A) Internal resistor

B) external resistor

CPUCK frequency: Select one of A, B

A). 1MHz

B). 2MHz

IOEF0 to IOEF5: Select one of A, B, C, D (Refer to INPUT/OUTPUT)

A). Without Fixed Pull Low Resistor 200K-Ohm, with Feedback MOS

B). With Fixed Pull Low Resistor 200K-Ohm, without Feedback MOS

C). With Fixed Pull Low Resistor 200K,-Ohm with Feedback MOS

D). Without Fixed Pull Low Resistor 200K-Ohm, without Feedback MOS

32768Hz clock source: Select one of A, B (Refer to R oscillator)

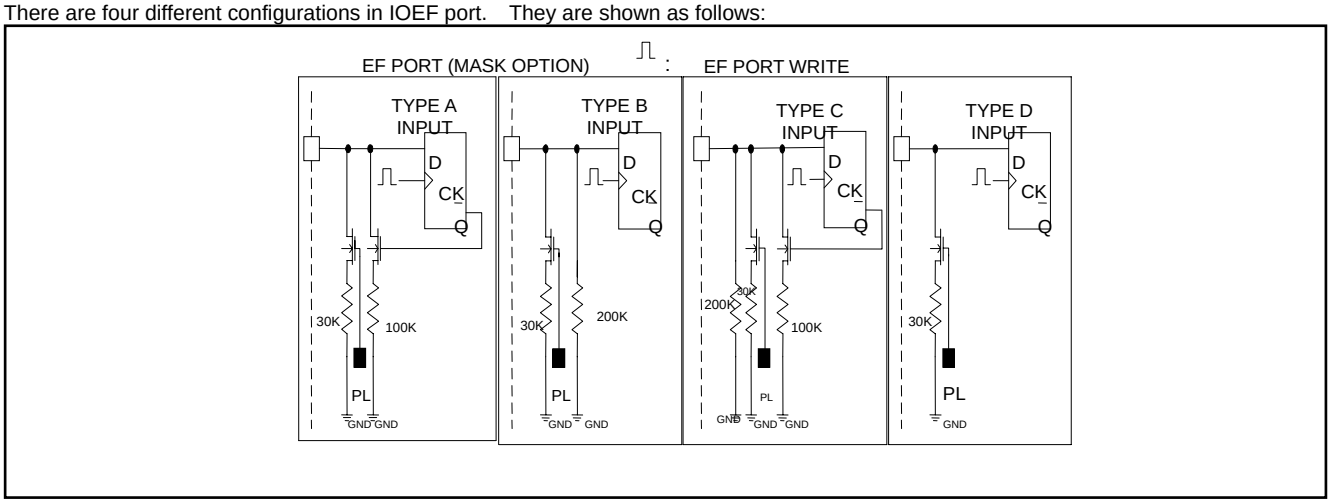
A). 32768Hz Crystal Oscillator

B). R Oscillator

6. I/O PORT CONFIGURATION

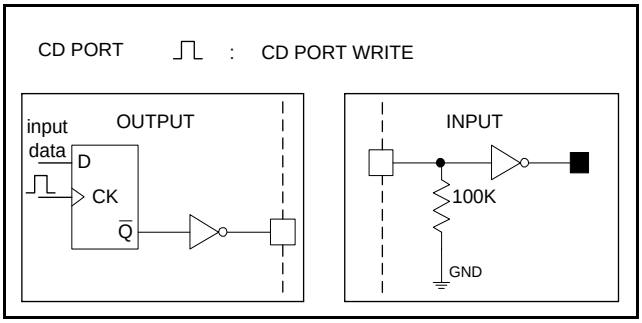
6.1. Input IOEF Port: IOEF0 to IOEF5

There are four different configurations in IOEF port. They are shown as follows:

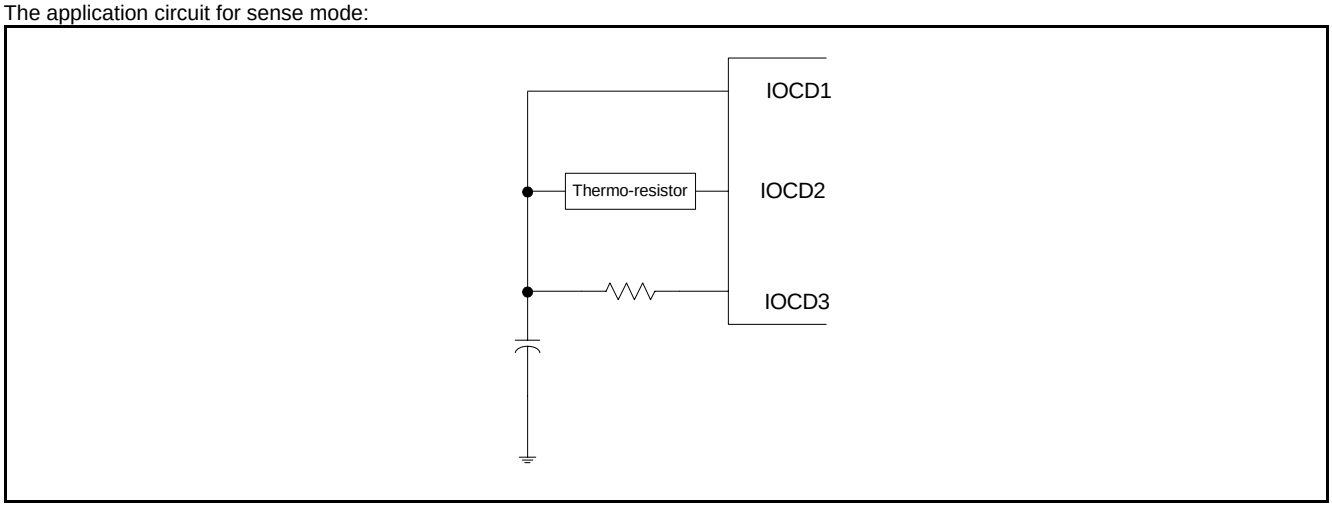


6.2. Input/Output IOCD Port: IOCD0 to IOCD3

These four IOCD ports can be programmed to be INPUT or OUTPUT pins independently. These pins also can be used to operate a thermometer by sense mode. Their configurations are shown as below:



The application circuit for sense mode:



7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	-20℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

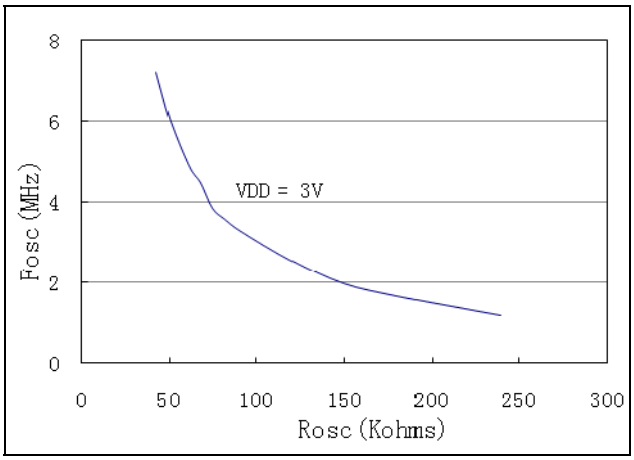
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.0	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	480	-	uA	F_{CPU} = 2MHz @ 3.0V, No load
Standby Current	I_{STBY}	-	-	1.0	uA	VDD = 3.0V, 32768Hz OFF
Audio Output Current	I_{AUD}	-	-7	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
IOCD output current	I_{OH}	-	-3	-	mA	VDD = 3.0V, V_{OH} = 2.4V
	I_{OL}	-	10	-	mA	VDD =3.0V, V_{OL} = 0.8V

7.3. DC Characteristics (VDD = 4.5V, T_A = 25℃)

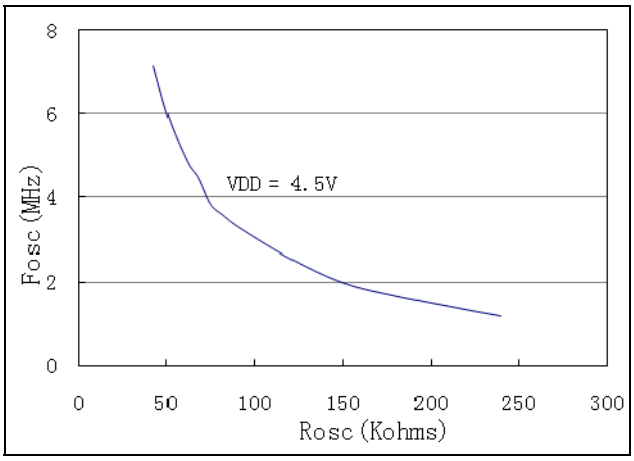
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	1.1	-	mA	F_{CPU} =2MHz @ 4.5V, no load
Standby Current	I_{STBY}	-	-	1.0	uA	VDD = 4.5V, 32768Hz OFF
Audio Output Current	I_{AUD}	-	-13	-	mA	VDD = 4.5V, V_{OH} = 3.6V
Input High Level	V_{IH}	3.0	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 4.5V
IOCD output current	I_{OH}	-	-6	-	mA	VDD = 4.5V, V_{OH} = 3.6V
	I_{OL}	-	15	-	mA	VDD = 4.5V, V_{OL} = 0.9V

7.4. The Relationships between the R_{OSC} and the F_{OSC}

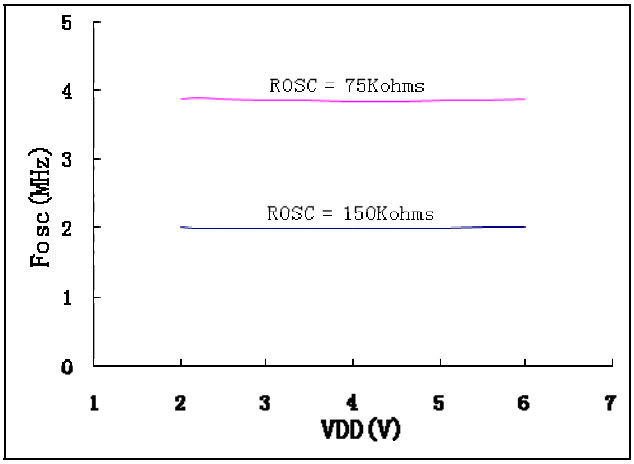
7.4.1. VDD = 3.0V, T_A = 25 ℃



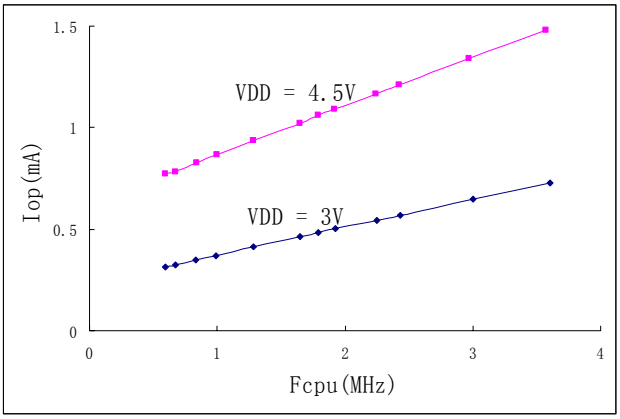
7.4.2. VDD = 4.5V, T_A = 25 ℃



7.5. The Relationships between the F_{OSC} and the VDD

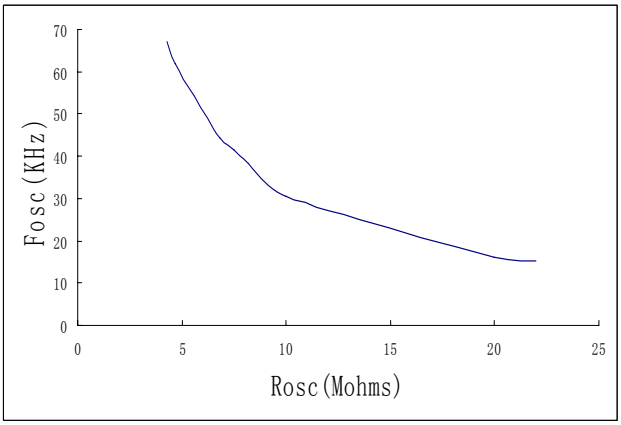


7.6. The Relationships between the F_{CPU} and the I_{OP}

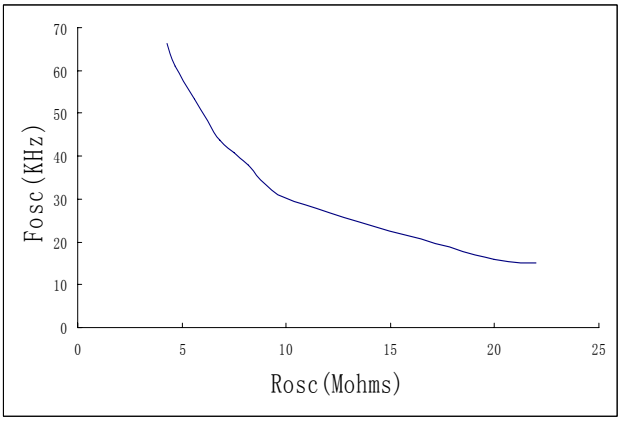


7.7. The Relationships between the R_{OSC32K} and the F_{32K}

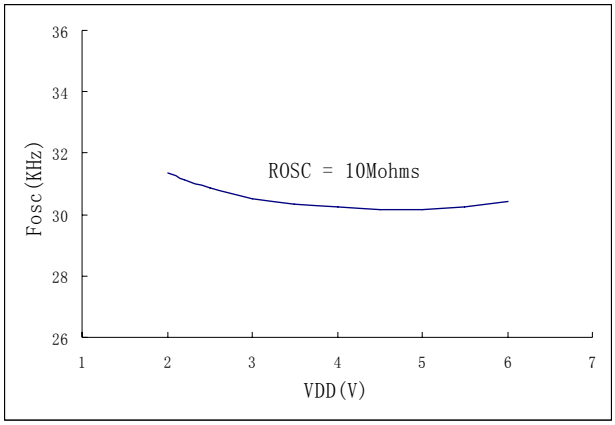
7.7.1. VDD = 3.0V, T_A = 25 ℃



7.7.2. VDD = 4.5V, T_A = 25 ℃



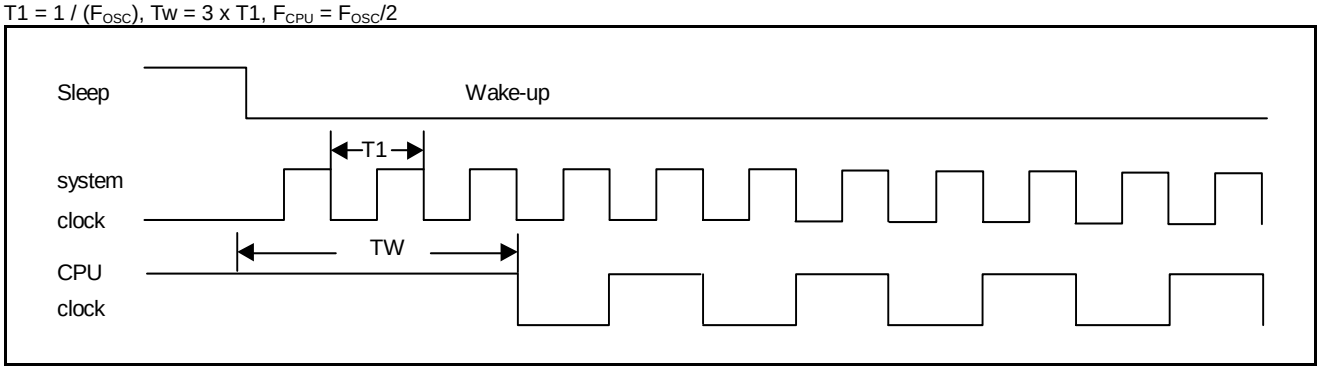
7.8. The Relationships between the F_{32K} and the VDD



7.9. AC Characteristics

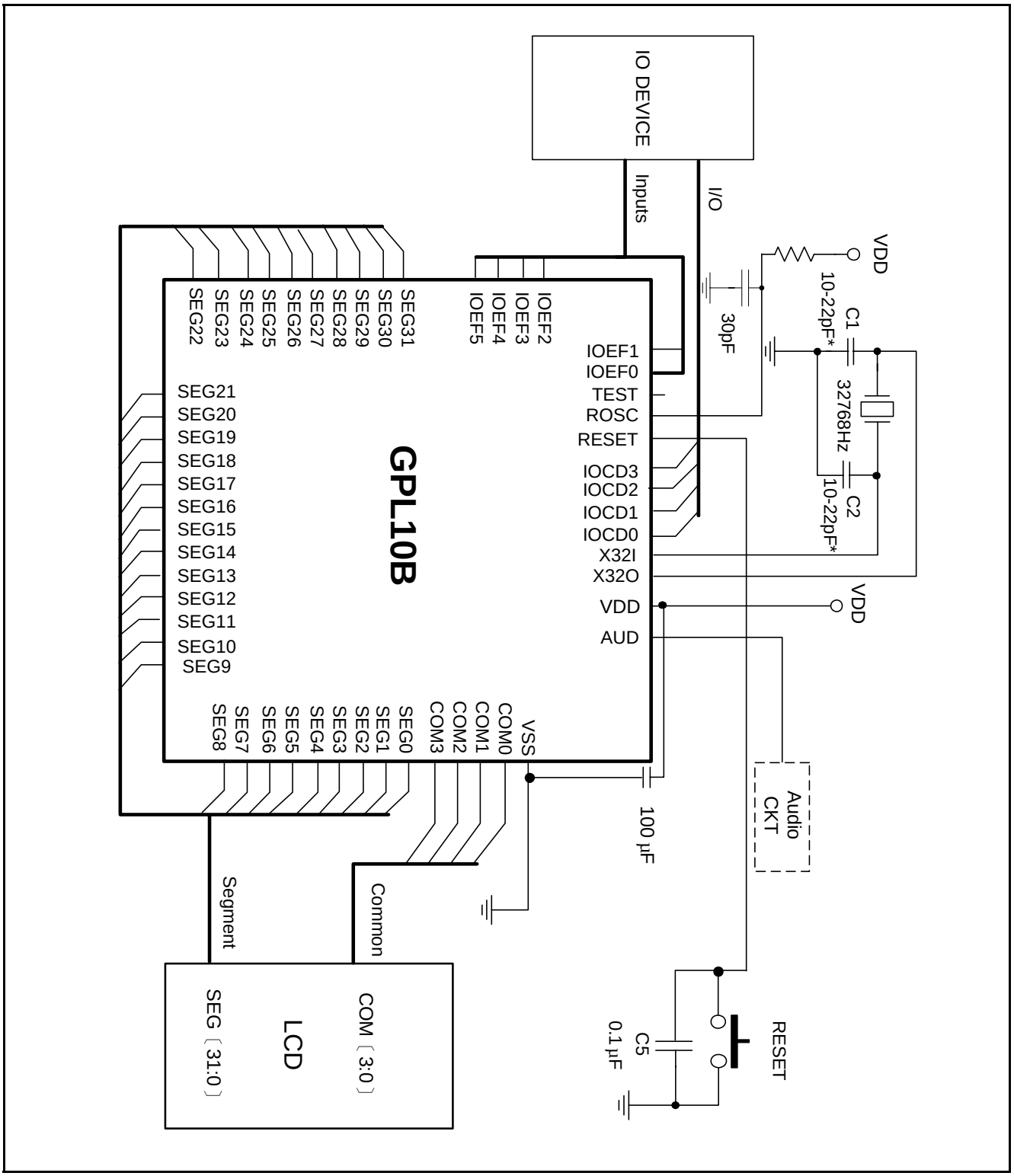
Characteristics	Symbol	Limits			Unit	Test condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC}	-	-	4.0	MHz	VDD = 2.0V
CPU Clock	F_{CPU}	-	-	2.0	MHz	$F_{CPU} = F_{OSC}/2$ @ 2.0V
Frame Frequency of The LCD Drive	F_{FM1}	-	64	-	Hz	1/2 duty
		-	85	-	Hz	1/3 duty
		-	64	-	Hz	1/4 duty
Wake-up time	T_W	6T1	-	-	Sec.	-

T1 = 1 / (F_{OSC}), Tw = 3 x T1, $F_{CPU} = F_{OSC}/2$



8. APPLICATION CIRCUITS

8.1. GPL10B Application Circuit



Note:1. The capacitor values for crystal are for design guidance only. Different capacitor values (10-22pF) may be required for different crystal/ resonator used.

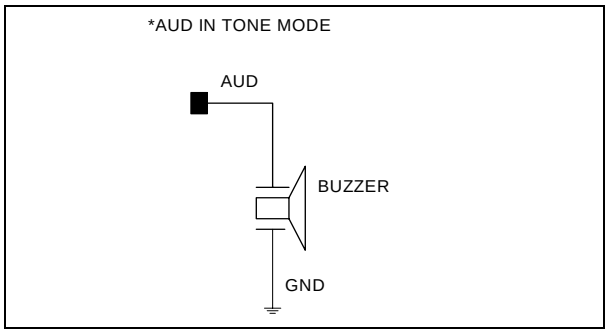
2. For crystal :

a. Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

b. This is the allowable frequency plus and minus deviation over a specified temperature range. It is specified in parts per million (PPM) referenced to the measured frequency at +25 degrees C.

c. Temperature range refers to the operating temperature range. Do not confuse this with temperature stability. Temperature stability depends on the application of the product. If a wide temperature stability is required, it should be communicated to the crystal manufacturer.

8.2. Audio Driver



9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPL10B - NnnV - C	Chip form
GPL10B - NnnV - QL02x	Halogen Free Package - LQFP 64
GPL10B - NnnV - QL02x	Halogen Free Package - LQFP 64 Lead free

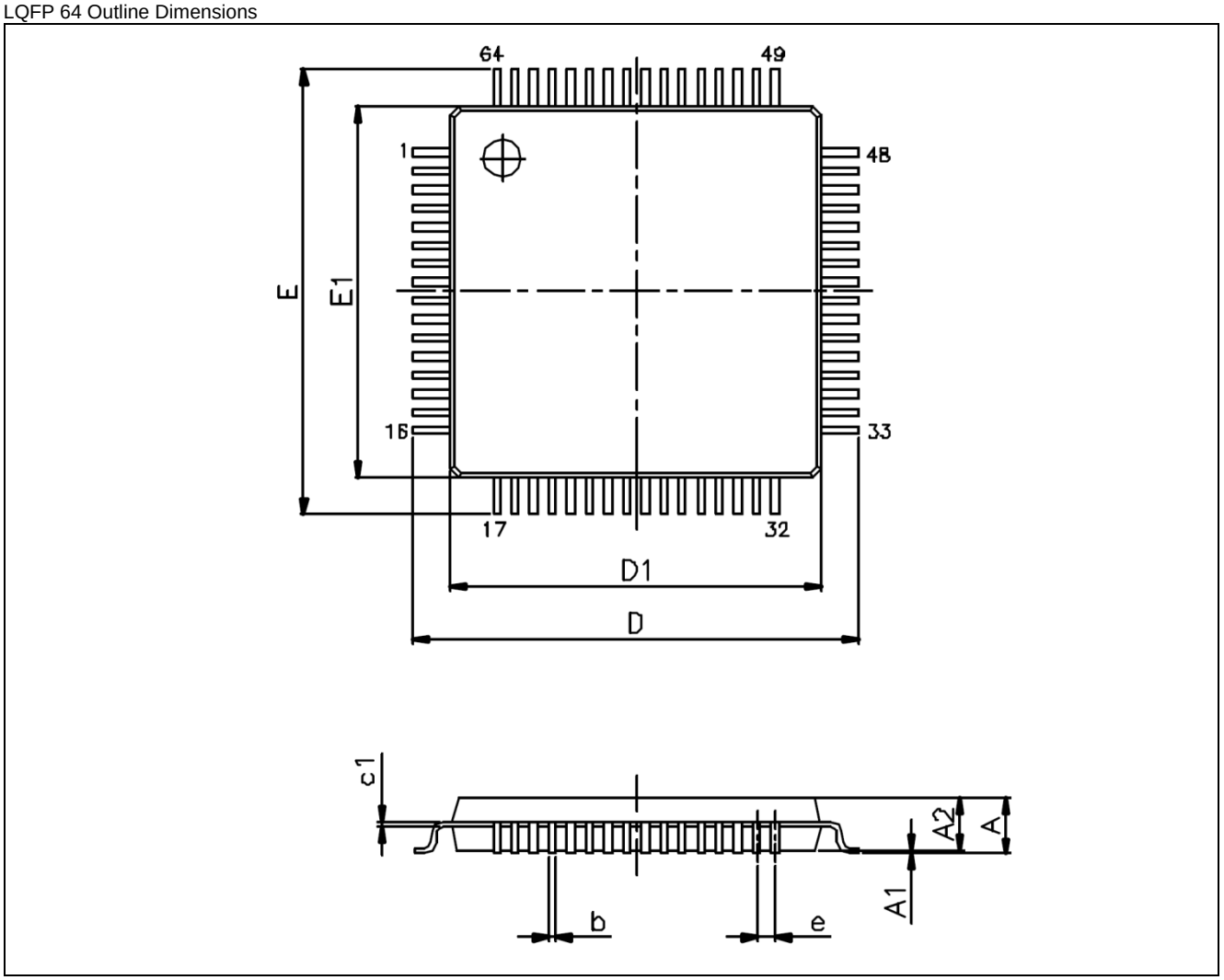
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

LQFP 64 Outline Dimensions



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	-	0.16
D	12.00		
D1	10.00		
E	12.00		
E1	10.00		
e	0.50 BSC.		

10. DISCLAIMER

The information appearing in this publication is believed to be accurate.

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11. REVISION HISTORY

Date	Revision #	Description	Page
May 29, 2014	1.5	1. Modify 7.1. 2. Modify 8.1 Note: adds the description of crystal.	15 18
Mar. 12, 2014	1.4	Remove P3 Note: Patent Circuitry Included. Taiwan Patent No. 68824.	3
OCT. 31, 2012	1.3	1. Modify 7.4 Relationships between the R_{OSC} and the $F_{OSC.}$ 2. Modify 7.5 Relationships between the F_{OSC} and the VDD.	16 16
MAR. 11, 2010	1.2	1. Modify 5.7. Interrupts 2. Modify 5.10. Output Waveform of the LCD Driver	6 8, 9, 11
DEC. 30, 2009	1.1	1. Add 7.7 The Relationships between the R_{OSC32K} and the F_{32K}. 2. Add 7.8 The Relationships between the F_{32K} and the VDD.	16
JUL. 10, 2008	1.0	1.Modify 7.2 DC Characteristics(VDD = 3.0V, TA = 25℃) 2.Modify 7.3 DC Characteristics(VDD = 4.5V, TA = 25℃) 3. Modify 7.4 Relationships between the R_{OSC} and the F_{CPU} 4. Modify 7.5 Relationships between the F_{CPU} and the VDD 5. Modify 7.6 Relationships between the F_{CPU} and the I_{OP}	14 14 15 15 15
FEB. 14, 2008	0.1	Original Note: The GPL10B data sheet v1.0 is a continued version of GPL10A5 data sheet v1.4.	21