

OPA4277-SP Radiation Hardened High-Precision Operational Amplifier

1 Features

- QMLV Qualified: [5962-16209](#)
 - Radiation Hardness Assurance (RHA) up to Total Ionizing Dose (TID) 50 krad(Si)
 - ELDRS-Free (See [Radiation Report](#))
 - Single Event Latchup (SEL) Immune to LET = 85 MeV-cm²/mg
- Ultra-Low Offset Voltage: 20 μ V
- Ultra-Low Drift: ± 0.15 μ V/°C
- High Open-Loop Gain: 134 dB
- High Common-Mode Rejection: 140 dB
- High-Power Supply Rejection: 130 dB
- Wide Supply Range: ± 2 to ± 18 V
- Low-Quiescent Current: 800 μ A/Amplifier
- Available in 14-lead CFP With Industry Standard Quad Operational Amplifier Pinout

2 Applications

- Space Satellite Temperature and Position Sensing
- High-Accuracy Space Instrumentation
- Space Precision and Scientific Applications
 - Transducer Amplifier
 - Bridge Amplifier
 - Strain Gage Amplifier
 - Precision Integrator

3 Description

The OPA4277-SP precision operational amplifier replaces the industry standard LM124-SP. It offers improved noise and two orders of magnitude lower input offset voltage. Features include ultra-low offset voltage and drift, low-bias current, high common-mode rejection, and high-power supply rejection.

The OPA4277-SP operates from ± 2 - to ± 18 -V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-SP precision operational amplifier is specified for real-world applications; a single limit applies over the ± 5 - to ± 15 -V supply range. High performance is maintained as the amplifier swings to the specified limits.

The OPA4277-SP is easy to use and free from phase inversion and overload problems found in some operational amplifiers. It is stable in unity gain and provides excellent dynamic behavior over a wide range of load conditions. The OPA4277-SP features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Device Information⁽¹⁾

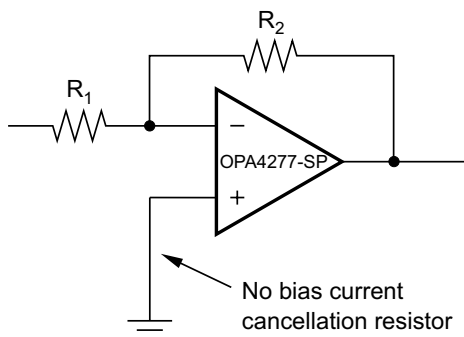
PART NUMBER	GRADE	PACKAGE
5962L1620901VYC	50 krad(Si) ELDRS-free	14-lead CFP (HFR)
5962L1620901VXA		28-lead CDIP (JDJ)
5962L1620901V9A		KGD ⁽²⁾
OPA4277HFR/EM	Engineering Samples ⁽³⁾	14-lead CFP (HFR)

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) KGD = known good die.

(3) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warrantied for performance over the full MIL specified temperature range of -55°C to 125°C or operating life.

Simplified Schematic



Copyright © 2016, Texas Instruments Incorporated



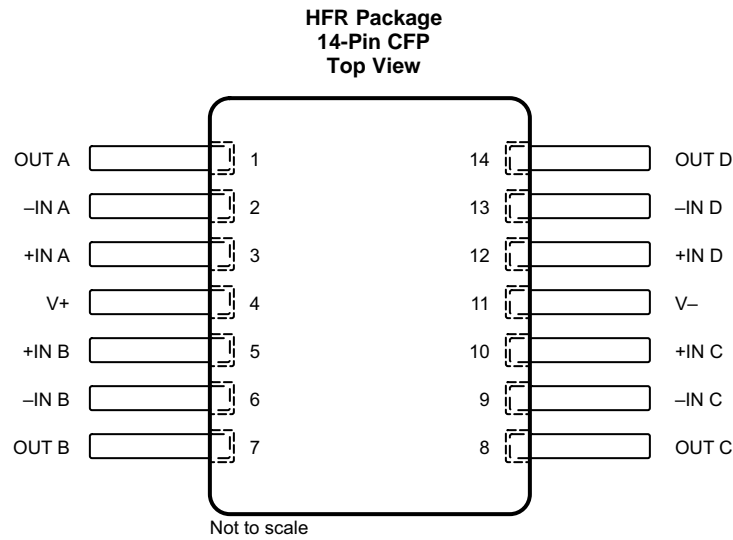
Table of Contents

1 Features	1	7.3 Feature Description	13
2 Applications	1	7.4 Device Functional Modes	14
3 Description	1	8 Application and Implementation	15
4 Revision History	2	8.1 Application Information	15
5 Pin Configuration and Functions	3	8.2 Typical Application	15
5.1 Bare Die Information	5	9 Power Supply Recommendations	17
6 Specifications	6	10 Layout	17
6.1 Absolute Maximum Ratings	6	10.1 Layout Guidelines	17
6.2 ESD Ratings	6	10.2 Layout Example	18
6.3 Recommended Operating Conditions	6	11 Device and Documentation Support	19
6.4 Thermal Information	6	11.1 Receiving Notification of Documentation Updates	19
6.5 Electrical Characteristics	7	11.2 Community Resources	19
6.6 Typical Characteristics	9	11.3 Trademarks	19
7 Detailed Description	13	11.4 Electrostatic Discharge Caution	19
7.1 Overview	13	11.5 Glossary	19
7.2 Functional Block Diagram	13	12 Mechanical, Packaging, and Orderable Information	20

4 Revision History

Changes from Original (December 2016) to Revision A	Page
• Changed <i>Features</i> section	1
• Added new device packages	1
• Updated <i>Pin Configurations and Functions</i> section	3
• Updated <i>Recommended Operating Conditions</i> table	6
• Updated Figure 3	9

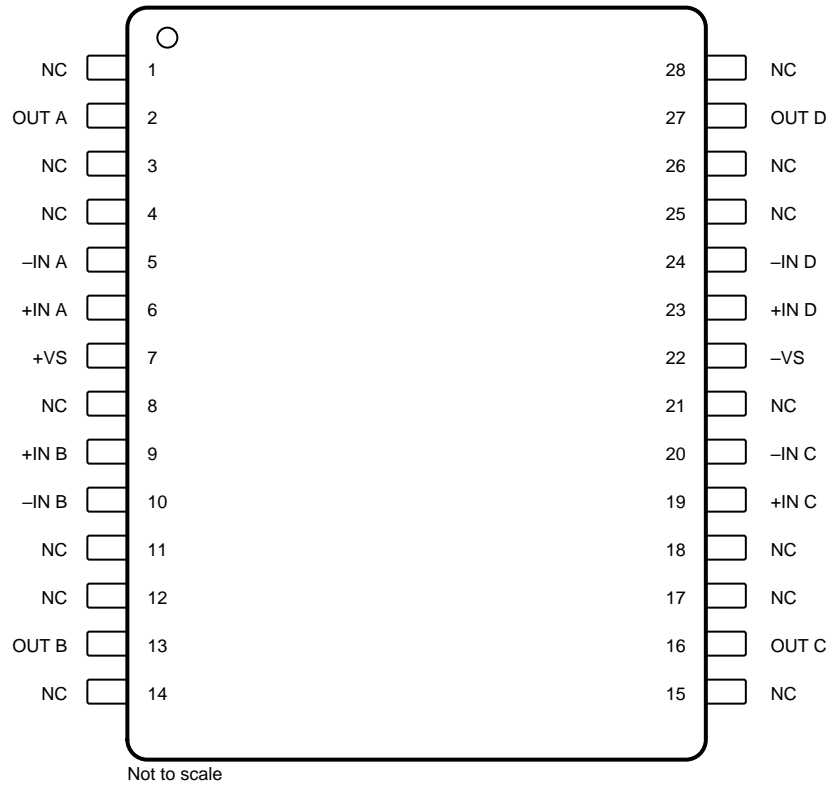
5 Pin Configuration and Functions



Pin Functions: CFP

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT A	O	Output channel A.
2	-IN A	I	Inverting input channel A.
3	+IN A	I	Noninverting input channel A.
4	V+	—	Positive (highest) power supply.
5	+IN B	I	Noninverting input channel B.
6	-IN B	I	Inverting input channel B.
7	OUT B	O	Output channel B.
8	OUT C	O	Output channel C.
9	-IN C	I	Inverting input channel C.
10	+IN C	I	Noninverting input channel C.
11	V-	—	Negative (lowest) power supply.
12	+IN D	I	Noninverting input channel D.
13	-IN D	I	Inverting input channel D.
14	OUT D	O	Output channel D.

JDJ Package
28-Pin CDIP
Top View



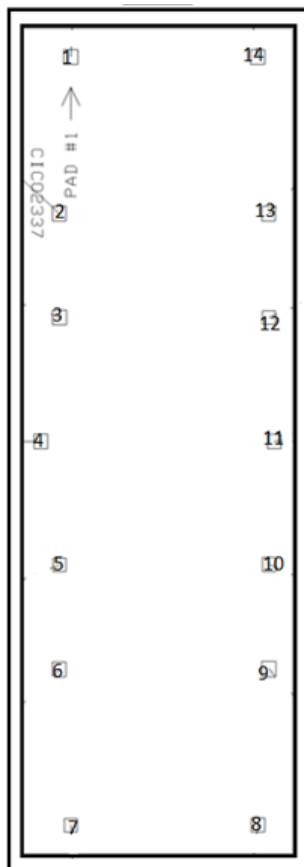
NC - no internal connection

Pin Functions: CDIP

PIN		I/O	DESCRIPTION
NO.	NAME		
1, 3, 4, 8, 11, 12, 14, 15, 17, 18, 21, 25, 26, 28	NC	—	Not connected.
2	OUT A	O	Output (channel A).
5	-IN A	I	Inverting input (channel A).
6	+IN A	I	Noninverting input (channel A).
7	+VS	—	Positive (highest) power supply.
9	+IN B	I	Inverting input (channel B).
10	-IN B	I	Noninverting input (channel B).
13	OUT B	O	Output (channel B).
16	OUT C	O	Output (channel C).
19	+IN C	I	Inverting input (channel C).
20	-IN C	I	Noninverting input (channel C).
22	-VS	—	Negative (lowest) power supply.
23	+IN D	I	Inverting input (channel D).
24	-IN D	I	Noninverting input (channel D).
27	OUT D	O	Output (channel D).

5.1 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Negative (lower) Power Supply	AlCu (0.5%)	990 to 1210 nm



Bond Pad Coordinates in Microns⁽¹⁾

PAD		I/O	DESCRIPTION	X MIN	Y MIN	X MAX	Y MAX
NO.	NAME						
1	OUT A	O	Output channel A.	1791.042	7290.340	1901.751	7401.049
2	-IN A	I	Inverting input channel A.	1701.719	6111.536	1807.397	6217.213
3	+IN A	I	Noninverting input channel A.	1701.719	5326.505	1812.429	5437.215
4	V+	—	Positive (higher) power supply.	1555.784	4390.507	1661.461	4498.700
5	+IN B	I	Noninverting input channel B.	1706.752	3462.057	1807.397	3562.702
6	-IN B	I	Inverting input channel B.	1701.719	2671.994	1807.397	2777.671
7	OUT B	O	Output channel B.	1796.074	1498.222	1896.719	1598.867
8	OUT C	O	Output channel C.	3278.071	1498.222	3383.748	1603.900
9	-IN C	I	Inverting input channel C.	3362.361	2671.994	3473.071	2782.704
10	+IN C	I	Noninverting input channel C.	3367.393	3462.057	3473.071	3567.734
11	V-	—	Negative (lower) power supply.	3407.651	4391.765	3513.329	4497.442
12	+IN D	I	Noninverting input channel D.	3367.393	5331.537	3468.038	5432.182
13	-IN D	I	Inverting input channel D.	3362.361	6111.536	3468.038	6217.213
14	OUT D	O	Output channel D.	3273.039	7290.340	3383.748	7401.049

(1) Substrate must be biased to V-, negative (lower) power supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage = (V+) – (V–)		36	V
Input voltage	(V–) – 0.7	(V+) + 0.7	V
Output short circuit	Continuous		
Operating temperature	–55	125	°C
Junction temperature		150	°C
Lead temperature (soldering, 10 s)		300	°C
Storage temperature, T _{stg}	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
	Machine model (MM)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Dual supply voltage	±2	±18	V
Tested supply voltage	±5	±15	V
T _J Operating junction temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA4277-SP	UNIT
		CDIP (JDJ)	
		28 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	66.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	19.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	26.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	26.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

At $T_J = 25^\circ\text{C}$, $V_S = \pm 5\text{ V}$ to $\pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	$T_J = 25^\circ\text{C}$, pre- and post-irradiated		± 20	± 65	μV
		$T_J = -55^\circ\text{C}$ to 125°C , pre-irradiated			± 140	
dV_{OS}/dT	Input offset voltage temperature drift	$T_J = -55^\circ\text{C}$ to 125°C , pre-irradiated		± 0.15		$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage	vs time		0.2		$\mu\text{V}/\text{mo}$
		vs power supply, $V_S = \pm 2\text{ V}$ to $\pm 18\text{ V}$, $T_J = 25^\circ\text{C}$, pre- and post-irradiated		± 0.3	± 1	$\mu\text{V}/\text{V}$
		$V_S = \pm 2\text{ V}$ to $\pm 18\text{ V}$, $T_J = -55^\circ\text{C}$ to 125°C			± 1	
	Channel separation	dc		0.1		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT						
I_B	Input bias current	$T_J = -55^\circ\text{C}$ to 125°C			± 17.5	nA
		$T_J = 25^\circ\text{C}$, pre- and post-irradiated			± 17.5	
I_{OS}	Input offset current	$T_J = -55^\circ\text{C}$ to 125°C			± 17.5	nA
		$T_J = 25^\circ\text{C}$, pre- and post-irradiated			± 17.5	
NOISE						
	Input voltage noise	$f = 0.1$ to 10 Hz		0.22		μV_{pp}
	Input voltage noise density	$f = 10\text{ Hz}$		12		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$		8		
		$f = 1\text{ kHz}$		8		
		$f = 10\text{ kHz}$		8		
i_n	Input noise current density	$f = 1\text{ kHz}$		0.2		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range	$T_J = 25^\circ\text{C}$, pre- and post-irradiated	$(V_-) + 2$		$(V_+) - 2$	V
CMRR	Common-mode rejection ratio	$(V_-) + 2\text{ V} < V_{CM} < (V_+) - 2\text{ V}$, $T_J = 25^\circ\text{C}$, post-irradiated	114	140		dB
		$(V_-) + 2\text{ V} < V_{CM} < (V_+) - 2\text{ V}$, $T_J = -55^\circ\text{C}$ to 125°C	114			
INPUT IMPEDANCE						
	Differential			100 3		$\text{M}\Omega$ pF
	Common mode	$(V_-) + 2\text{ V} < V_{CM} < (V_+) - 2\text{ V}$		250 3		$\text{G}\Omega$ pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$V_O = (V_{O-}) + 0.5\text{ V}$ to $(V_{O+}) - 1.2\text{ V}$, $R_L = 10\text{ k}\Omega$		140		dB
		$V_O = (V_{O-}) + 1.5\text{ V}$ to $(V_{O+}) - 1.5\text{ V}$, $R_L = 2\text{ k}\Omega$, $T_J = -55^\circ\text{C}$ to 125°C	118	134		
		$V_O = (V_{O-}) + 1.5\text{ V}$ to $(V_{O+}) - 1.5\text{ V}$, $R_L = 2\text{ k}\Omega$, $T_J = 25^\circ\text{C}$, pre- and post-irradiated	118	134		
		$V_O = (V_{O-}) + 3.4\text{ V}$ to $(V_{O+}) - 3.4\text{ V}$, $R_L = 600\ \Omega$, $V_S = \pm 7\text{ V}$, $T_J = -55^\circ\text{C}$ to 125°C	118	134		
		$V_O = (V_{O-}) + 3.4\text{ V}$ to $(V_{O+}) - 3.4\text{ V}$, $R_L = 600\ \Omega$, $V_S = \pm 7\text{ V}$, $T_J = 25^\circ\text{C}$, pre- and post-irradiated	118	134		

Electrical Characteristics (continued)

 At $T_J = 25^\circ\text{C}$, $V_S = \pm 5\text{ V}$ to $\pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			1		MHz
SR	Slew rate			0.8		V/ μs
	Settling time	0.1%, 10-V step, $V_S = \pm 15\text{ V}$, $G = 1$		14		μs
		0.01%, 10-V step, $V_S = \pm 15\text{ V}$, $G = 1$		16		
THD + N	Total harmonic distortion + noise	1 kHz, $G = 1$, $V_O = 3.5\text{ V}_{\text{rms}}$		0.002%		
OUTPUT						
V_O	Output voltage	$R_L = 10\text{ k}\Omega$, $T_J = 25^\circ\text{C}$, pre- and post-irradiated	$(V_-) + 0.5$		$(V_+) - 1.2$	V
		$R_L = 10\text{ k}\Omega$, $T_J = -55^\circ\text{C}$ to 125°C	$(V_-) + 0.5$		$(V_+) - 1.2$	
		$R_L = 2\text{ k}\Omega$, $T_J = 25^\circ\text{C}$, pre- and post-irradiated	$(V_-) + 1.5$		$(V_+) - 1.5$	
		$R_L = 2\text{ k}\Omega$, $T_J = -55^\circ\text{C}$ to 125°C	$(V_-) + 1.5$		$(V_+) - 1.5$	
		$T_J = 25^\circ\text{C}$, $R_L = 600\ \Omega$, pre- and post-irradiated	$(V_-) + 3.4$		$(V_+) - 3.4$	
		$R_L = 600\ \Omega$, $V_S = \pm 7\text{ V}$, $T_J = -55^\circ\text{C}$ to 125°C	$(V_-) + 3.4$		$(V_+) - 3.4$	
I_{SC}	Short-circuit current			± 35		mA
C_{LOAD}	Capacitive load drive	$f = 350\text{ kHz}$, $I_O = 0$		See Typical Characteristics		
POWER SUPPLY						
V_S	Specified voltage	$T_J = -55^\circ\text{C}$ to 125°C	± 5	± 7	± 15	V
		$T_J = 25^\circ\text{C}$, pre- and post-irradiated	± 5	± 7	± 15	
V_S	Operating voltage	$T_J = -55^\circ\text{C}$ to 125°C	± 2	± 7	± 18	V
		$T_J = 25^\circ\text{C}$, pre- and post-irradiated	± 2	± 7	± 18	
I_Q	Quiescent current per amplifier	$I_O = 0$, $T_J = 25^\circ\text{C}$, pre- and post-irradiated		± 790	± 850	μA
		$I_O = 0$, $T_J = -55^\circ\text{C}$ to 125°C			± 900	

6.6 Typical Characteristics

At $T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$, pre-irradiated (unless otherwise noted).

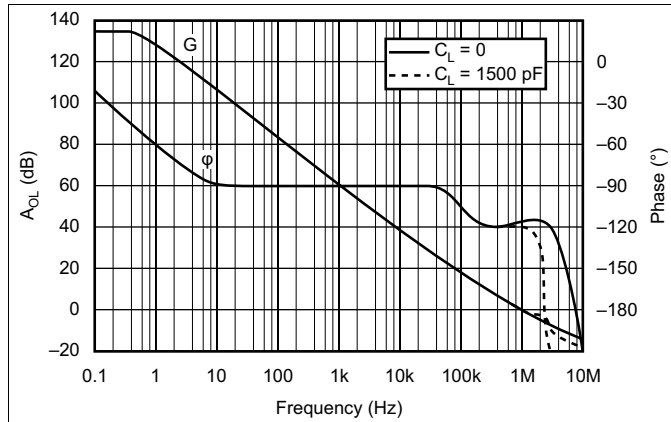


Figure 1. Open-Loop Gain/Phase vs Frequency

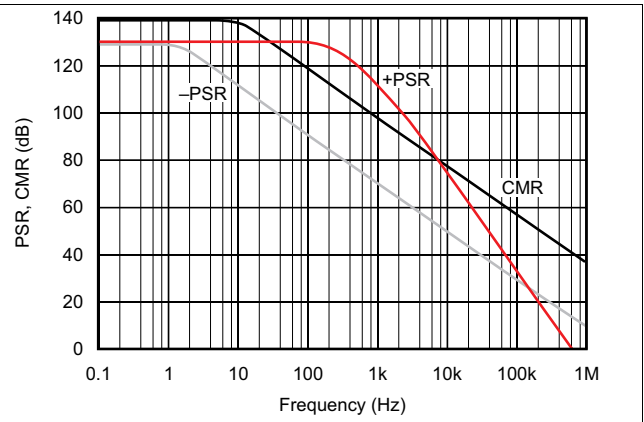


Figure 2. Power Supply and Common-Mode Rejection vs Frequency

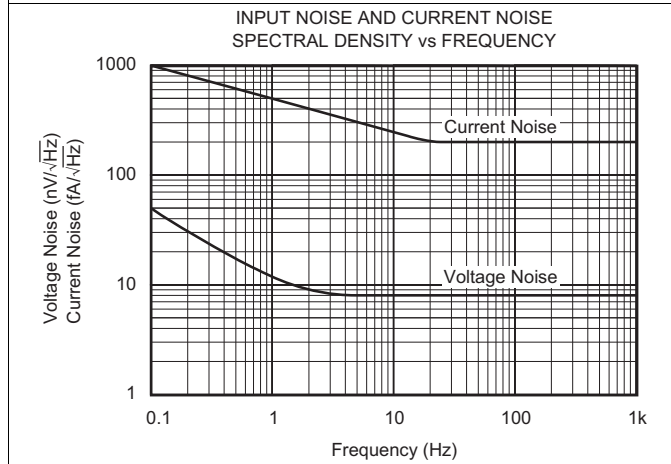
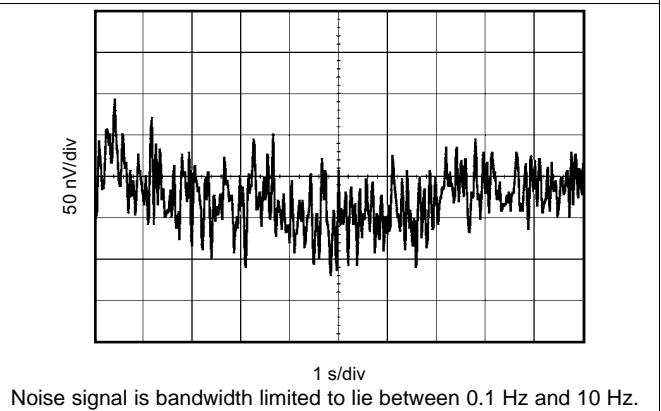
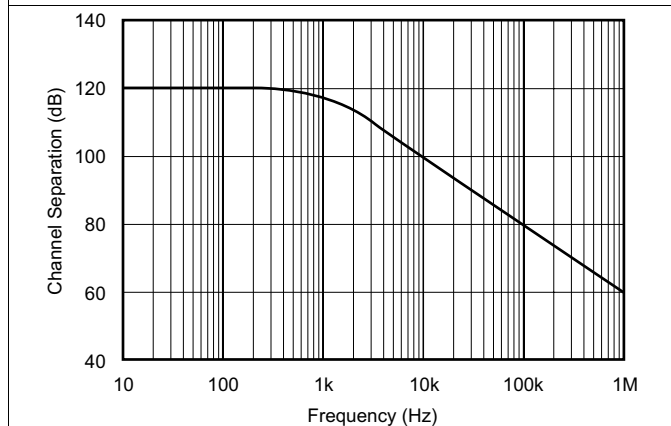


Figure 3. Input Noise and Current Noise Spectral Density vs Frequency



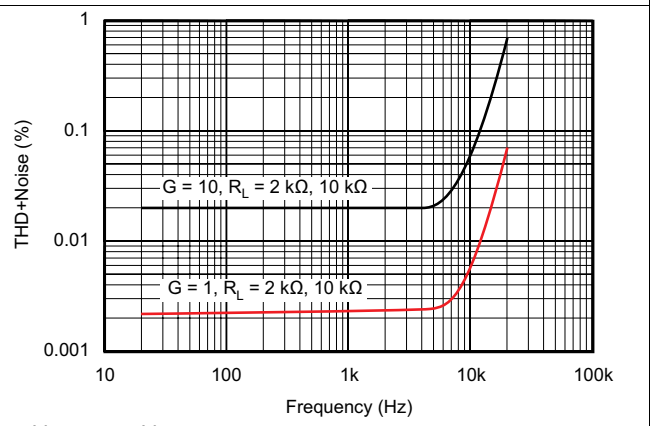
Noise signal is bandwidth limited to lie between 0.1 Hz and 10 Hz.

Figure 4. Input Noise Voltage vs Time



$G = 1$, measured channel A to D or B to C.
Other combinations yield similar or improved rejection.

Figure 5. Channel Separation vs Frequency



$V_{OUT} = 3.5\text{ Vrms}$

Figure 6. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$, pre-irradiated (unless otherwise noted).

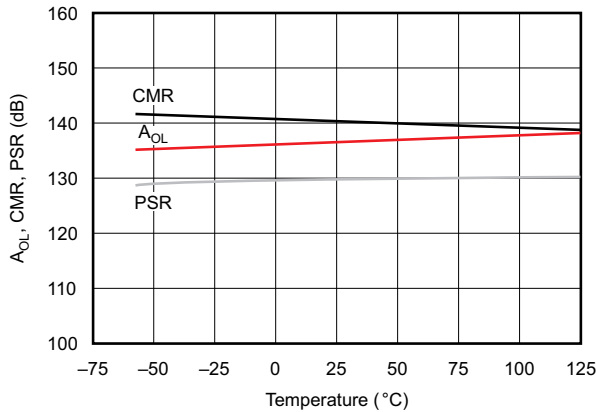
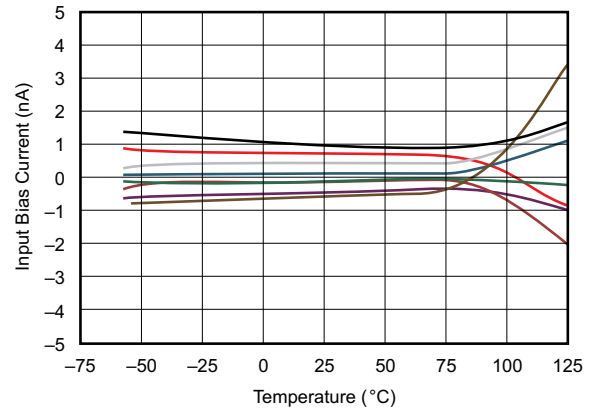


Figure 7. A_{OL} , CMR, PSR vs Temperature



Curves represent typical production units.

Figure 8. Input Bias Current vs Temperature

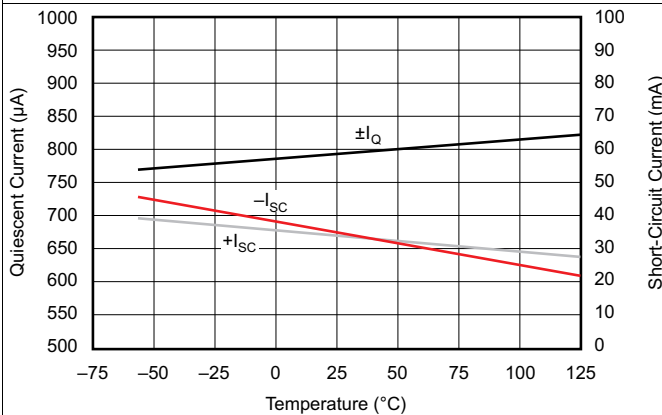
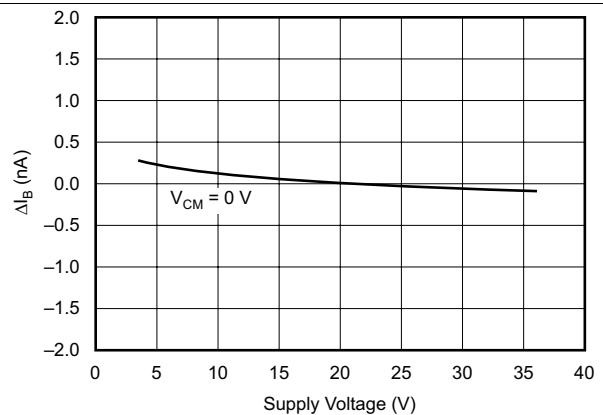
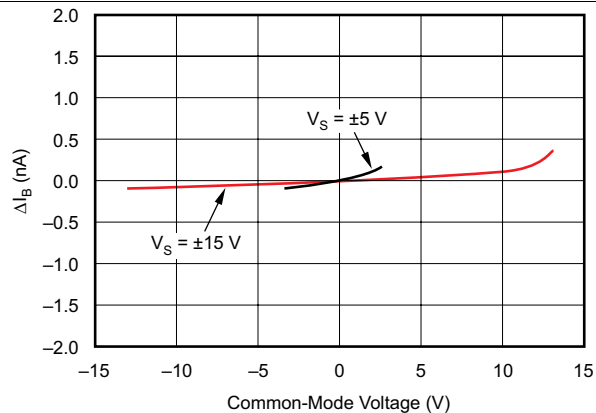


Figure 9. Quiescent Current and Short-Circuit Current vs Temperature



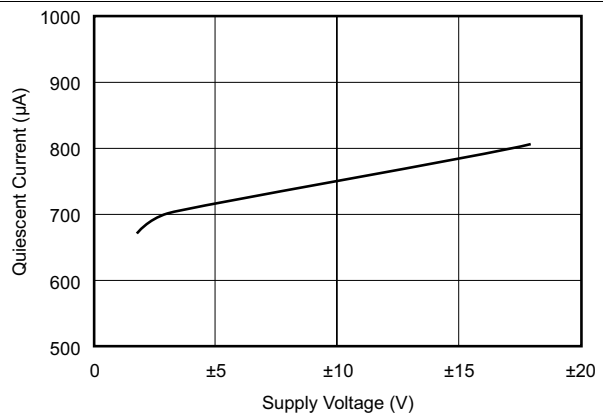
Curve shows normalized change in bias current with respect to $V_S = \pm 10\text{ V}$ (+20 V). Typical I_B may range from -0.5 nA to 0.5 nA at $V_S = \pm 10\text{ V}$.

Figure 10. Change in Input Bias Current vs Power Supply Voltage



Curve shows normalized change in bias current with respect to $V_{CM} = 0\text{ V}$. Typical I_B may range from -0.5 nA to 0.5 nA at $V_{CM} = 0\text{ V}$.

Figure 11. Change in Input Bias Current vs Common-Mode Voltage



Per amplifier

Figure 12. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$, pre-irradiated (unless otherwise noted).

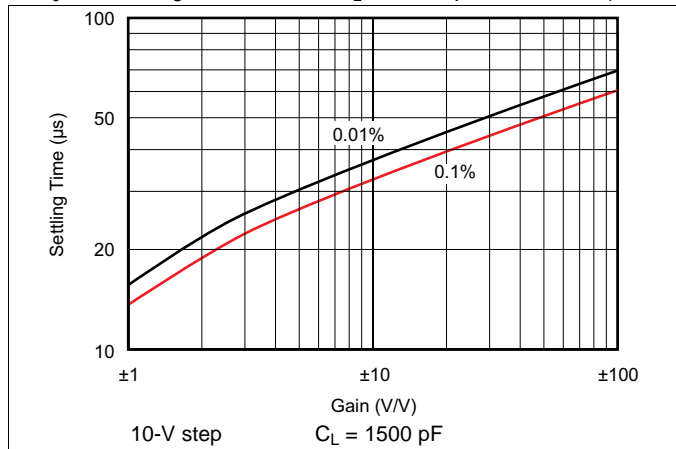


Figure 13. Settling Time vs Closed-Loop Gain

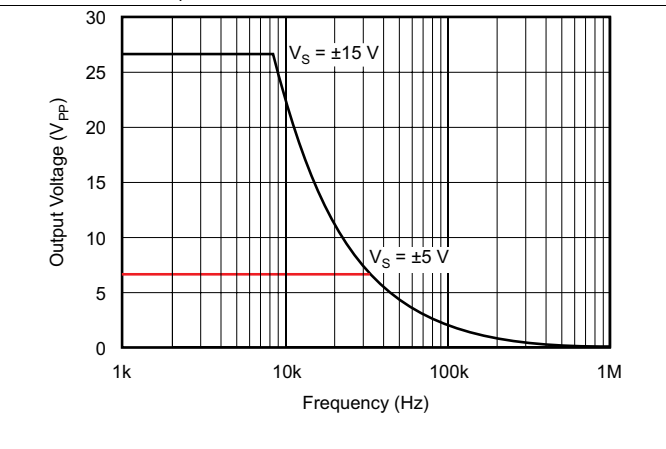


Figure 14. Maximum Output Voltage vs Frequency

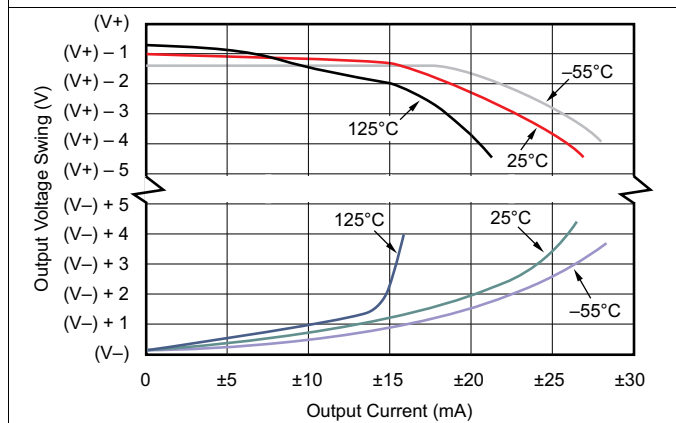


Figure 15. Output Voltage Swing vs Output Current

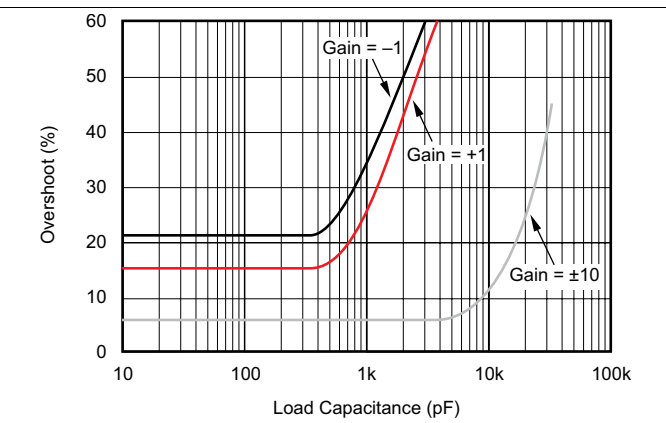


Figure 16. Small-Signal Overshoot vs Load Capacitance

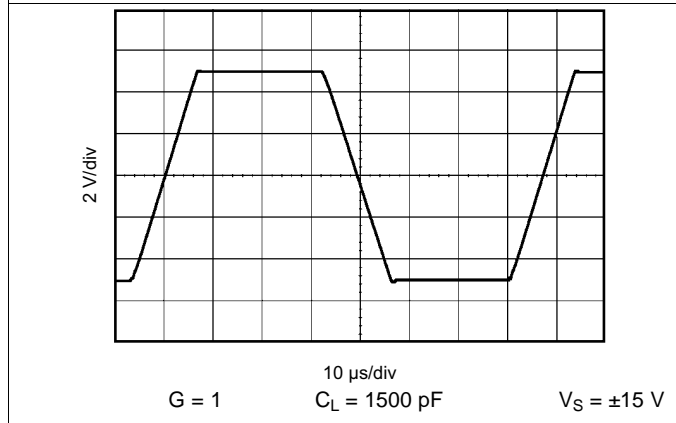


Figure 17. Large-Signal Step Response

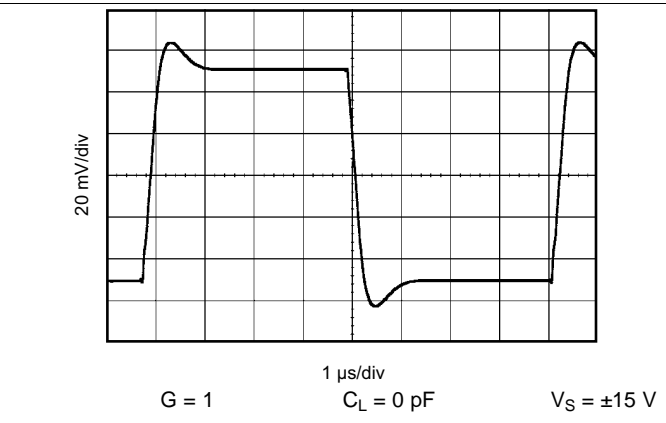
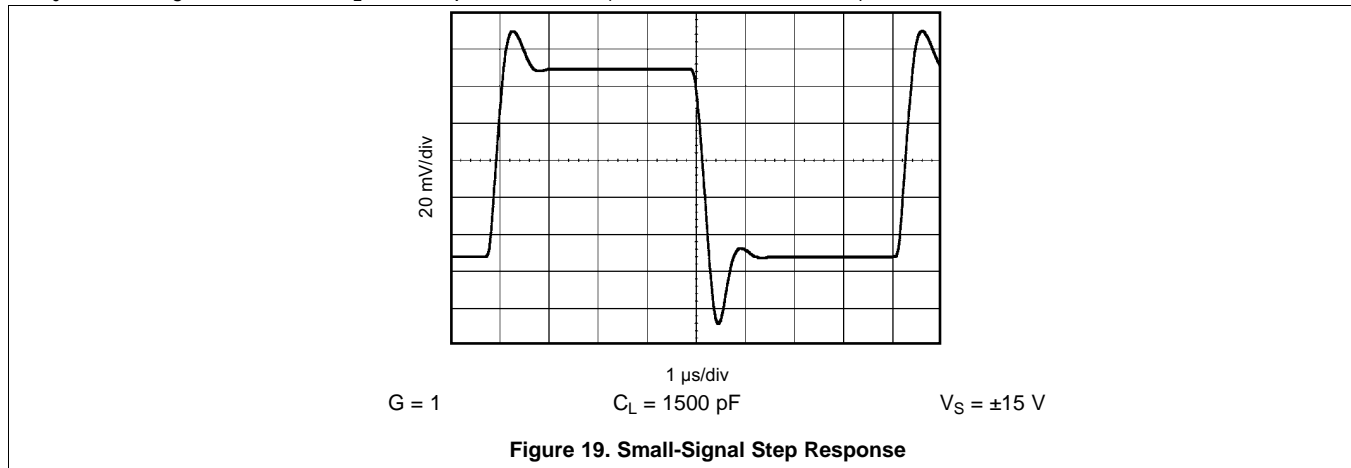


Figure 18. Small-Signal Step Response

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$, pre-irradiated (unless otherwise noted).

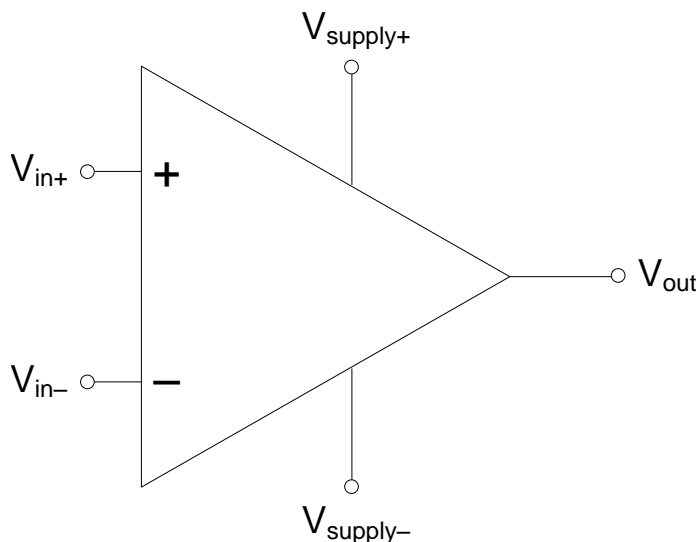


7 Detailed Description

7.1 Overview

The OPA4277-SP precision operational amplifier replaces the industry standard LM124-SP. It offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

The OPA4277-SP operates from ± 2 - to ± 18 -V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-SP precision operational amplifier is specified for real-world applications; a single limit applies over the ± 5 - to ± 15 -V supply range. High performance is maintained as the amplifier swings to the specified limits. Because the initial offset voltage (± 50 - μ V max) is so low, user adjustment is usually not required.

7.3.1 Input Protection

The inputs of the OPA4277-SP are protected with 1-k Ω series input resistors and diode clamps. The inputs can withstand ± 30 -V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the operational amplifier.

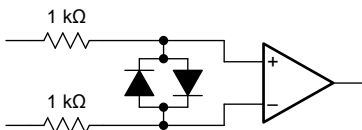


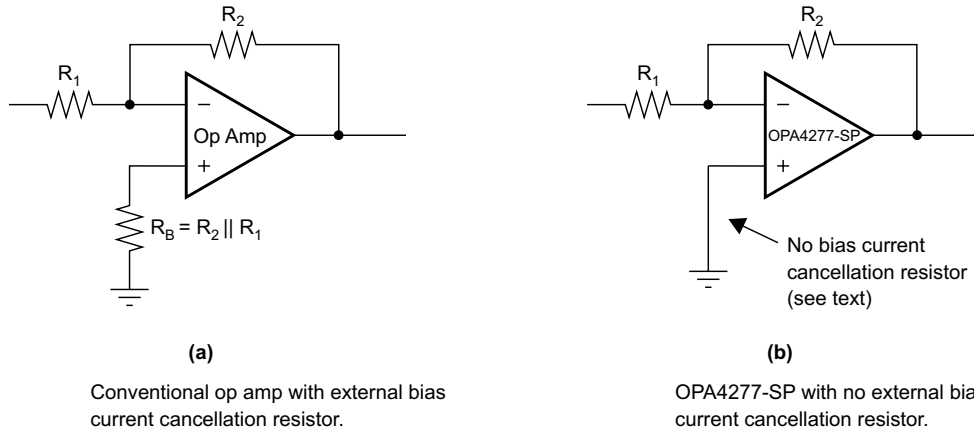
Figure 20. OPA4277-SP Input Protection

7.3.2 Input Bias Current Cancellation

The input stage base current of the OPA4277-SP is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

Feature Description (continued)

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor, as is often done with other operational amplifiers (see [Figure 21](#)). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.



Copyright © 2016, Texas Instruments Incorporated

Figure 21. Input Bias Current Cancellation

7.4 Device Functional Modes

The OPA4277-SP has a single functional mode and is operational when the power-supply voltage, (V+) – (V–), is less than 36 V.

8 Application and Implementation

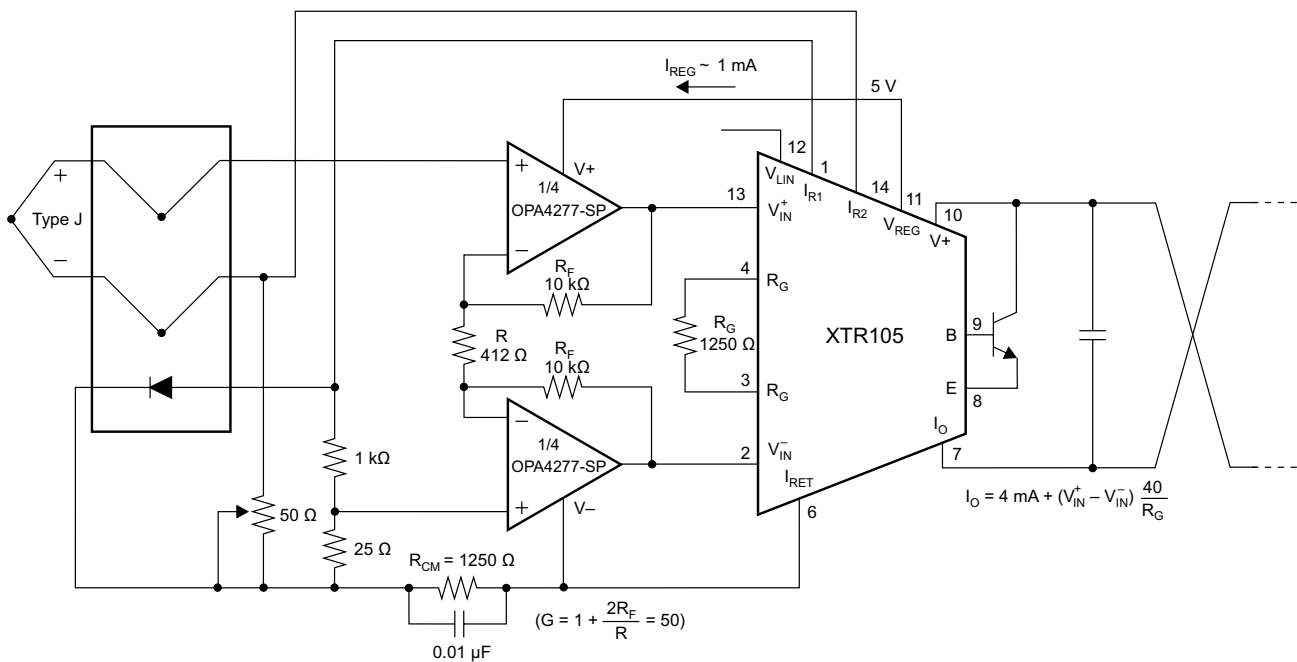
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA4277-SP is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1- μ F capacitors are adequate.

8.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

Figure 22. Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

8.2.1 Design Requirements

For the thermocouple low-offset, low-drift loop measurement with diode cold junction compensation shown in Figure 22, a gain of 50 is desired.

Typical Application (continued)

8.2.2 Detailed Design Procedure

Equation 1 shows the equation used to determine the resistor values needed for a gain of 50. Table 1 lists the design parameters.

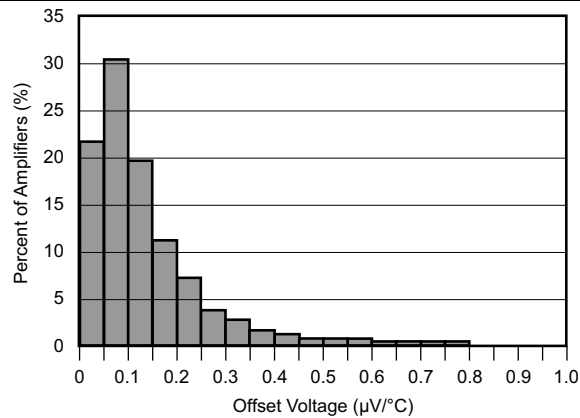
$$G = 1 + \frac{2R_F}{R} = 50 \tag{1}$$

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
R _F	10 kΩ
R	412 Ω

8.2.3 Application Curve

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.



Typical distribution of packaged units. Single, dual, and quad included.

Figure 23. Warm-Up Offset Voltage Drift

9 Power Supply Recommendations

OPA4277-SP operates from ± 2 - to ± 18 -V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-SP is specified for real-world applications; a single limit applies over the ± 5 - to ± 15 -V supply range. This allows a customer operating at $V_S = \pm 10$ V to have the same assured performance as a customer using ± 15 -V supplies. In addition, key parameters are assured over the specified temperature range, -55°C to 125°C . Most behavior remains unchanged through the full operating voltage range (± 2 to ± 18 V). Parameters which vary significantly with operating voltage or temperature are shown in the typical performance curves.

10 Layout

10.1 Layout Guidelines

The leadframe die pad should be soldered to a thermal pad on the PCB. Mechanical drawings located in [Mechanical, Packaging, and Orderable Information](#) show the physical dimensions for the package and pad.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

The OPA4277-SP has very-low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the OPA4277-SP. Cancel these thermal potentials by assuring that they are equal in both input terminals.

- Keep the thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as cooling fans.

10.2 Layout Example

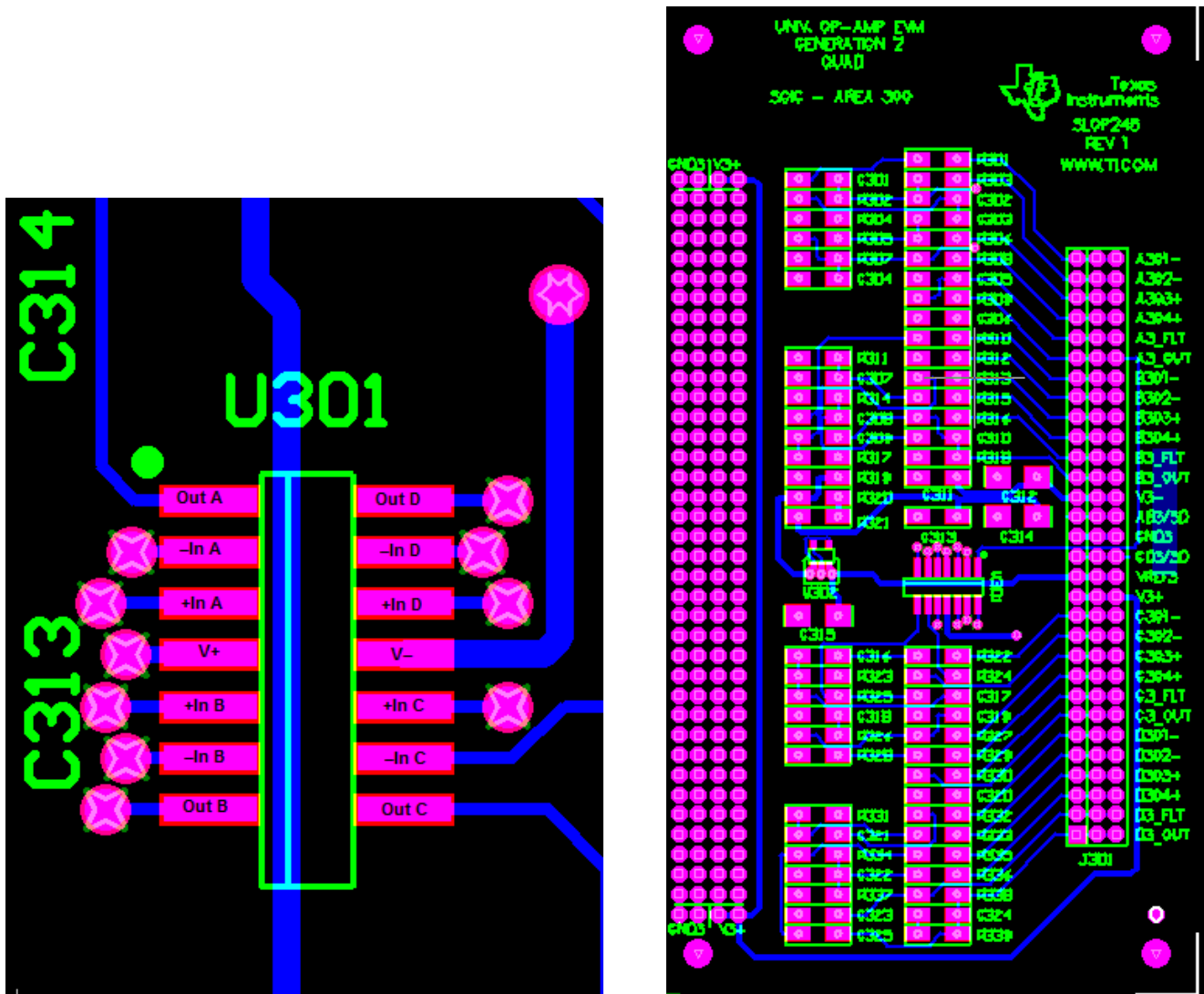


Figure 24. Board Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962L1620901V9A	ACTIVE	XCEPT	KGD	0	50	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962L1620901VXA	ACTIVE	CDIP SB	JDJ	28	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962L1620901VX A OPA4277-SP	Samples
5962L1620901VYC	ACTIVE	CFP	HFR	14	1	TBD	AU	N / A for Pkg Type	-55 to 125	5962L1620901VYC OPA4277-SP	Samples
OPA4277HFR/EM	ACTIVE	CFP	HFR	14	1	TBD	AU	N / A for Pkg Type	25 to 25	OPA4277HFR/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA4277-SP :

- Catalog: [OPA4277](#)
- Enhanced Product: [OPA4277-EP](#)

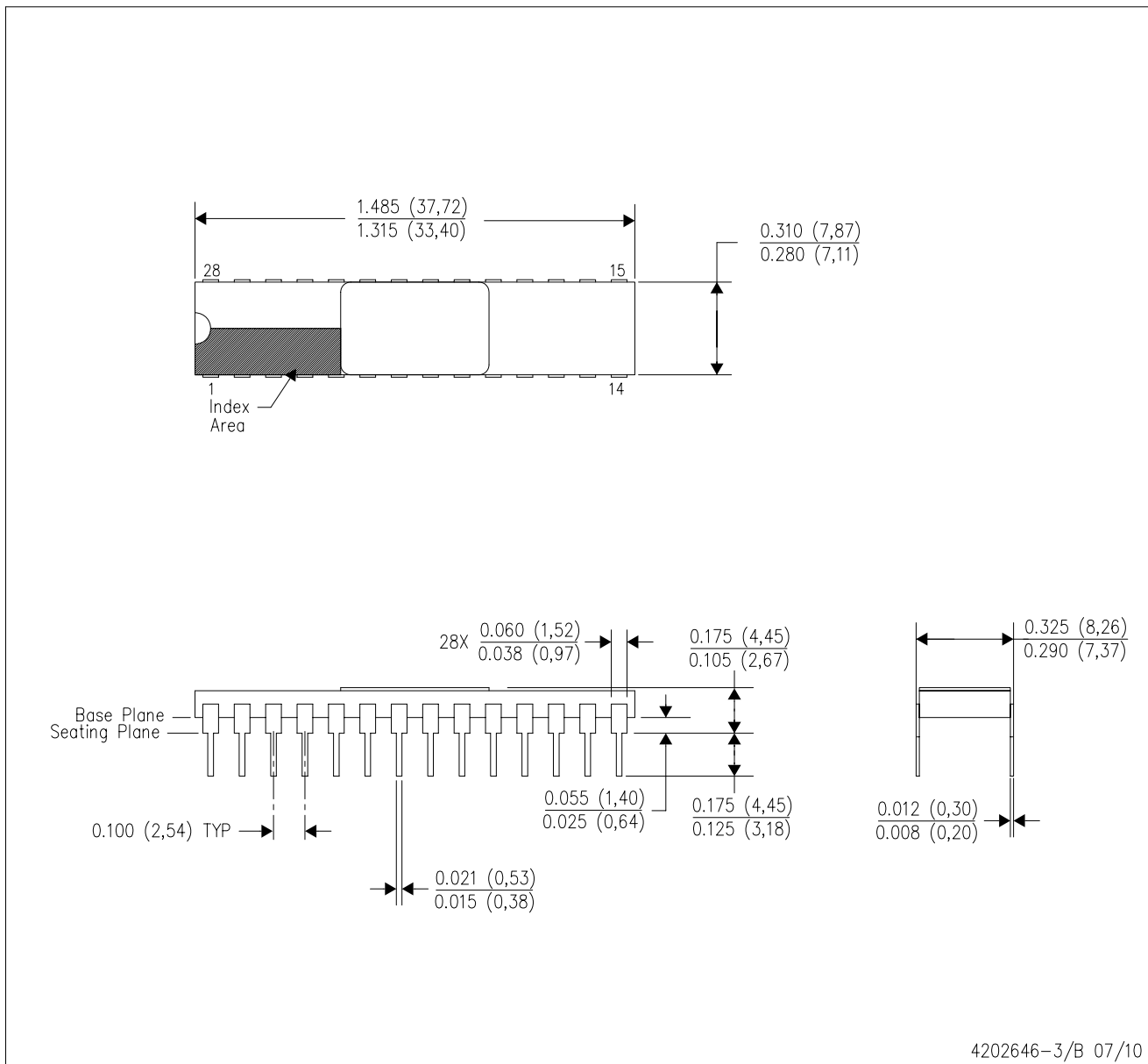
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

MECHANICAL DATA

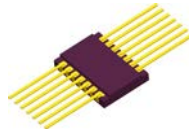
JDJ (R-CDIP-T28)

CERAMIC DUAL IN-LINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
 - This package is hermetically sealed with a metal lid.
 - The leads are gold plated and can be solderdipped.
 - Leads not shown for clarity purposes.
 - Lid and heat sink are connected to GND leads.

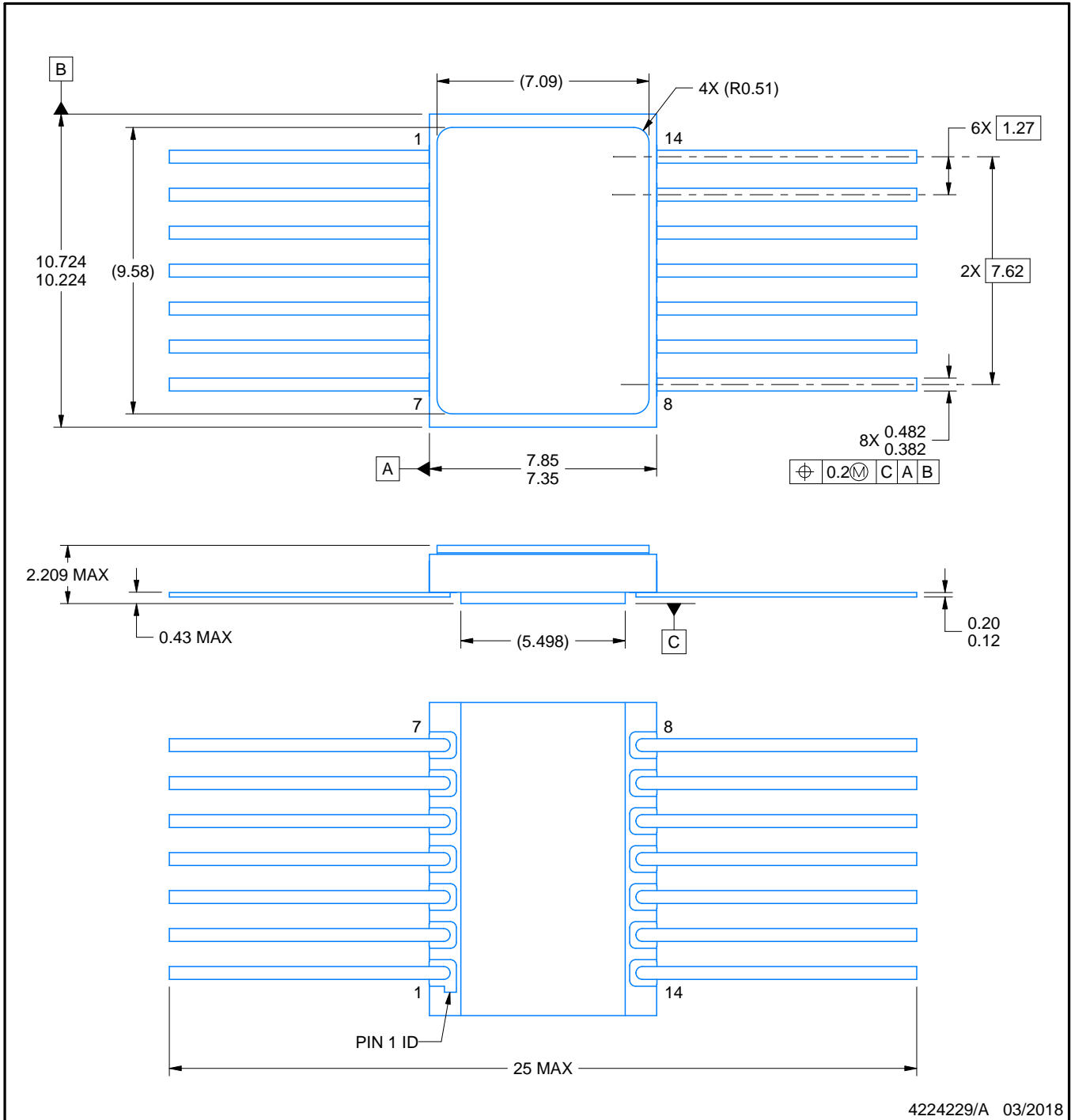
HFR0014A



PACKAGE OUTLINE

CFP - 2.209 mm max height

CERAMIC FLATPACK



4224229/A 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated