

PMV30UN

μ TrenchMOS™ ultra low level FET



1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PMV30UN in SOT23.

1.2 Features

- Surface mount package
- Fast switching.

1.3 Applications

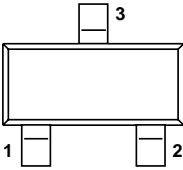
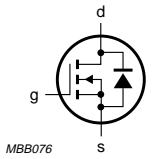
- Battery management
- High-speed switches.

1.4 Quick reference data

- $V_{DS} \leq 20\text{ V}$
- $I_D \leq 5.7\text{ A}$
- $P_{tot} \leq 1.9\text{ W}$
- $R_{DS(on)} \leq 36\text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT23 simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 <p>Top view MSB003</p>	 <p>MBB076</p>
2	source (s)		
3	drain (d)		

3. Limiting values

Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	20	V
V_{GS}	gate-source voltage (DC)		-	±8	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 4.5\text{ V}$; Figure 2 and 3	-	5.7	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 4.5\text{ V}$; Figure 2	-	3.65	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	23.1	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	1.9	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	1.6	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	6.4	A

4. Characteristics

Table 3: Characteristics

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ }^\circ\text{C}$	20	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS};$ Figure 9				
		$T_j = 25\text{ }^\circ\text{C}$	0.45	0.7	-	V
		$T_j = 150\text{ }^\circ\text{C}$	0.25	0.4	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 20\ \text{V}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ }^\circ\text{C}$	-	-	1	μA
		$T_j = 150\text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 8\ \text{V}; V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}; I_D = 2\ \text{A};$ Figure 7 and 8				
		$T_j = 25\text{ }^\circ\text{C}$	-	30	36	mΩ
		$T_j = 150\text{ }^\circ\text{C}$	-	48	57.6	mΩ
		$V_{GS} = 2.5\ \text{V}; I_D = 1.5\ \text{A};$ Figure 7 and 8	-	36	43	mΩ
		$V_{GS} = 1.8\ \text{V}; I_D = 1\ \text{A};$ Figure 7 and 8	-	44	63	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 5\ \text{A}; V_{DD} = 10\ \text{V}; V_{GS} = 4.5\ \text{V};$ Figure 13	-	7.4	-	nC
Q_{gs}	gate-source charge		-	1.2	-	nC
Q_{gd}	gate-drain (Miller) charge		-	1.8	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 20\ \text{V}; f = 1\ \text{MHz};$ Figure 11	-	460	-	pF
C_{oss}	output capacitance		-	100	-	pF
C_{rss}	reverse transfer capacitance		-	70	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\ \text{V}; R_L = 10\ \Omega; V_{GS} = 4.5\ \text{V}; R_G = 6\ \Omega$	-	7	-	ns
t_r	rise time		-	13	-	ns
$t_{d(off)}$	turn-off delay time		-	53	-	ns
t_f	fall time		-	13	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 1.7\ \text{A}; V_{GS} = 0\ \text{V};$ Figure 12	-	0.81	1.2	V