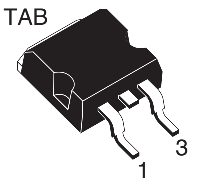
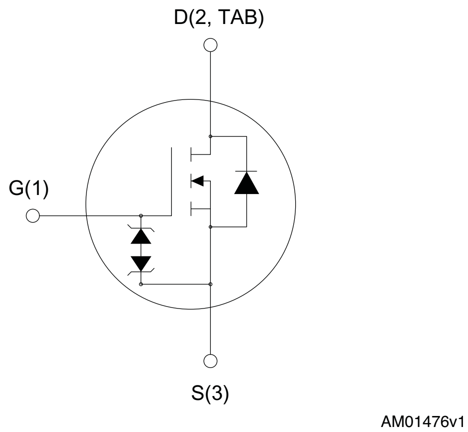
# Automotive-grade N-channel 800 V, 1.5 Ω typ., 5.2 A Zener-protected SuperMESH™ Power MOSFETs in $D^2PAK$ package

Datasheet - production data




**$D^2PAK$**

**Figure 1. Internal schematic diagram**




## Features

| Type | $V_{DS}$ (@Tjmax) | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STB9NK80Z | 800V | 1.8Ω | 5.2A |

- Designed for automotive applications and AEC-Q101 qualified
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Zener-protected
- Very low intrinsic capacitances

## Applications

- Switching application

## Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

**Table 1. Device summary**

| Order codes | Marking | Package | Packaging |
|---|---|---|---|
| STB9NK80Z | B9NK80Z | $D^2PAK$ | Tape and reel |

# Contents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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 800 | V |
| $V_{GS}$ | Gate- source voltage | ± 30 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 5.2 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 3.3 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 20.8 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25°C | 125 | W |
| | Derating factor | 1 | W/°C |
| ESD | Gate-source human body model (C = 100 pF, R = 1.5 kΩ) | 4 | kV |
| dv/dt (2) | Peak diode recovery voltage slope | 4.5 | V/ns |
| $T_j$<br>$T_{stg}$ | Max operating junction temperature<br>Storage temperature | -55 to 150 | °C |

1. Pulse width limited by junction temperature.
2. $I_{SD} \leq$ 5.2 A, di/dt $\leq$ 200 A/µs, $V_{DD} \leq V_{(BR)DSS}$

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 1 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 62.5 | °C/W |

**Table 4. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not-repetitive<br>(pulse width limited by Tj Max) | 5.2 | A |
| $E_{AS}$ | Single pulse avalanche energy<br>(starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 210 | mJ |

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified)

**Table 5. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown voltage | $I_D$ =1 mA, $V_{GS}$ = 0 | 800 | | | V |
| $I_{DSS}$ | Zero gate voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = 800 V<br>$V_{DS}$ = 800 V, $T_C$ = 125 °C | | | 1<br>50 | µA<br>µA |
| $I_{GSS}$ | Gate-body leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20 V | | | ± 10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 100 µA | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$ = 10 V, $I_D$ = 2.6 A | | 1.5 | 1.8 | Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DS}$ = 15 V, $I_D$ = 2.6 A | - | 5 | - | S |
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 | - | 1138 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 122 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 25 | - | pF |
| $C_{oss\ eq.}$ (2) | Equivalent output capacitance | $V_{DS}$ =0 , $V_{DS}$ = 0 to 640 V | - | 50 | - | pF |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 400 V, $I_D$ = 2.6 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 15*) | - | 20 | - | ns |
| $t_r$ | Rise time | | - | 12 | - | ns |
| $t_{r(off)}$ | Turn-off delay time | | - | 45 | - | ns |
| $t_r$ | Fall time | | - | 22 | - | ns |
| $Q_g$ | Total gate charge | $V_{DD}$ = 640 V, $I_D$ = 2.6 A, $V_{GS}$ = 10 V (see *Figure 16*) | - | 40 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 7 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 2.1 | - | nC |
| $t_{r(Voff)}$ | Off-voltage rise time | $V_{DD}$ = 640 V, $I_D$ = 2.6 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 15*) | - | 12 | - | ns |
| $t_r$ | Fall time | | - | 10 | - | ns |
| $t_c$ | Cross-over time | | - | 20 | - | ns |

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$(1) | Source-drain current<br>Source-drain current (pulsed) | | - | | 5.2<br>20.8 | A<br>A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 5.2 A, $V_{GS}$ = 0 | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 5.2 A, di/dt = 100 A/µs<br>$V_{DD}$ = 50 V, Tj = 150°C<br>(see *Figure 20*) | - | 530 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 3.31 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 12.5 | | A |

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. Pulse width limited by safe operating area

**Table 8. Gate-source zener diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)\ GSO}$ | Gate-source breakdown voltage | $I_D$= 0<br>$I_{GS}$= ± 1mA | 30 | | | V |

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device’s ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device’s integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

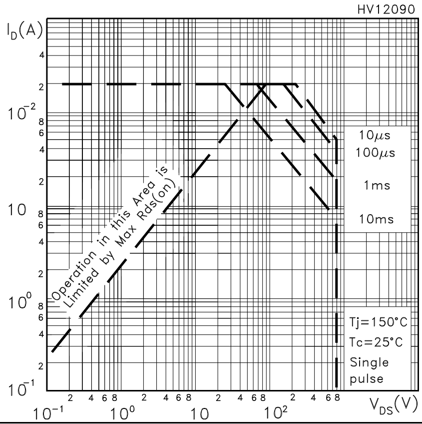



**Figure 3. Thermal impedance**

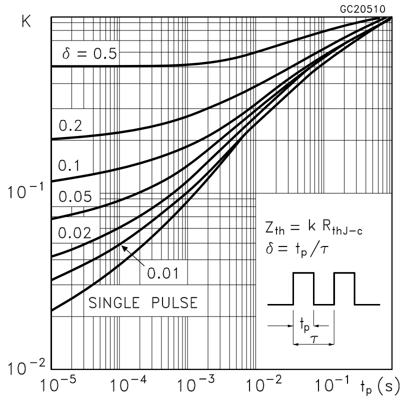



**Figure 4. Output characteristics**

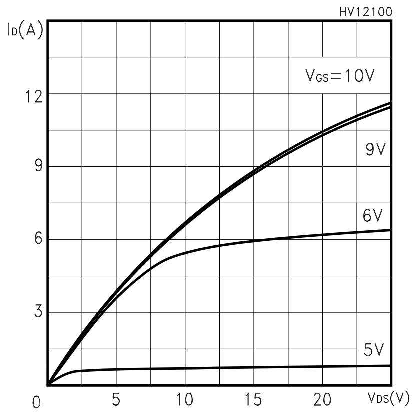



**Figure 5. Transfer characteristics**

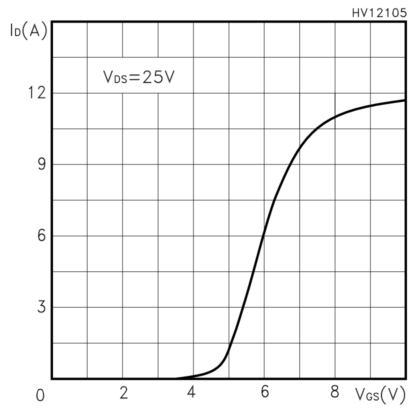



**Figure 6. Transconductance**

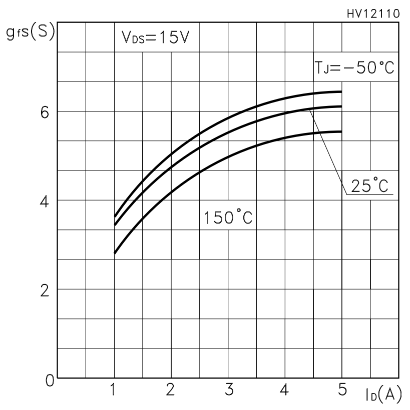



**Figure 7. Static drain-source on-resistance**

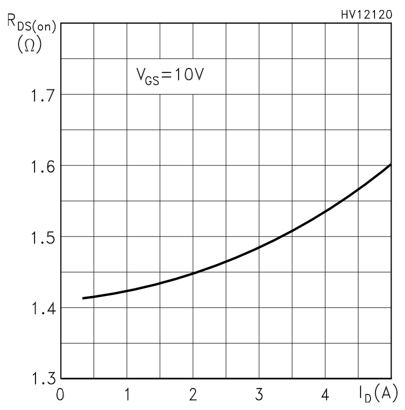


**Figure 8. Gate charge vs gate-source voltage**

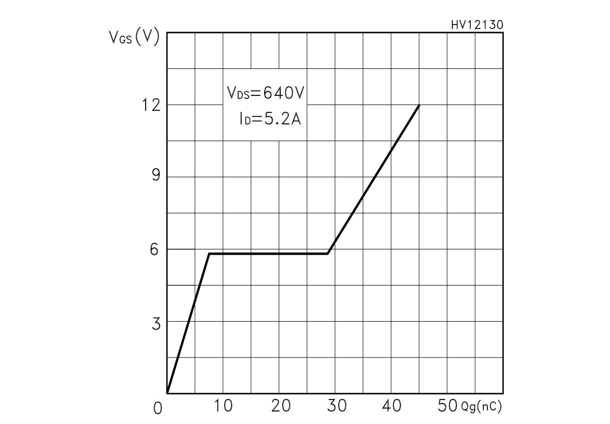



**Figure 9. Capacitance variations**

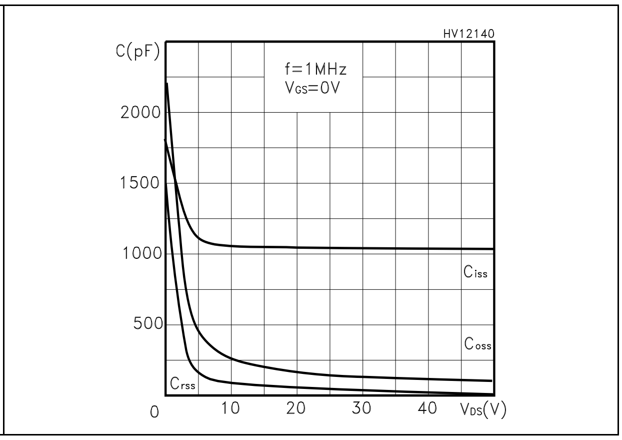



**Figure 10. Normalized gate threshold voltage vs temperature**

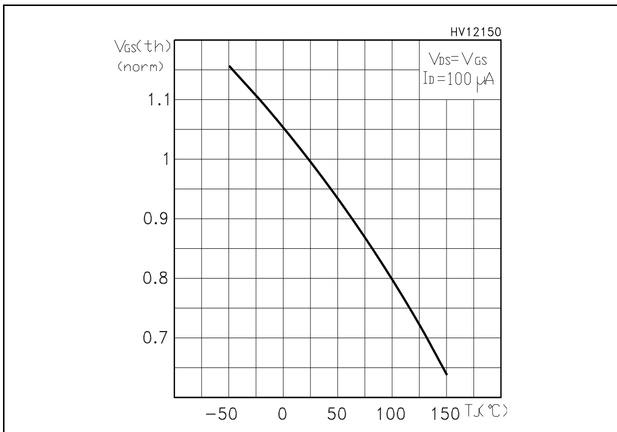



**Figure 11. Normalized on-resistance vs temperature**

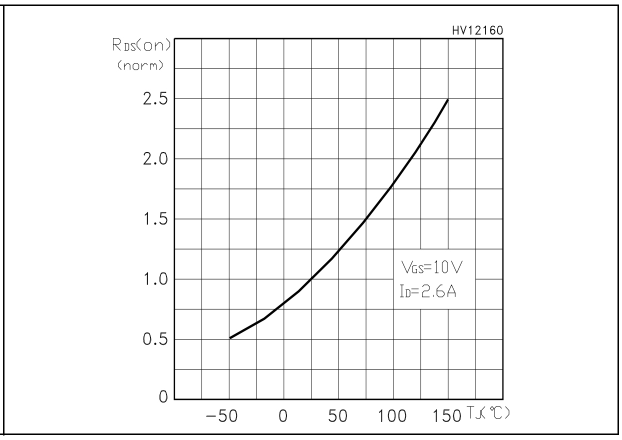



**Figure 12. Source-drain diode forward characteristic**

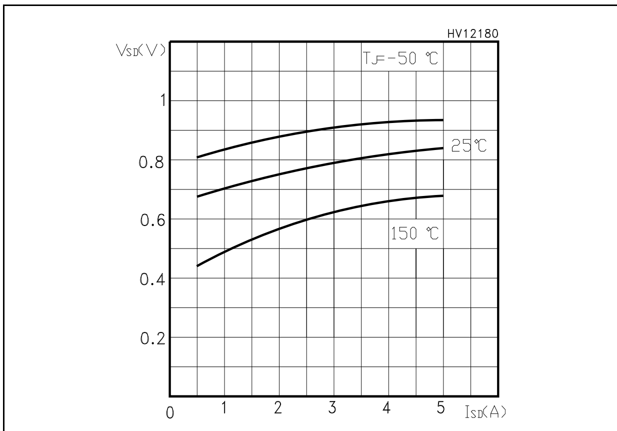



**Figure 13. Normalized BVDSS vs temperature**

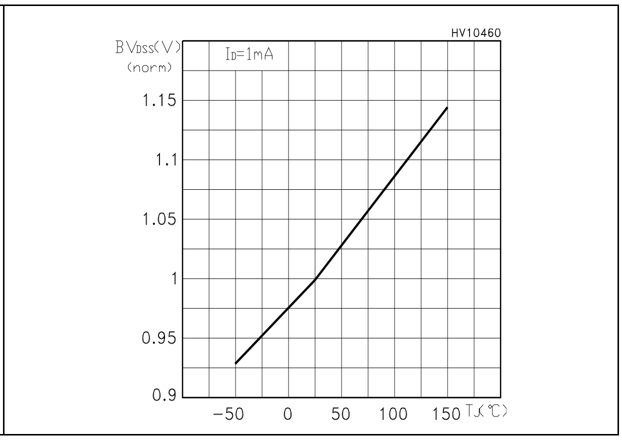
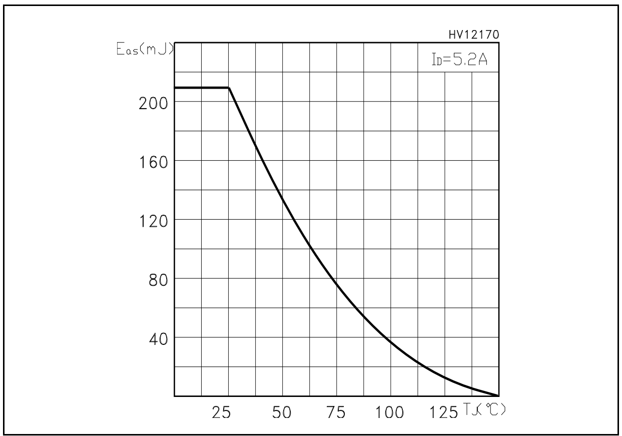


**Figure 14. Maximum avalanche energy vs temperature**



# 3 Test circuits

**Figure 15. Switching times test circuit for resistive load**

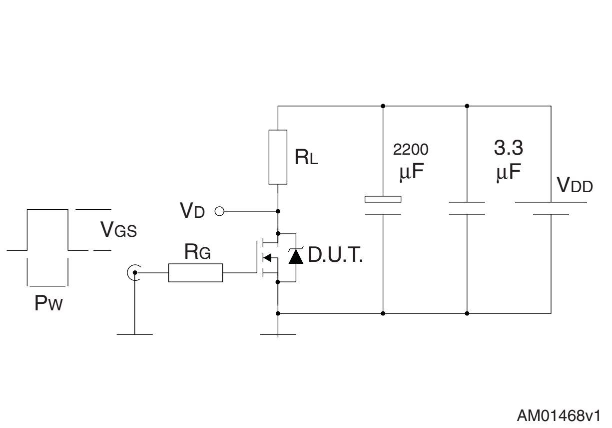



**Figure 16. Gate charge test circuit**

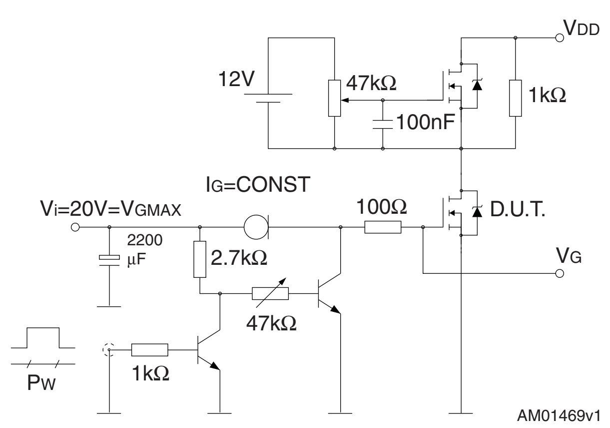



**Figure 17. Test circuit for inductive load switching and diode recovery times**

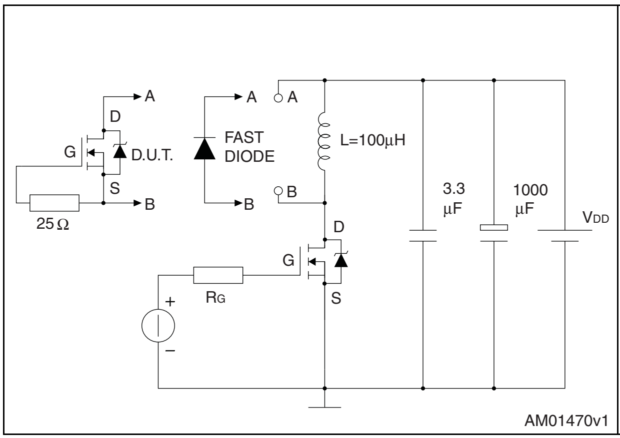



**Figure 18. Unclamped inductive load test circuit**

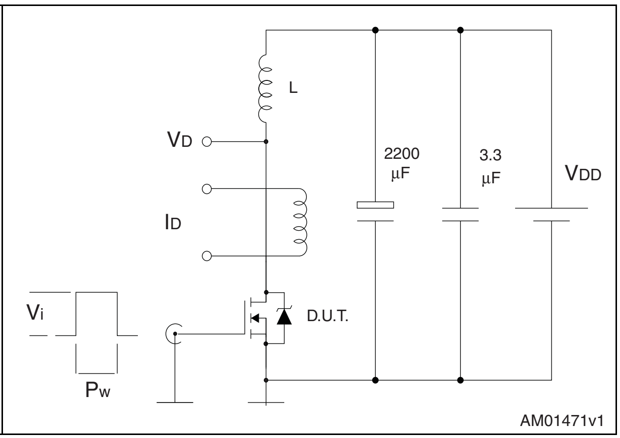



**Figure 19. Unclamped inductive waveform**

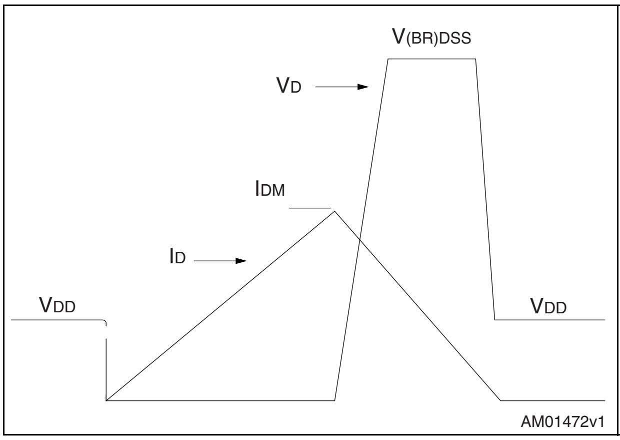
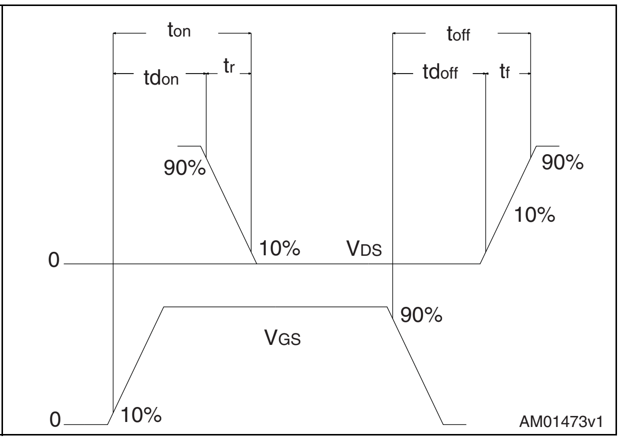



**Figure 20. Switching time waveform**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

**Table 9. D²PAK (TO-263) mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | | |
| E | 10 | | 10.40 |
| E1 | 8.50 | | |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.4 | |
| V2 | 0° | | 8° |

**Figure 21. D²PAK (TO-263) drawing**

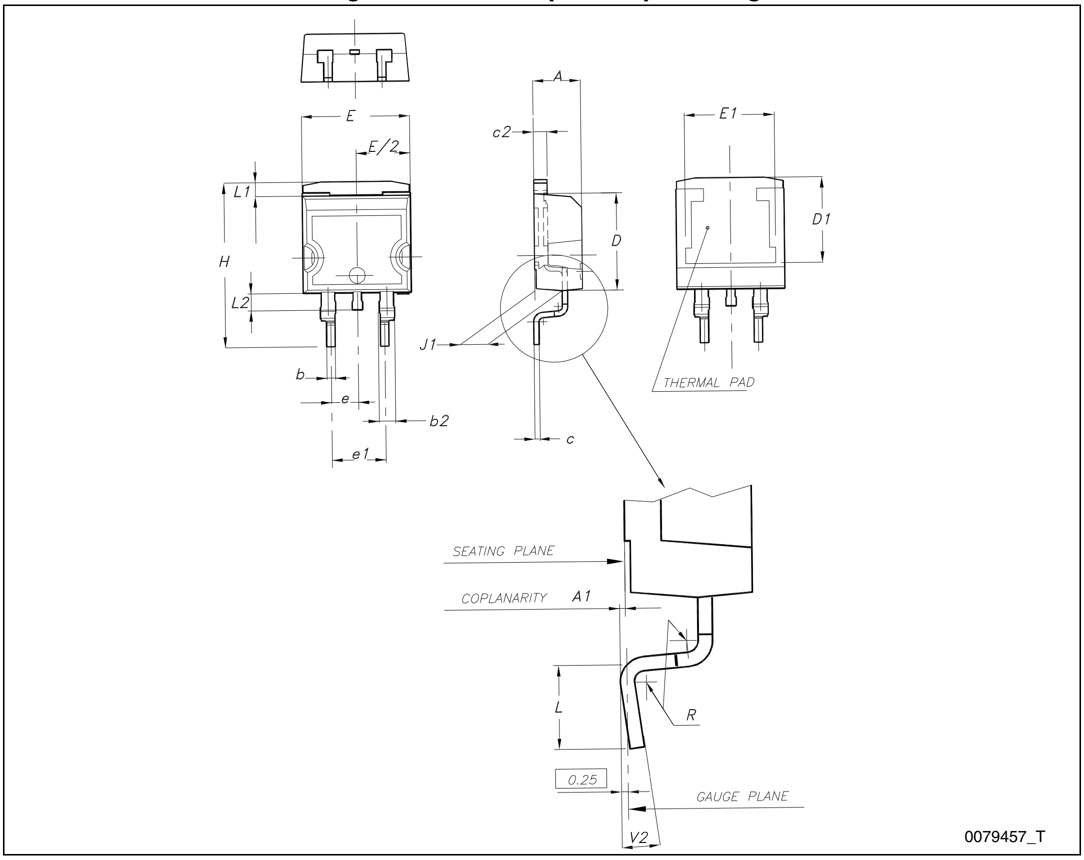
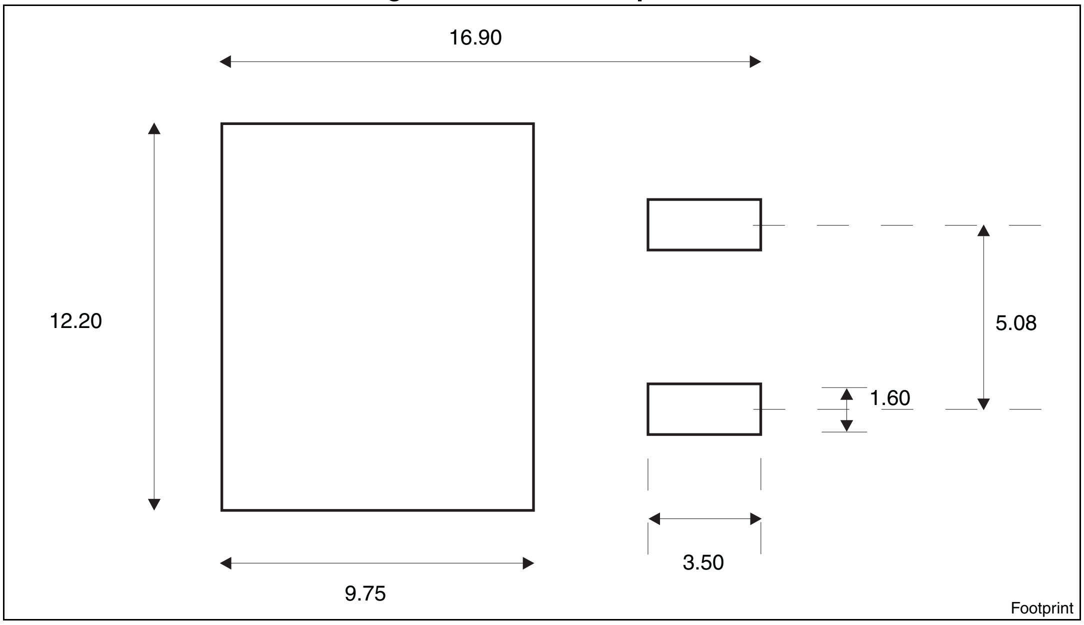



**Figure 22. D²PAK footprint[(a)]**




a. All dimension are in millimeters

# 5 Packaging mechanical data

Table 10. $D^2PAK$ (TO-263) tape and reel mechanical data

| Tape | | | Reel | | |
|---|---|---|---|---|---|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 10.5 | 10.7 | A | | 330 |
| B0 | 15.7 | 15.9 | B | 1.5 | |
| D | 1.5 | 1.6 | C | 12.8 | 13.2 |
| D1 | 1.59 | 1.61 | D | 20.2 | |
| E | 1.65 | 1.85 | G | 24.4 | 26.4 |
| F | 11.4 | 11.6 | N | 100 | |
| K0 | 4.8 | 5.0 | T | | 30.4 |
| P0 | 3.9 | 4.1 | | | |
| P1 | 11.9 | 12.1 | Base qty | | 1000 |
| P2 | 1.9 | 2.1 | Bulk qty | | 1000 |
| R | 50 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 23.7 | 24.3 | | | |

**Figure 23. Tape**

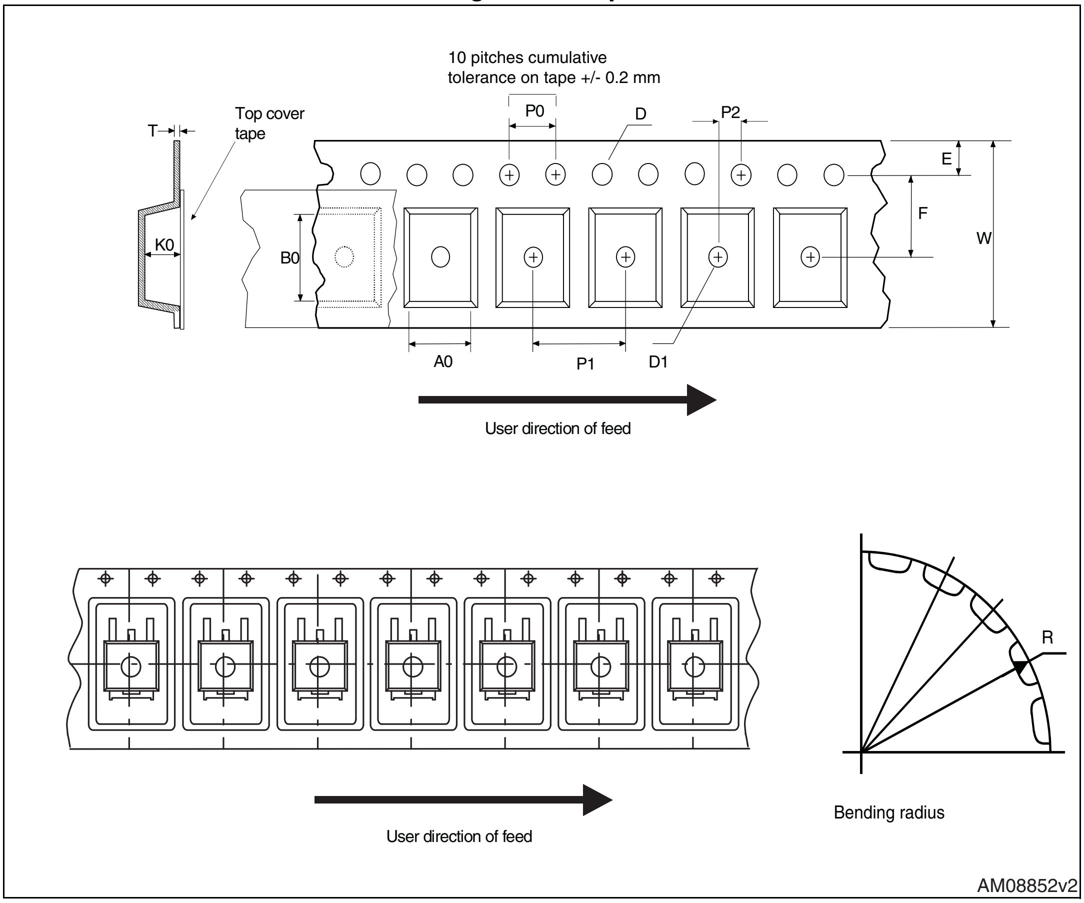
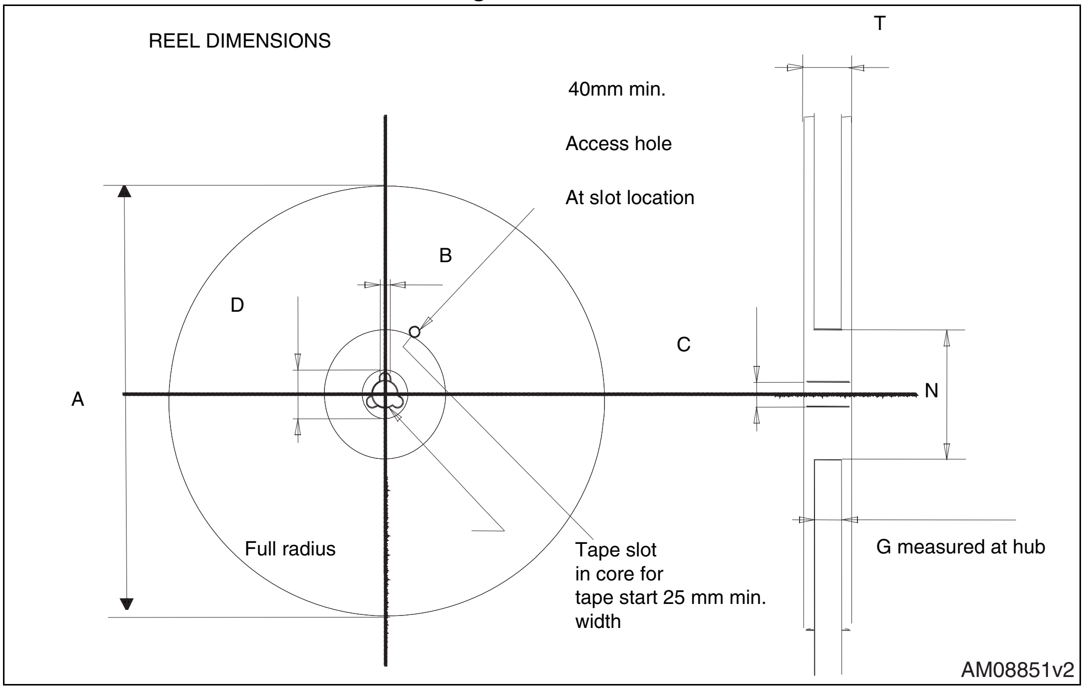



**Figure 24. Reel**



# 6 Revision history

**Table 11. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 05-Jun-2013 | 1 | First issue. |
| 12-Jul-2013 | 2 | Document status promoted from preliminary to production data. |