

## Automotive-grade N-channel 800 V, 1.5 $\Omega$ typ., 5.2 A Zener-protected SuperMESH™ Power MOSFETs in D<sup>2</sup>PAK package

Datasheet - production data

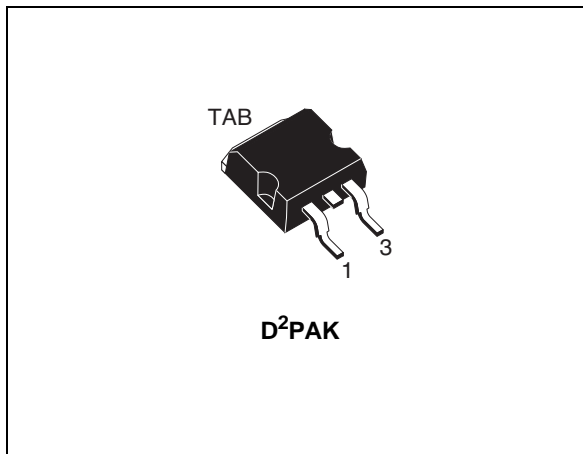
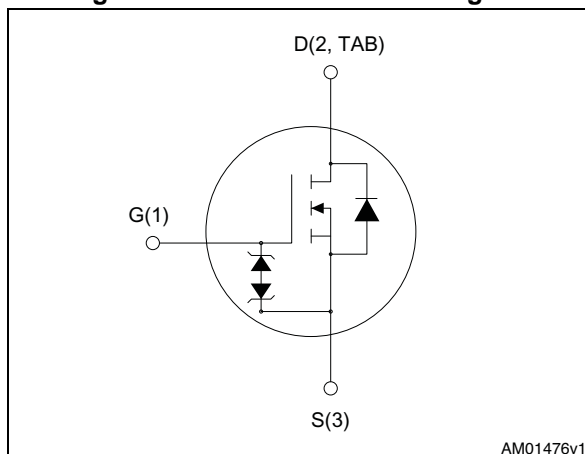


Figure 1. Internal schematic diagram



### Features

Type	V <sub>DS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB9NK80Z	800V	1.8 $\Omega$	5.2A

- Designed for automotive applications and AEC-Q101 qualified
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Zener-protected
- Very low intrinsic capacitances

### Applications

- Switching application

### Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB9NK80Z	B9NK80Z	D <sup>2</sup> PAK	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	800	V
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5.2	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	20.8	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	125	W
	Derating factor	1	W/ $^\circ\text{C}$
ESD	Gate-source human body model (C = 100 pF, R = 1.5 k $\Omega$ )	4	kV
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	4.5	V/ns
$T_j$	Max operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

1. Pulse width limited by junction temperature.
2.  $I_{SD} \leq 5.2\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ Max)	5.2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	210	mJ

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	800			V
I <sub>DSS</sub>	Zero gate voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 800 V V <sub>DS</sub> = 800 V, T <sub>C</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			± 10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.6 A		1.5	1.8	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2.6 A	-	5	-	S
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0	-	1138	-	pF
C <sub>oss</sub>	Output capacitance		-	122	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	25	-	pF
C <sub>oss eq.</sub> <sup>(2)</sup>	Equivalent output capacitance	V <sub>DS</sub> = 0, V <sub>DS</sub> = 0 to 640 V	-	50	-	pF
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 2.6 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 15</a> )	-	20	-	ns
t <sub>r</sub>	Rise time		-	12	-	ns
t <sub>r(off)</sub>	Turn-off delay time		-	45	-	ns
t <sub>f</sub>	Fall time		-	22	-	ns
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 640 V, I <sub>D</sub> = 2.6 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 16</a> )	-	40	-	nC
Q <sub>gs</sub>	Gate-source charge		-	7	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	2.1	-	nC
t <sub>r(Voff)</sub>	Off-voltage rise time	V <sub>DD</sub> = 640 V, I <sub>D</sub> = 2.6 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 15</a> )	-	12	-	ns
t <sub>f</sub>	Fall time		-	10	-	ns
t <sub>c</sub>	Cross-over time		-	20	-	ns

1. Pulsed: pulse duration=300μs, duty cycle 1.5%
2. C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		5.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5.2 \text{ A}, V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5.2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	530		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50 \text{ V}, T_J = 150^\circ\text{C}$	-	3.31		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 20</a> )	-	12.5		A

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%
2. Pulse width limited by safe operating area

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_D = 0$ $I_{GS} = \pm 1 \text{ mA}$	30			V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

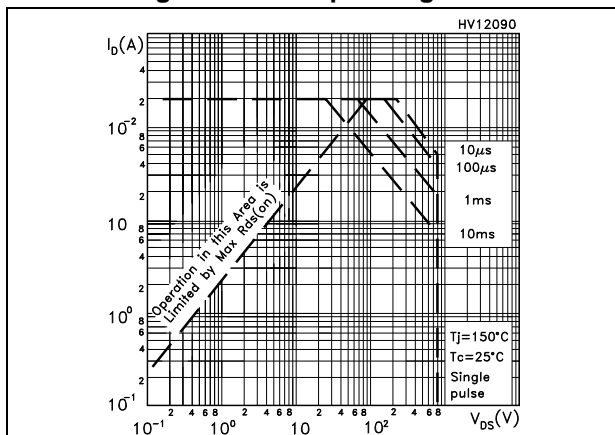


Figure 3. Thermal impedance

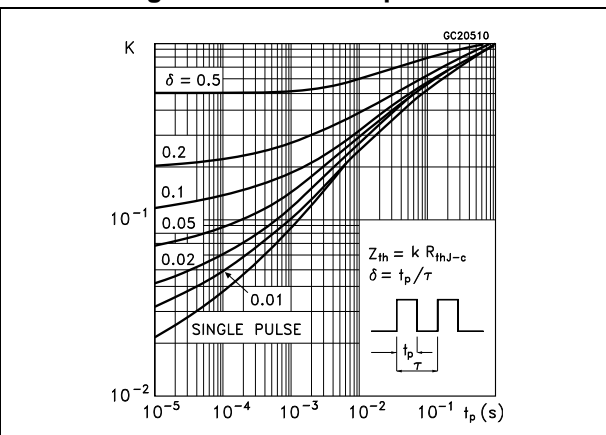


Figure 4. Output characteristics

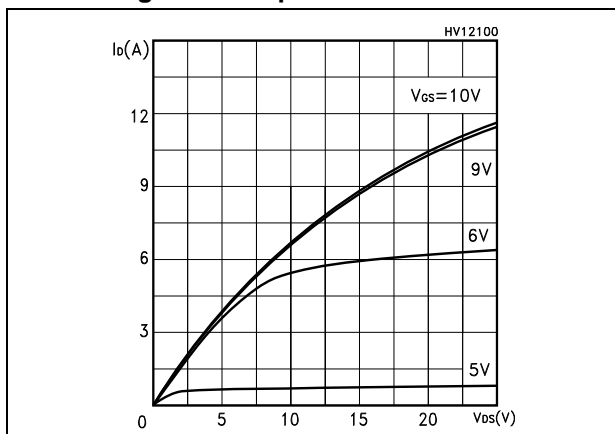


Figure 5. Transfer characteristics

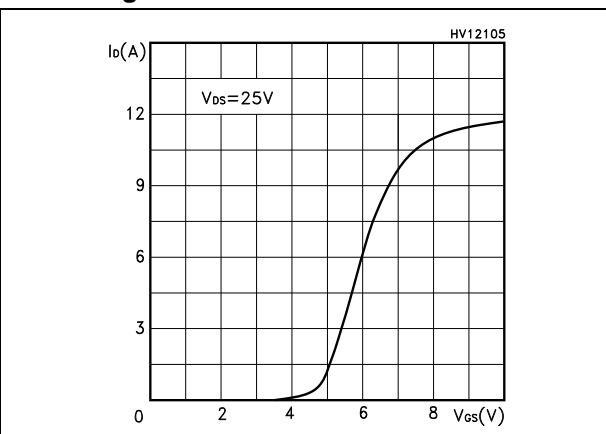


Figure 6. Transconductance

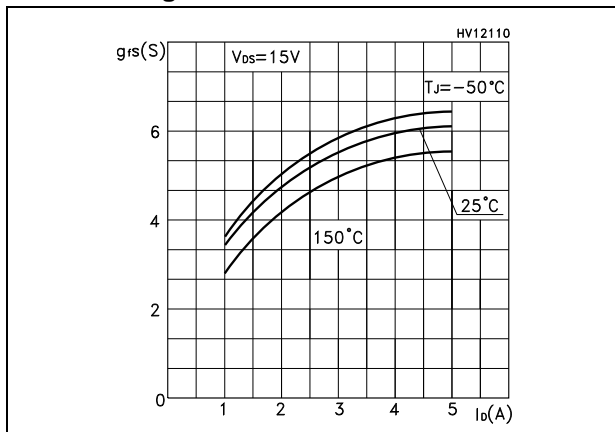


Figure 7. Static drain-source on-resistance

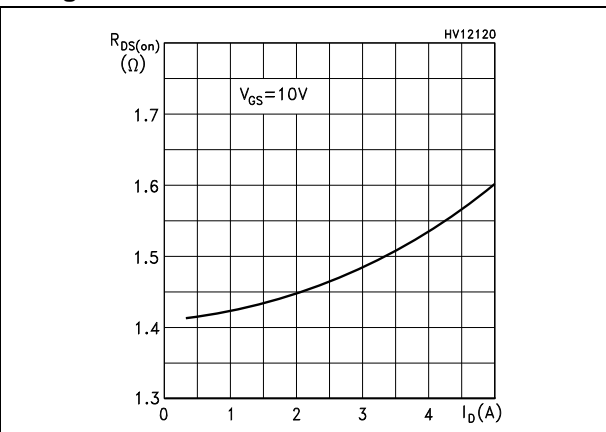


Figure 8. Gate charge vs gate-source voltage

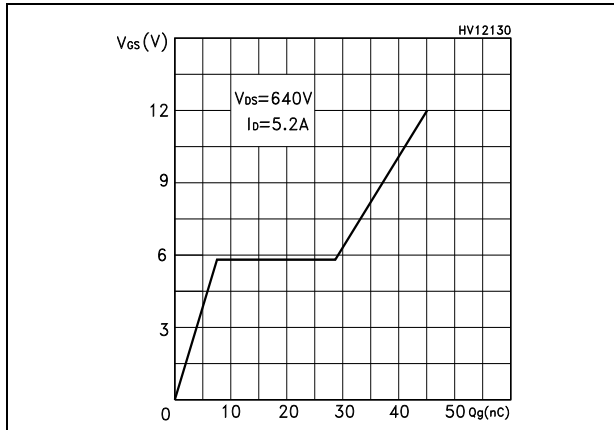


Figure 9. Capacitance variations

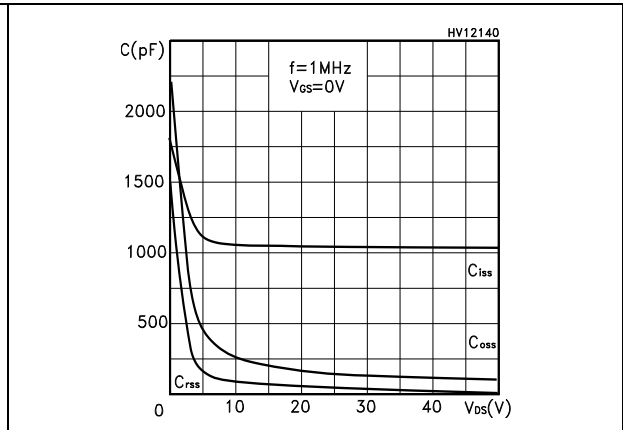


Figure 10. Normalized gate threshold voltage vs temperature

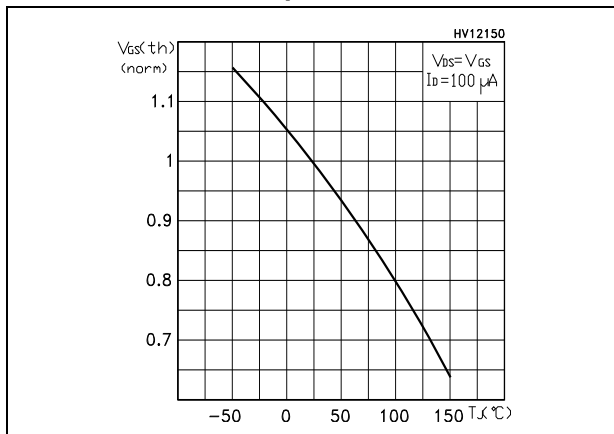


Figure 11. Normalized on-resistance vs temperature

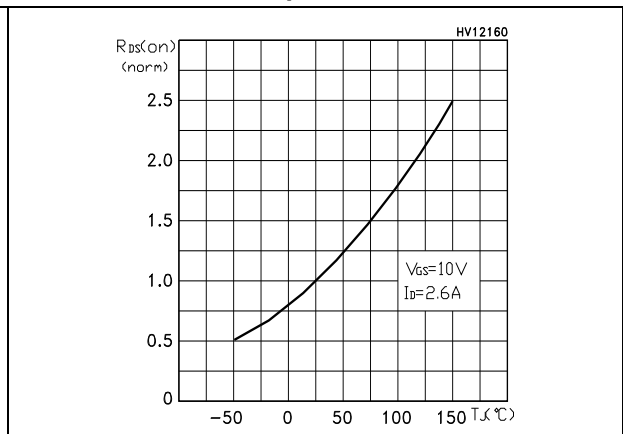


Figure 12. Source-drain diode forward characteristic

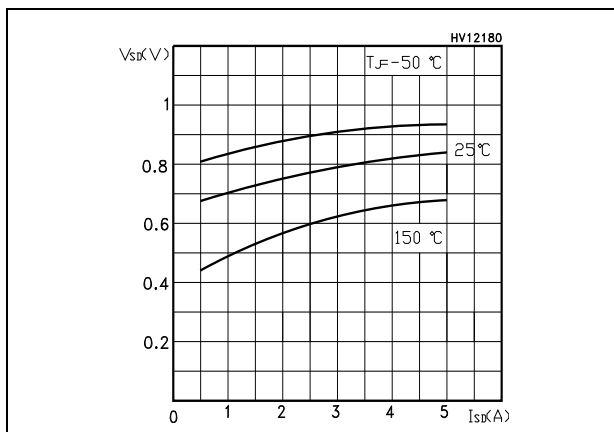


Figure 13. Normalized BVDSS vs temperature

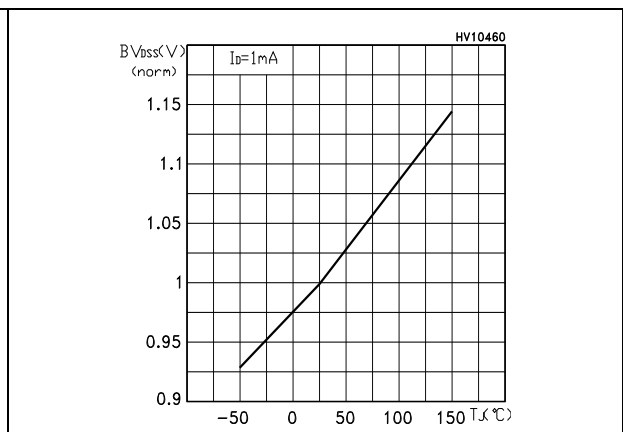
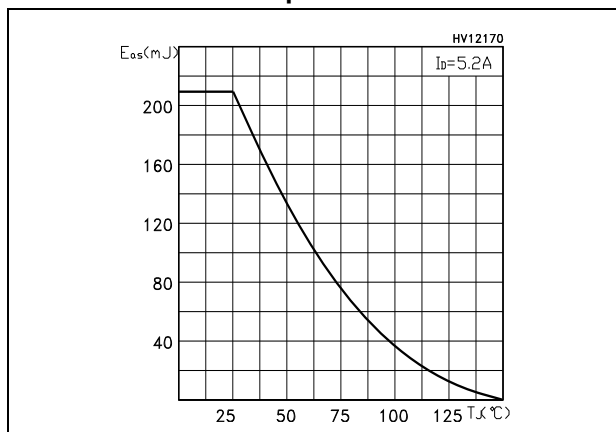


Figure 14. Maximum avalanche energy vs temperature





### 3 Test circuits

Figure 15. Switching times test circuit for resistive load



Figure 16. Gate charge test circuit



Figure 17. Test circuit for inductive load switching and diode recovery times

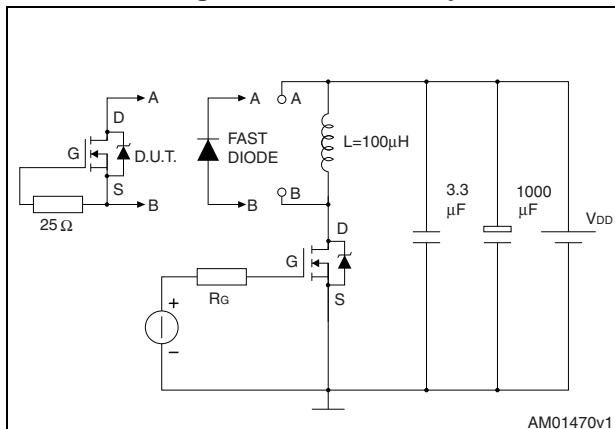


Figure 18. Unclamped inductive load test circuit



Figure 19. Unclamped inductive waveform

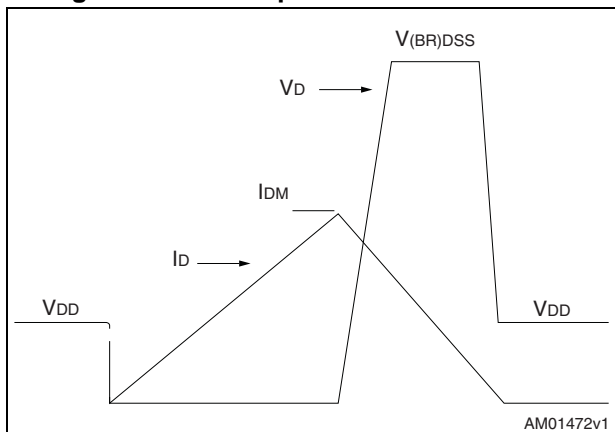
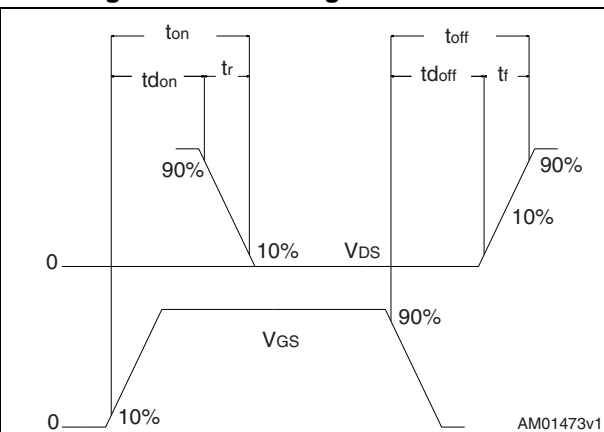


Figure 20. Switching time waveform



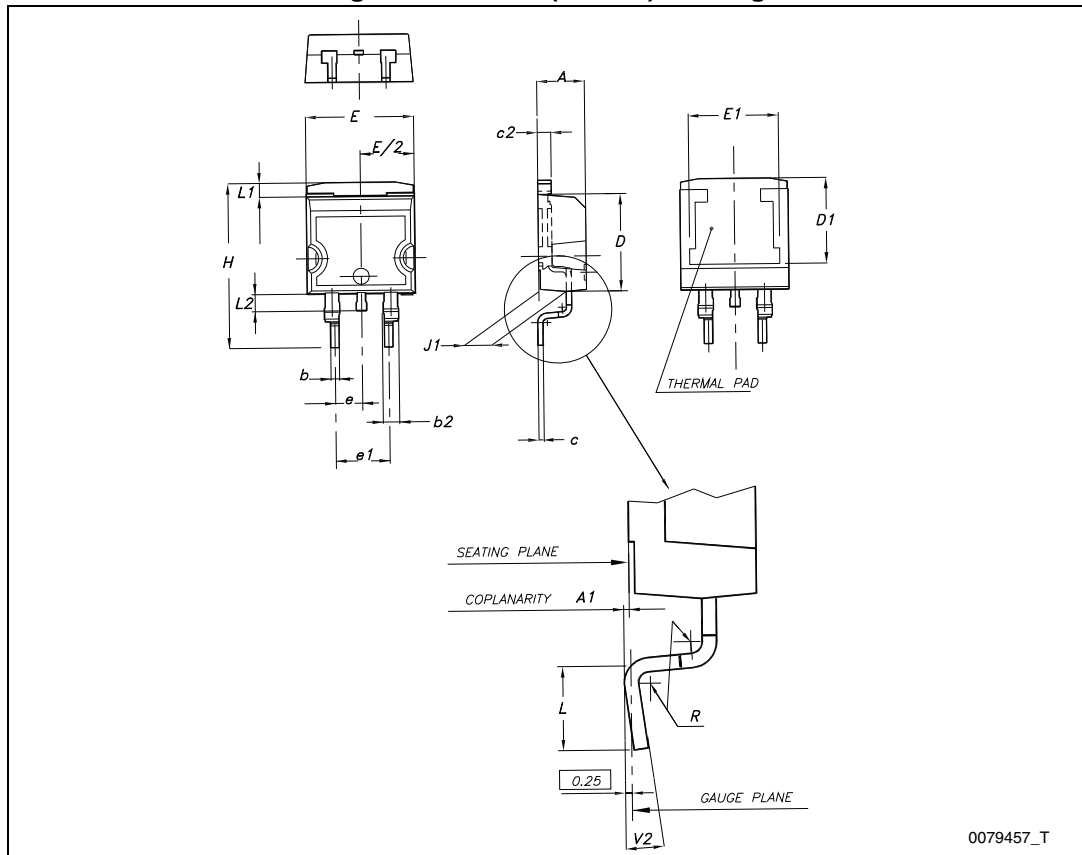
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 9. D<sup>2</sup>PAK (TO-263) mechanical data**

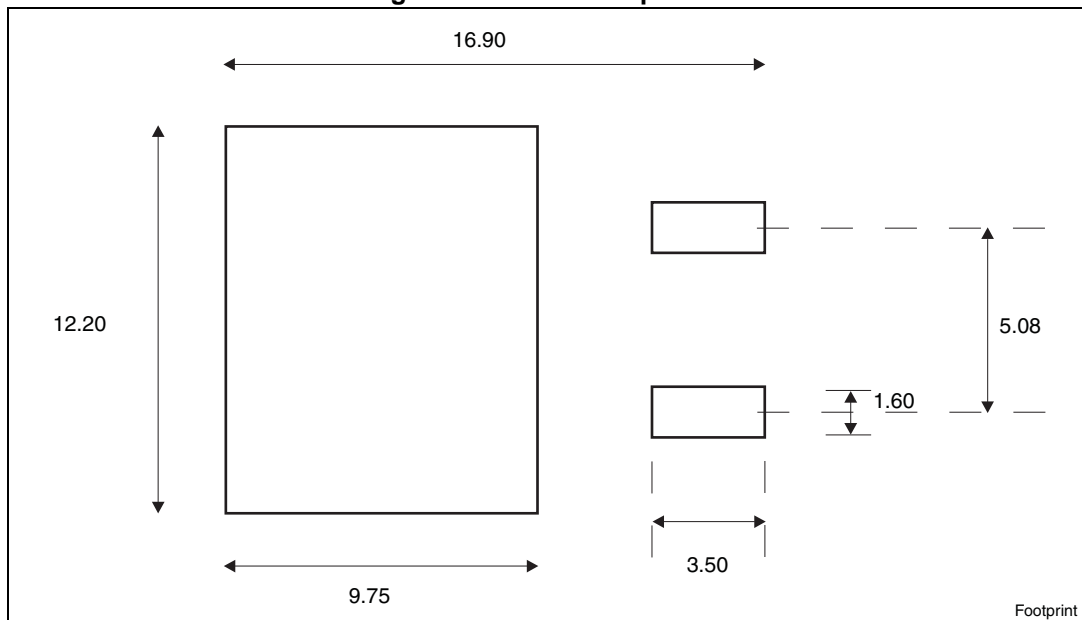
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 21. D<sup>2</sup>PAK (TO-263) drawing



0079457\_T

Figure 22. D<sup>2</sup>PAK footprint<sup>(a)</sup>



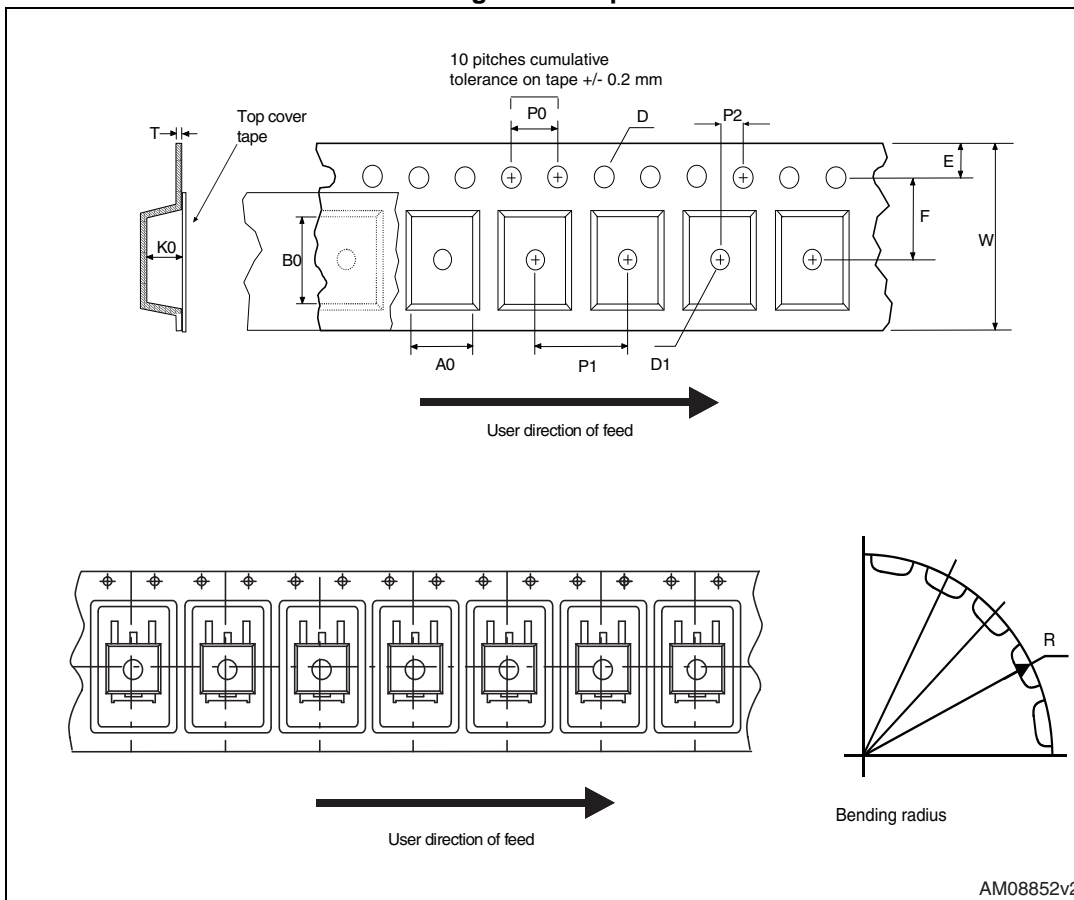
a. All dimension are in millimeters

## 5 Packaging mechanical data

Table 10. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

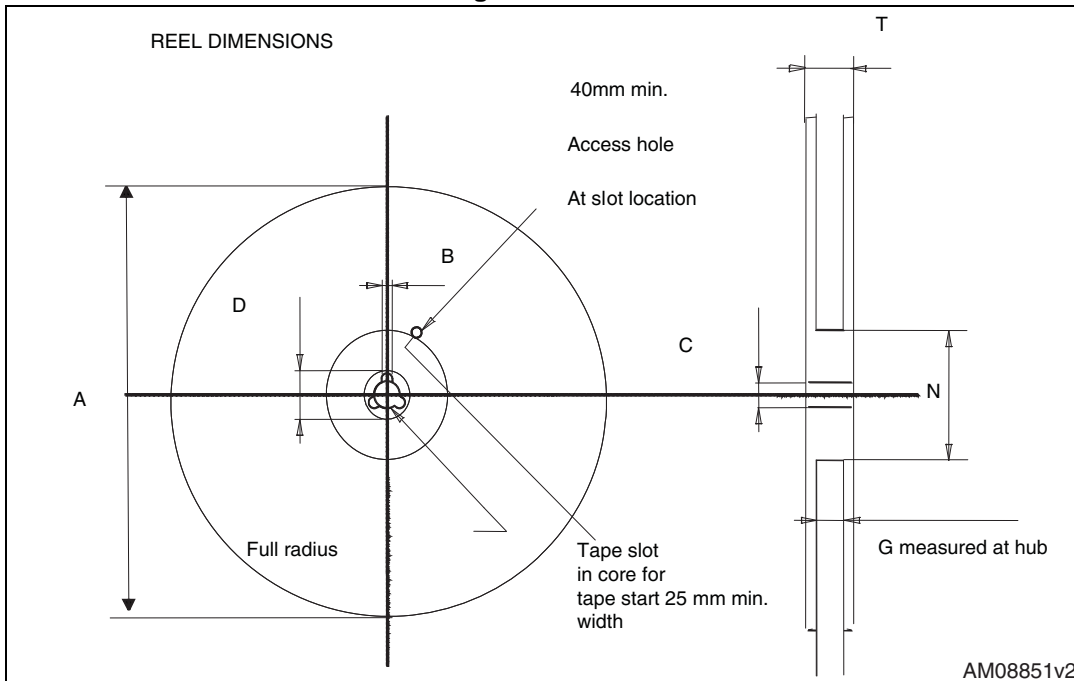
Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 23. Tape



AM08852v2

Figure 24. Reel



AM08851v2

## 6 Revision history

Table 11. Document revision history

Date	Revision	Changes
05-Jun-2013	1	First issue.
12-Jul-2013	2	Document status promoted from preliminary to production data.

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