- **Generates Clocks for Pentium™ III Class Microprocessors**
- **Supports a Single Pentium III Microprocessor**
- **Uses a 14.318 MHz Crystal Input to Generate Multiple Output Frequencies**
- **Includes Spread Spectrum Clocking (SSC), 0.34% Downspread for Reduced EMI Performance**
- **Power Management Control Terminals**
- **Low Output Skew and Jitter for Clock Distribution**
- **Operates from Dual 2.5-V and 3.3-V Supplies**
- **Generates the Following Clocks:**
  - **3 CPU (2.5 V, 100/133 MHz)**
  - **10 PCI (3.3 V, 33.3 MHz)**
  - **1 CPU/2 (2.5 V, 50/66 MHz)**
  - **1 APIC (2.5 V, 16.67 MHz)**
  - **3 3V66 (3.3 V, 66 MHz)**
  - **2 REF (3.3 V, 14.318 MHz)**
  - **1 48MHz (3.3 V, 48 MHz)**
- **Packaged in 48-Pin SSOP Package**
- **Designed for Use with TI's Direct Rambus™ Clock Generators (CDCR81, CDCR82, CDCR83)**

DL PACKAGE
(TOP VIEW)

REF0	1	48	GND
REF1	2	47	V_{DD}2.5V
V_{DD}3.3V	3	46	APIC
XIN	4	45	GND
XOUT	5	44	V_{DD}2.5V
GND	6	43	CPU_DIV2
PCI0	7	42	GND
PCI1	8	41	V_{DD}2.5V
V_{DD}3.3V	9	40	CPU2
PCI2	10	39	GND
PCI3	11	38	V_{DD}2.5V
PCI4	12	37	CPU1
PCI5	13	36	CPU0
GND	14	35	GND
PCI6	15	34	V_{DD}3.3V
PCI7	16	33	GND
V_{DD}3.3V	17	32	$\overline{\text{PWR\_DWN}}$
PCI8	18	31	$\overline{\text{SPREAD}}$
PCI9	19	30	SEL1
GND	20	29	SEL0
3V66(0)	21	28	V_{DD}3.3V
3V66(1)	22	27	48MHz
3V66(2)	23	26	GND
V_{DD}3.3V	24	25	SEL133/$\overline{\text{100}}$

description

The CDC922 is a clock synthesizer/driver that generates CPU, CPU_DIV2, 3V66, PCI, APIC, 48MHz, and REF system clock signals to support computer systems with a single Pentium III class microprocessor.

All output frequencies are generated from a 14.318-MHz crystal input. Instead of a crystal, a reference clock input can be provided at the XIN input. Two phase-locked loops (PLLs) are used to generate the host frequencies and the 48-MHz clock frequency. On-chip loop filters and internal feedback eliminate the need for external components.

The host and PCI clock outputs provide low-skew and low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected via control inputs SEL0, SEL1, and SEL133/$\overline{\text{100}}$.

The 48MHz clock can be independently disabled via the control inputs SEL0, SEL1, and SEL133/$\overline{\text{100}}$. In this state, the 48-MHz PLL is disabled and the 48MHz clock is driven to high impedance to reduce component jitter.

The outputs are either 3.3-V or 2.5-V single-ended CMOS buffers. With a logic high-level on the $\overline{\text{PWR\_DWN}}$ terminal, the device operates normally, but when a logical low-level input is applied, the device powers down completely with the outputs in a low-level output state.

description (continued)

The CPU bus can operate at 100 MHz or 133 MHz. Output frequency selection is done with corresponding setting for SEL133/$\overline{100}$ control input. The PCI bus frequency is fixed to 33 MHz.

Since the CDC922 is based on PLL circuitry, it requires a stabilization time to achieve phase lock of the PLL. This stabilization time is required after power up or after changes to the SEL inputs are made. With use of an external reference clock, this signal must be fixed-frequency and fixed-phase before the stabilization time starts.

Function Tables

SELECT FUNCTIONS

INPUTS			OUTPUTS							FUNCTION
SEL133/$\overline{100}$	SEL1	SEL0	CPU	CPU_DIV2	3V66	PCI	48MHz	REF	APIC	
L	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	3-state
L	L	H	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
L	H	L	100 MHz	50 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	48-MHz PLL off
L	H	H	100 MHz	50 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	48-MHz PLL on
H	L	L	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16	Test
H	L	H	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
H	H	L	133 MHz	66 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	48-MHz PLL off
H	H	H	133 MHz	66 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	48-MHz PLL on

ENABLE FUNCTIONS

INPUTS	OUTPUTS						INTERNAL	
$\overline{\text{PWR\_DWN}}$	CPU	CPU_DIV2	APIC	3V66	PCI	REF, 48MHz	CRYSTAL	VCOs
L	L	L	L	L	L	L	Off	Off
H	On	On	On	On	On	On	On	On

OUTPUT BUFFER SPECIFICATIONS

BUFFER NAME	V_{DD} RANGE (V)	IMPEDANCE (Ω)	BUFFER TYPE
CPU, CPU_DIV2, APIC	2.375 – 2.625	13.5 – 45	TYPE 1
48MHz, REF	3.135 – 3.465	20 – 60	TYPE 3
PCI, 3V66	3.135 – 3.465	12 – 55	TYPE 5

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3V66 [0–2]	21–23	O	3.3 V, Type 5, 66-MHz clock outputs
48MHz	27	O	3.3 V, Type 3, 48-MHz clock output
APIC	46	O	2.5 V, Type 2, APIC clock output at 16.67 MHz
CPU [0–2]	36, 37, 40	O	2.5 V, Type 1, CPU clock outputs
CPU_DIV2	43	O	2.5 V, Type 1, CPU_DIV2 clock output
GND	6, 14, 20, 26, 33, 35, 39, 42, 45, 48		Ground for PCI, 3V66, 48MHz, CPU, CPU_DIV2, APIC, REF [0–1] outputs and CORE
PCI [0–9]	7, 8, 10–13, 15, 16, 18, 19	O	3.3 V, Type 5, 33-MHz PCI clock outputs
$\overline{\text{PWR\_DWN}}$	32	I	Power down for complete device with outputs forced low
REF0, REF1	1, 2	O	3.3 V, Type 3, 14.318-MHz reference clock outputs
SEL0, SEL1	29, 30	I	LVTTL level logic select terminals for function selection
SEL133/$\overline{100}$	25	I	LVTTL level logic select terminal for enabling 100/133 MHz
$\overline{\text{SPREAD}}$	31	I	Disables SSC function
V_{DD}2.5V	38, 41, 44, 47		Power for CPU, CPU_DIV2, and APIC outputs
V_{DD}3.3V	3, 9, 17, 24, 28, 34		Power for the REF, PCI, 3V66, 48MHz outputs and CORE
XIN	4	I	Crystal input – 14.318 MHz
XOUT	5	O	Crystal output – 14.318 MHz

spread spectrum clock (SSC) implementation for CDC922

Simultaneously switching at fixed frequency generates a significant power peak at the selected frequency, which in turn will cause EMI disturbance to the environment. The purpose of the internal frequency modulation of the CPU–PLL allows to distribute the energy to many different frequencies which reduces the power peak. A typical characteristic for a single frequency spectrum and a frequency modulated spectrum is shown in Figure 1.

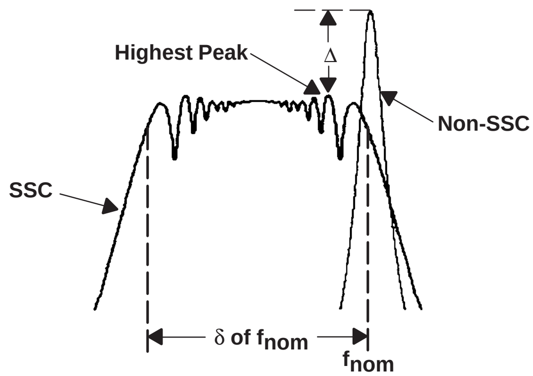


Figure 1. Frequency Power Spectrum With and Without the Use of SSC

The modulated spectrum has its distribution left hand to the single frequency spectrum which indicates a “down-spread modulation”.

The peak reduction depends on the modulation scheme and modulation profile. System performance and timing requirements are the limiting factors for actual design implementations. The implementation was driven to keep the average clock frequency closed to its upper specification limit. The modulation amount was set to approximately –0.34% (compared to –0.5% on the CDC921).

In order to allow a downstream PLL to follow the frequency modulated signal, the bandwidth of the modulation signal is limited in order to minimize SSC induced tracking skew jitter. The ideal modulation profile used for CDC922 is shown in Figure 2.

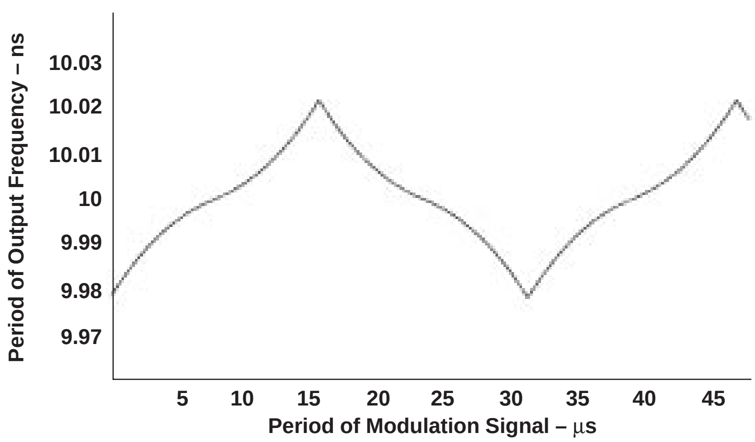
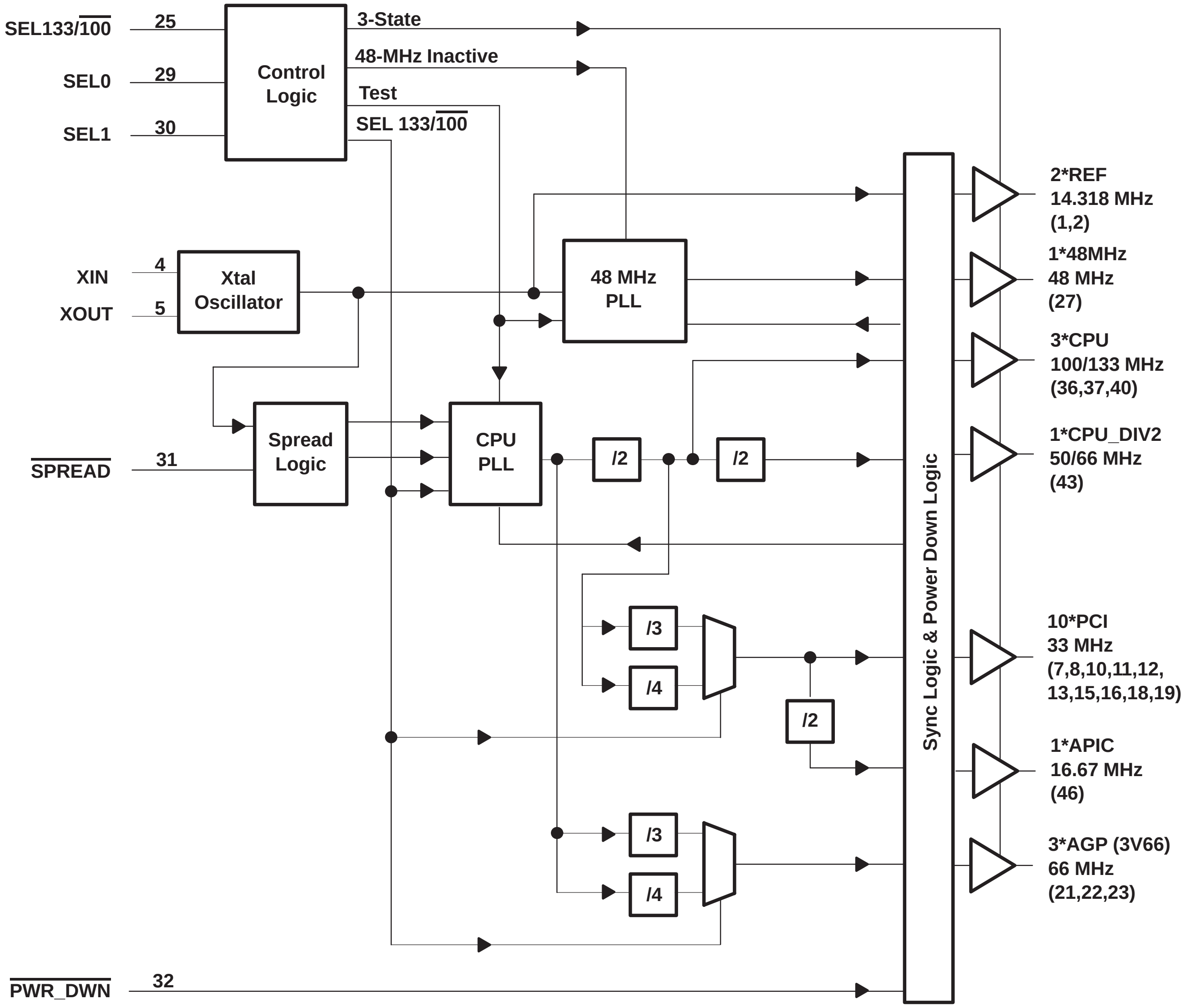


Figure 2. SSC Modulation Profile

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} .... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance state or power-off state,
V_O (see Note 1) .... –0.5 V to V_{DD} + 0.5 V
Current into any output in the low state, I_O .... 2 × I_{OL}
Input clamp current, I_{IK} (V_I < 0) .... –18 mA
Output clamp current, I_{OK} (V_O < 0) .... –50 mA
Operating free-air temperature range, T_A .... –0°C to 85°C
Storage temperature range, T_{stg} .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATNG	DERATING FACTOR† ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DL	1315.7 mW	10.53 mW/°C	842.1 mW	684.2 mW

† This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) and uses a board-mounted device at 95°C/W.

recommended operating conditions (see Note 2)

		MIN	NOM†	MAX	UNIT
Supply voltage, V_{DD}	3.3 V	3.135		3.465	V
	2.5 V	2.375		2.625	
High-level input voltage, V_{IH}		2		V_{DD} + 0.3 V	V
Low-level input voltage, V_{IL}		GND – 0.3 V		0.8	V
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	CPUx, CPU_DIV2			–12	mA
	APIC			–12	
	48MHz, REFx			–14	
	PCIx, PCI_F, 3V66x			–18	
Low-level output current, I_{OL}	CPUx, CPU_DIV2			12	mA
	APIC			12	
	48MHz, REFx			9	
	PCIx, PCI_F, 3V66x			12	
Reference frequency, $f_{(XTAL)}$‡	Test mode		130		MHz
Crystal frequency, $f_{(XTAL)}$§	Normal mode	13.8	14.318	14.8	MHz
Operating free-air temperature, T_A		0		85	°C

NOTE 2: Unused inputs must be held high or low to prevent them from floating.
† All nominal values are measured at their respective nominal V_{DD} values.
‡ Reference frequency is a test clock driven on the XIN input during the device test mode and normal mode. In test mode, XIN can be driven externally up to $f_{(XTAL)}$ = 130 MHz. If XIN is driven externally, XOUT is floating.
§ This is a series fundamental crystal with f_O = 14.31818 MHz.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{DD} = 3.135 V,	I_I = –18 mA			–1.2	V
R_I	Input resistance	XIN, XOUT	V_{DD} = 3.465 V,	V_I = V_{DD} –0.5 V	80		350	kΩ
I_{IH}	High-level input current	XOUT	V_{DD} = 3.135 V,	V_I = V_{DD} –0.5 V		20	50	mA
		$\overline{\text{SEL0, SEL1}}$, $\overline{\text{SPREAD}}$	V_{DD} = 3.465 V,	V_I = V_{DD}		<10	10	µA
		$\overline{\text{PWR\_DWN}}$	V_{DD} = 3.465 V,	V_I = V_{DD}		<10	10	µA
		SEL133/$\overline{\text{100}}$	V_{DD} = 3.465 V,	V_I = V_{DD}		<10	10	µA
I_{IL}	Low-level input current	XOUT	V_{DD} = 3.135 V,	V_I = 0 V		–2	–5	mA
		$\overline{\text{SEL0, SEL1}}$, $\overline{\text{SPREAD}}$	V_{DD} = 3.465 V,	V_I = GND		<10	–10	µA
		$\overline{\text{PWR\_DWN}}$	V_{DD} = 3.465 V,	V_I = GND		<10	–10	µA
		SEL133/$\overline{\text{100}}$	V_{DD} = 3.465 V,	V_I = GND		<10	–10	µA
I_{OZ}	High-impedance-state output current		$\lvert V_{DD}\rvert$ = max,	V_O = V_{DD} or GND			±10	µA
I_{DD}	Supply current		V_{DD} = 2.625 V, $\overline{\text{PWR\_DWN}}$ = low	All outputs = low,		<20	100	µA
			V_{DD} = 2.625 V,	All outputs = high		<20	100	µA
			V_{DD} = 3.465 V, $\overline{\text{PWR\_DWN}}$ = low	All outputs = low,		<50	200	µA
			V_{DD} = 3.465 V,	All outputs = high		12	37	mA
$I_{DD(Z)}$	High-impedance-state supply current		V_{DD} = 2.625 V				1.4	mA
			V_{DD} = 3.465 V				30	
	Dynamic I_{DD}		C_L = 20 pF, CPU = 133 MHz	V_{DD} = 3.465 V		114	156	mA
				V_{DD} = 2.625 V		44	60	
C_I	Input capacitance		V_{DD} = 3.3 V,	V_I = V_{DD} or GND	3.3		5.8	pF
	Crystal terminal capacitance		V_{DD} = 3.3 V,	V_I = 0.3 V	18	18.5	22.5	pF

† All typical values are measured at their respective nominal V_{DD} values.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

CPUx, CPU_DIV2, APIC (Type 1)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = min to max,	I_{OH} = –1 mA	VDD – 0.1 V			V
			V_{DD} = 2.375 V,	I_{OH} = –12 mA	2			
V_{OL}	Low-level output voltage		V_{DD} = min to max,	I_{OL} = 1 mA			0.1	V
			V_{DD} = 2.375 V,	I_{OL} = 12 mA		0.18	0.4	
I_{OH}	High-level output current		V_{DD} = 2.375 V,	V_O = 1 V	–26	–42		mA
			V_{DD} = 2.5 V,	V_O = 1.25 V		–46		
			V_{DD} = 2.625 V,	V_O = 2.375 V		–16	–27	
I_{OL}	Low-level output current		V_{DD} = 2.375 V,	V_O = 1.2 V	27	57		mA
			V_{DD} = 2.5 V,	V_O = 1.25 V		63		
			V_{DD} = 2.625 V,	V_O = 0.3 V		23	43	
C_O	Output capacitance		V_{DD} = 3.3 V,	V_O = V_{DD} or GND	5.8		8.5	pF
Z_O	Output impedance	High state	V_O = 0.5 V_{DD},	V_O/I_{OH}	13.5	27	45	Ω
		Low state	V_O = 0.5 V_{DD},	V_O/I_{OL}	13.5	20	45	

† All typical values are measured at their respective nominal V_{DD} values.

48MHz, REFx (Type 3)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = min to max,	I_{OH} = –1 mA	VDD – 0.1 V			V
			V_{DD} = 3.135 V,	I_{OH} = –14 mA	2.4			
V_{OL}	Low-level output voltage		V_{DD} = min to max,	I_{OL} = 1 mA			0.1	V
			V_{DD} = 3.135 V,	I_{OL} = 9 mA		0.18	0.4	
I_{OH}	High-level output current		V_{DD} = 3.135 V,	V_O = 1 V	–27	–41		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		–41		
			V_{DD} = 3.465 V,	V_O = 3.135 V		–12	–23	
I_{OL}	Low-level output current		V_{DD} = 3.135 V,	V_O = 1.95 V	29	50		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		53		
			V_{DD} = 3.465 V,	V_O = 0.4 V		20	37	
C_O	Output capacitance		V_{DD} = 3.3 V,	V_O = V_{DD} or GND	4.5		7	pF
Z_O	Output impedance	High state	V_O = 0.5 V_{DD},	V_O/I_{OH}	20	40	60	Ω
		Low state	V_O = 0.5 V_{DD},	V_O/I_{OL}	20	31	60	

† All typical values are measured at their respective nominal V_{DD} values.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PCIx, 3V66x (Type 5)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = min to max,	I_{OH} = –1 mA	VDD – 0.1 V			V
			V_{DD} = 3.135 V,	I_{OH} = –18 mA	2.4			
V_{OL}	Low-level output voltage		V_{DD} = min to max,	I_{OL} = 1 mA			0.1	V
			V_{DD} = 3.135 V,	I_{OL} = 12 mA		0.15	0.4	
I_{OH}	High-level output current		V_{DD} = 3.135 V,	V_O = 1 V	–33	–53		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		–53		
			V_{DD} = 3.465 V,	V_O = 3.135 V		–16	–33	
I_{OL}	Low-level output current		V_{DD} = 3.135 V,	V_O = 1.95 V	30	67		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		70		
			V_{DD} = 3.465 V,	V_O = 0.4 V		27	49	
C_O	Output capacitance		V_{DD} = 3.3 V,	V_O = V_{DD} or GND	4.5		7.5	pF
Z_O	Output impedance	High state	V_O = 0.5 V_{DD},	V_O/I_{OH}	12	31	55	Ω
		Low state	V_O = 0.5 V_{DD},	V_O/I_{OL}	12	24	55	

† All typical values are measured at their respective nominal V_{DD} values.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Overshoot/undershoot		GND – 0.7 V		V_{DD} + 0.7 V	V
	Ring back		V_{IL} – 0.1 V		V_{IH} + 0.1 V	V
	Stabilization time, $\overline{\text{PWR\_DWN}}$ to PCIx	$f_{(CPU)}$ = 133 MHz		0.05	3	ms
t_{dis3}	Disable time, $\overline{\text{PWR\_DWN}}$ to PCIx	$f_{(CPU)}$ = 133 MHz		50		ns
	Stabilization time, $\overline{\text{PWR\_DWN}}$ to CPUx	$f_{(CPU)}$ = 133 MHz		0.03	3	ms
t_{dis4}	Disable time, $\overline{\text{PWR\_DWN}}$ to CPUx	$f_{(CPU)}$ = 133 MHz		50		ns
	Stabilization time†	After SEL1, SEL0			3	ms
		After power up			3	

† Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at X1. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics tables are not applicable. Stabilization time is defined as the time from when V_{DD} achieves its nominal operating level until the output frequency is stable and operating within specification.

switching characteristics, V_{DD} = 2.375 V to 2.625 V, T_A = 0°C to 85°C (continued)

CPUx

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/$\overline{100}$	CPUx	$f_{(CPU)}$ = 100 or 133MHz		6	10	ns
t_{dis1}	Output disable time	SEL133/$\overline{100}$	CPUx	$f_{(CPU)}$ = 100 or 133MHz		8	10	ns
t_c	CPU clock period†			$f_{(CPU)}$ = 100 MHz	10	10.04	10.2	ns
				$f_{(CPU)}$ = 133 MHz	7.5	7.53	7.7	ns
	Cycle to cycle jitter			$f_{(CPU)}$ = 100 or 133MHz			250	ps
	Duty cycle			$f_{(CPU)}$ = 100 or 133MHz	45		55	%
$t_{sk(o)}$	CPU bus skew	CPUx	CPUx	$f_{(CPU)}$ = 100 or 133MHz		50	175	ps
$t_{sk(p)}$	CPU pulse skew	CPUn	CPUn	$f_{(CPU)}$ = 100 or 133MHz			2.2	ns
$t_{(off)}$	CPU clock to APIC clock offset, rising edge				1.5	2.8	4	ns
$t_{(off)}$	CPU clock to 3V66 clock offset, rising edge				0	0.75	1.5	ns
t_{w1}	Pulse duration width, high			$f_{(CPU)}$ = 100 MHz	2.6	4.3		ns
				$f_{(CPU)}$ = 133 MHz	1.4	3.7		
t_{w2}	Pulse duration width, low			$f_{(CPU)}$ = 100 MHz	2.8	4.3		ns
				$f_{(CPU)}$ = 133 MHz	1.7	4		
t_r	Rise time			V_O = 0.4 V to 2.0 V	0.4	1.5	2.2	ns
t_f	Fall time			V_O = 0.4 V to 2.0 V	0.4	1.4	2	ns

† The average over any 1-µs period of time is greater than the minimum specified period.

CPU_DIV2

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/$\overline{100}$	CPU_DIV2	$f_{(CPU)}$ = 100 or 133MHz		6	10	ns
t_{dis1}	Output disable time	SEL133/$\overline{100}$	CPU_DIV2	$f_{(CPU)}$ = 100 or 133MHz		8	10	ns
t_c	CPU_DIV2 clock period†			$f_{(CPU)}$ = 100 MHz	20	20.08	20.4	ns
				$f_{(CPU)}$ = 133 MHz	15	15.06	15.3	ns
	Cycle to cycle jitter			$f_{(CPU)}$ = 100 or 133MHz			250	ps
	Duty cycle			$f_{(CPU)}$ = 100 or 133MHz	45		55	%
$t_{sk(p)}$	CPU_DIV2 pulse skew			$f_{(CPU)}$ = 100 or 133MHz			1.6	ns
t_{w1}	Pulse duration width, high			$f_{(CPU)}$ = 100 MHz	7.1			ns
				$f_{(CPU)}$ = 133 MHz	4.7			
t_{w2}	Pulse duration width, low			$f_{(CPU)}$ = 100 MHz	7.3	8.9		ns
				$f_{(CPU)}$ = 133 MHz	5	6.6		
t_r	Rise time			V_O = 0.4 V to 2.0 V	0.4	1.4	2	ns
t_f	Fall time			V_O = 0.4 V to 2.0 V	0.4	1.3	1.8	ns

† The average over any 1-µs period of time is greater than the minimum specified period.

switching characteristics, V_{DD} = 2.375 V to 2.625 V, T_A = 0°C to 85°C (continued)

APIC

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/$\overline{100}$	APIC	$f_{(APIC)}$ = 16.67 MHz		6	10	ns
t_{dis1}	Output disable time	SEL133/$\overline{100}$	APIC	$f_{(APIC)}$ = 16.67 MHz		8	10	ns
t_c	APIC clock period†			$f_{(APIC)}$ = 16.67 MHz	60	60.24	60.6	ns
	Cycle to cycle jitter			$f_{(CPU)}$ = 100 or 133 MHz			400	ps
	Duty cycle			$f_{(APIC)}$ = 16.67 MHz	45		55	%
$t_{sk(p)}$	APIC pulse skew			$f_{(APIC)}$ = 16.67 MHz			3	ns
$t_{(off)}$	APIC clock to CPU clock offset, rising edge	APIC	CPUx		–1.5		–4	ns
t_{w1}	Pulse duration width, high			$f_{(APIC)}$ = 16.67 MHz	25.5	28		ns
t_{w2}	Pulse duration width, low			$f_{(APIC)}$ = 16.67 MHz	25.3	29.2		ns
t_r	Rise time			V_O = 0.4 V to 2 V	0.4	1.6	2.1	ns
t_f	Fall time			V_O = 0.4 V to 2 V	0.4	1.2	1.7	ns

† The average over any 1-µs period of time is greater than the minimum specified period.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C

3V66

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/$\overline{100}$	3V66x	$f_{(3V66)}$ = 66 MHz		6	10	ns
t_{dis1}	Output disable time	SEL133/$\overline{100}$	3V66x	$f_{(3V66)}$ = 66 MHz		8	10	ns
t_c	3V66 clock period†			$f_{(3V66)}$ = 66 MHz	15	15.06	15.3	ns
	Cycle to cycle jitter			$f_{(CPU)}$ = 100 or 133 MHz			400	ps
	Duty cycle			$f_{(3V66)}$ = 66 MHz	45		55	%
$t_{sk(o)}$	3V66 bus skew	3V66x	3V66x	$f_{(3V66)}$ = 66 MHz		50	150	ps
$t_{sk(p)}$	3V66 pulse skew	3V66n	3V66n	$f_{(3V66)}$ = 66 MHz			2.6	ns
$t_{(off)}$	3V66 clock to CPU clock offset	3V66x	CPUx		0	–0.75	–1.5	ns
$t_{(off)}$	3V66 clock to PCI clock offset, rising edge				1.2	2.1	3	ns
t_{w1}	Pulse duration width, high			$f_{(3V66)}$ = 66 MHz	5.2			ns
t_{w2}	Pulse duration width, low			$f_{(3V66)}$ = 66 MHz	5			ns
t_r	Rise time			V_O = 0.4 V to 2 V	0.5	1.5	2	ns
t_f	Fall time			V_O = 0.4 V to 2 V	0.5	1.5	2	ns

† The average over any 1-µs period of time is greater than the minimum specified period.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C (continued)

48MHz

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/$\overline{100}$	48MHz	$f_{(48MHz)}$ = 48 MHz		6	10	ns
t_{dis1}	Output disable time	SEL133/$\overline{100}$	48MHz	$f_{(48MHz)}$ = 48 MHz		8	10	ns
t_c	48MHz clock period†			$f_{(48MHz)}$ = 48 MHz	20.5	20.83	21.1	ns
	Cycle to cycle jitter			$f_{(CPU)}$ = 100 or 133 MHz			500	ps
	Duty cycle			$f_{(48MHz)}$ = 48 MHz	45		55	%
$t_{sk(p)}$	48MHz pulse skew	48MHz	48MHz	$f_{(48MHz)}$ = 48 MHz			3	ns
t_{w1}	Pulse duration width, high			$f_{(48MHz)}$ = 48 MHz	7.8			ns
t_{w2}	Pulse duration width, low			$f_{(48MHz)}$ = 48 MHz	7.8			ns
t_r	Rise time			V_O = 0.4 V to 2 V	1	2.1	2.8	ns
t_f	Fall time			V_O = 0.4 V to 2 V	1	1.9	2.8	ns

† The average over any 1-µs period of time is greater than the minimum specified period.

REF

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/$\overline{100}$	REFx	$f_{(REF)}$ = 14.318 MHz		6	10	ns
t_{dis1}	Output disable time	SEL133/$\overline{100}$	REFx	$f_{(REF)}$ = 14.318 MHz		8	10	ns
t_c	REF clock period†			$f_{(REF)}$ = 14.318 MHz		69.84		ns
	Cycle to cycle jitter			$f_{(CPU)}$ = 100 or 133 MHz			700	ps
	Duty cycle			$f_{(REF)}$ = 14.318 MHz	45		55	%
$t_{sk(o)}$	REF bus skew	REFx	REFx	$f_{(REF)}$ = 14.318 MHz		150	250	ps
$t_{sk(p)}$	REF pulse skew	REFn	REFn	$f_{(REF)}$ = 14.318 MHz			2	ns
t_{w1}	Pulse duration width, high			$f_{(REF)}$ = 14.318 MHz	26.2	32.7		ns
t_{w2}	Pulse duration width, low			$f_{(REF)}$ = 14.318 MHz	26.2	31.2		ns
t_r	Rise time			V_O = 0.4 V to 2 V	1	2	2.8	ns
t_f	Fall time			V_O = 0.4 V to 2 V	1	1.9	2.8	ns

† The average over any 1-µs period of time is greater than the minimum specified period.

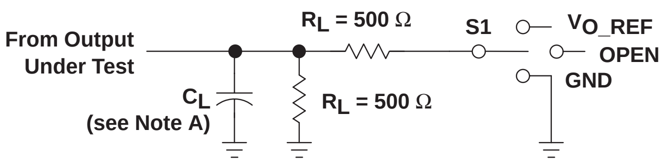
switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C (continued)

PCI

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en1}	Output enable time	SEL133/$\overline{100}$	PCIx	$f_{(PCI)}$ = 33 MHz		6	10	ns
t_{dis1}	Output disable time	SEL133/$\overline{100}$	PCIx	$f_{(PCI)}$ = 33 MHz		8	10	ns
t_c	PCIx clock period†			$f_{(PCI)}$ = 33 MHz	30	30.12	30.5	ns
	Cycle to cycle jitter			$f_{(CPU)}$ = 100 or 133 MHz			300	ps
	Duty cycle			$f_{(PCI)}$ = 33 MHz	45		55	%
$t_{sk(o)}$	PCIx bus skew	PCIx	PCIx	$f_{(PCI)}$ = 33 MHz		70	300	ps
$t_{sk(p)}$	PCIx pulse skew	PCIn	PCIn	$f_{(PCI)}$ = 33 MHz			4	ns
$t_{(off)}$	PCIx clock to 3V66 clock offset				–1.2		–3	ns
t_{w1}	Pulse duration width, high			$f_{(PCI)}$ = 33 MHz	12			ns
t_{w2}	Pulse duration width, low			$f_{(PCI)}$ = 33 MHz	12			ns
t_r	Rise time			V_O = 0.4 V to 2 V	0.5	1.6	2	ns
t_f	Fall time			V_O = 0.4 V to 2 V	0.5	1.5	2	ns

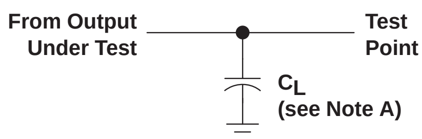
† The average over any 1-µs period of time is greater than the minimum specified period.

PARAMETER MEASUREMENT INFORMATION

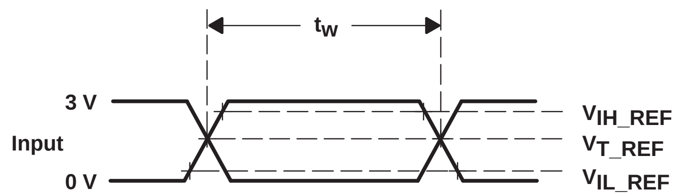


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{O_REF}
t_{PHZ}/t_{PZH}	GND

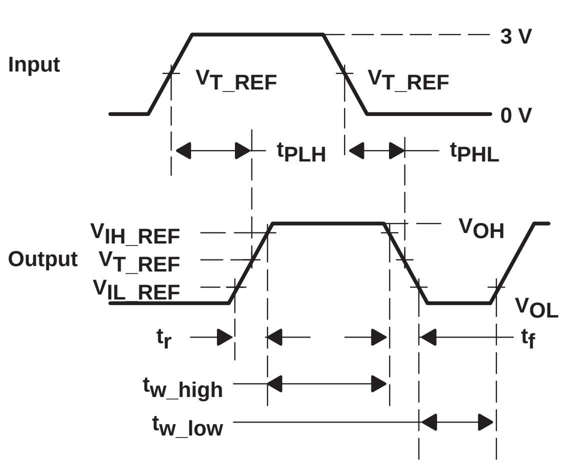
LOAD CIRCUIT for t_{pd} and t_{sk}



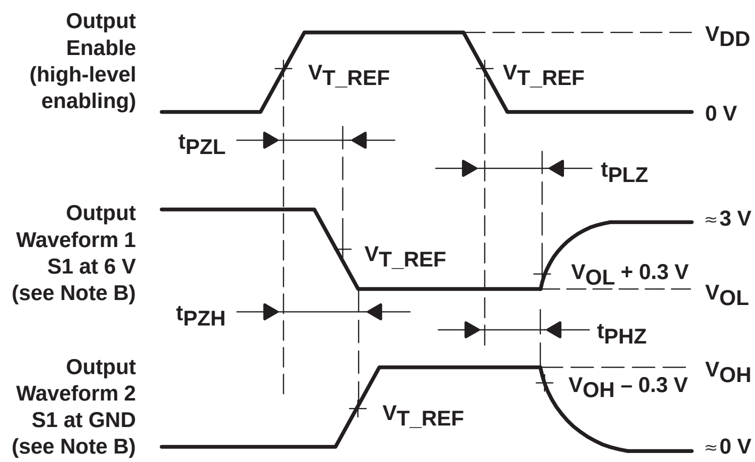
LOAD CIRCUIT FOR t_r and t_f



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



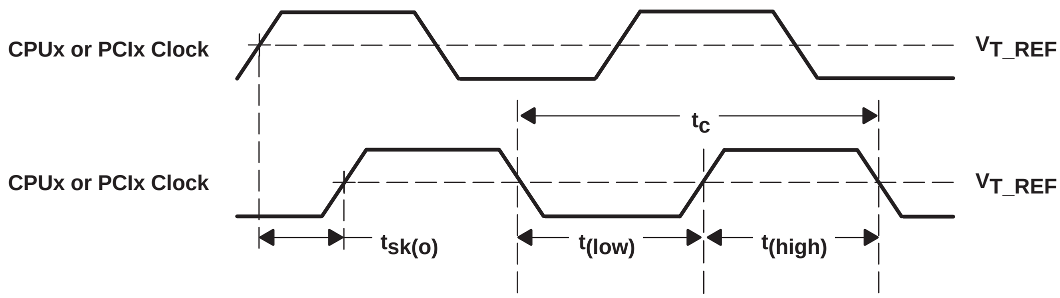
VOLTAGE WAVEFORMS

NOTES:
A. C_L includes probe and jig capacitance. C_L = 20 pF (CPUx, APIC, 48MHz, REF), C_L = 30 pF (PCIx)
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 14.318 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

PARAMETER		3.3-V INTERFACE	2.5-V INTERFACE	UNIT
V_{IH_REF}	High-level reference voltage	2.4	2	V
V_{IL_REF}	Low-level reference voltage	0.4	0.4	V
V_{T_REF}	Input Threshold reference voltage	1.5	1.25	V
V_{O_REF}	Off-state reference voltage	6	4.6	V

Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



$t_{sk(p)} = |t_{PLH} - t_{PHL}|$ Duty Cycle $= \frac{t_{(low)}}{t_c} \times 100$

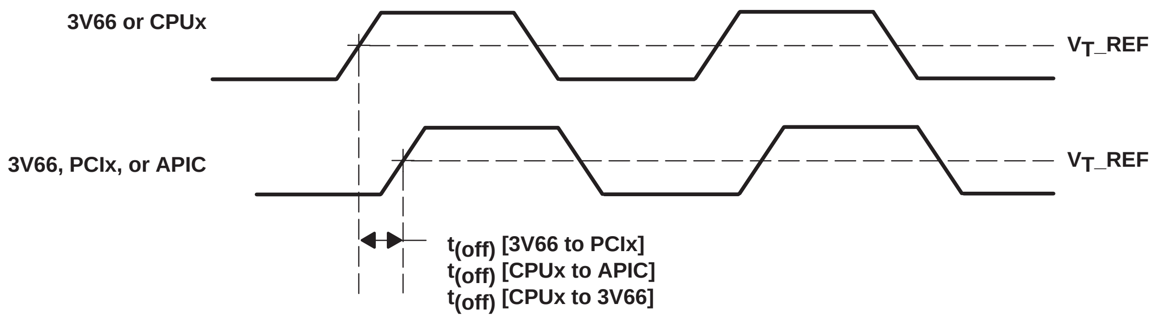
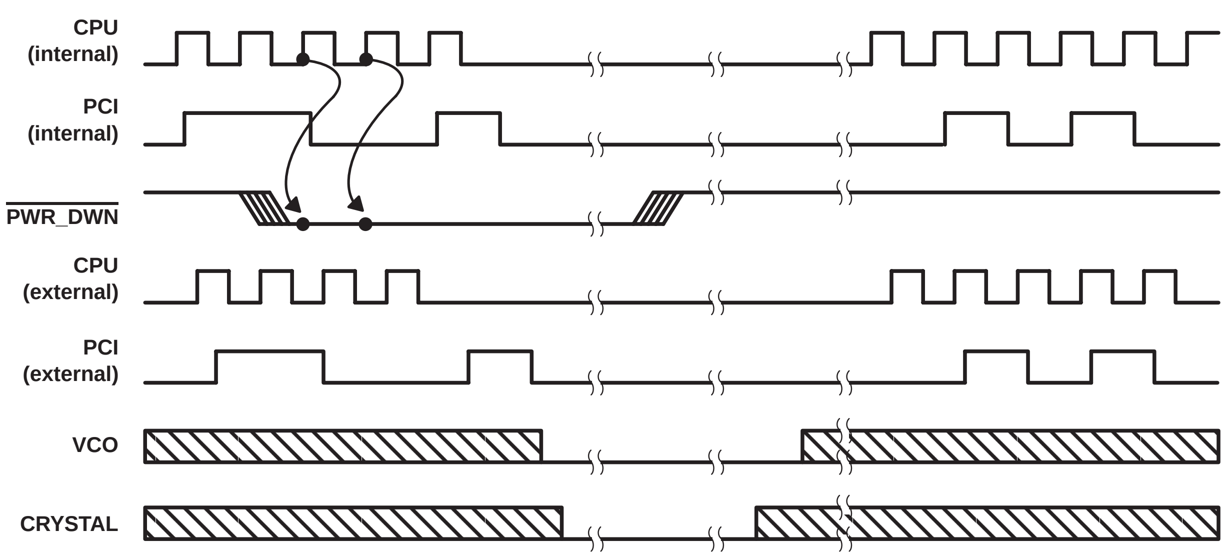


Figure 4. Waveforms for Calculation of Skew, Offset, and Jitter



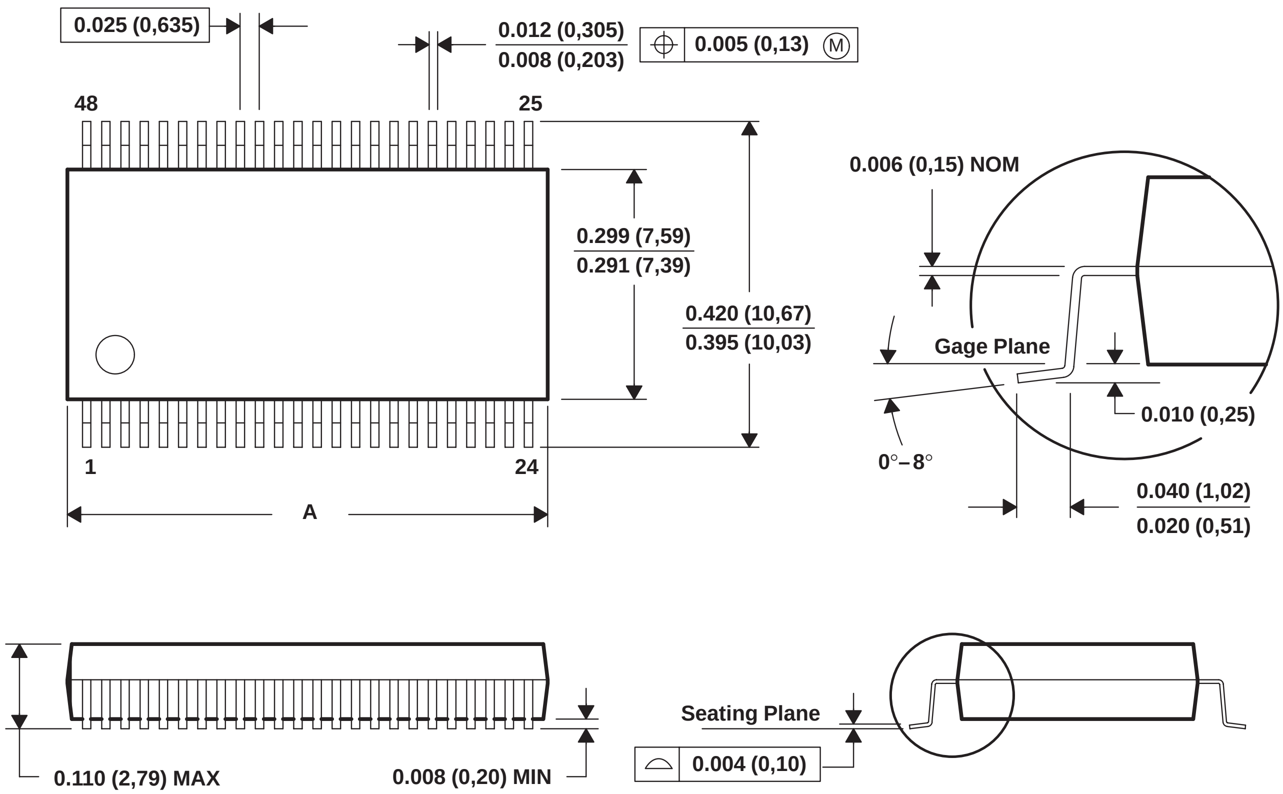
NOTE A: Shaded sections on the VCO and Crystal waveforms indicate that the VCO and crystal oscillators are active and there is a valid clock.

Figure 5. Power-Down Timing

MECHANICAL DATA

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48-PIN SHOWN



PINS ** / DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / D 08/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

IMPORTANT NOTICE