1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS design technology to combine higher speed and smaller size with the low power and high noise immunity.

On chip memory system includes 2.0 K words of ROM, and 80 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

- Fully CMOS static design
- 8-bit data bus
- On chip ROM size : 2 K words
- Internal RAM size : 80 bytes (72 general purpose, 8 special registers)
- 36 single word instructions
- 14-bit instructions
- 2-level stacks
- Operating voltage : 2.3 V ~ 5.5 V
- Operating frequency : 0 ~ 20 MHz
- The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instructions.
- Addressing modes include direct, indirect and relative addressing modes
- Power-on Reset (POR)
- 4 types of power edge-detector reset: 1.8v , 2.1v , always enable 1.8v and Disable
- Sleep mode for power saving
- 2 oscillator start-up time :
  EXT-R、RC：150 μs,20ms
  XT、LF　　：20ms,80ms
- 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- 4 types of oscillator can be selected by user options :
  RC－Low cost RC oscillator
  LFXT－Low frequency crystal oscillator
  XTAL－Standard crystal oscillator
  EXT-R－Low cost R oscillator
- On-chip RC oscillator based Watchdog Timer(WDT) can be operated freely
- 20 I/O pins with their own independent direction control
- 20 I/O pins own independent weak pull-high and can be enabled by software.
- WDT can be enabled by software if WDT Disable is selected in user option.

3. Applications

This MDT10P257 can be used in appliance motor control, high speed automotive, low power remote transmitters/receivers, pointing devices, and telecommunications processors. Such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral … etc.

4. Pin Assignment

MDT10P257P11
MDT10P257S11
MDT10P257K11

RTCC	1	28	/MCLR
V_{dd}	2	27	OSC1
N/C	3	26	OSC2
V_{ss}	4	25	PC7
N/C	5	24	PC6
PA0	6	23	PC5
PA1	7	22	PC4
PA2	8	21	PC3
PA3	9	20	PC2
PB0	10	19	PC1
PB1	11	18	PC0
PB2	12	17	PB7
PB3	13	16	PB6
PB4	14	15	PB5

MDT10P257SS11

VSS	1	28	/MCLR
RTCC	2	27	OSC1
VDD	3	26	OSC2
VDD	4	25	PC7
PA0	5	24	PC6
PA1	6	23	PC5
PA2	7	22	PC4
PA3	8	21	PC3
PB0	9	20	PC2
PB1	10	19	PC1
PB2	11	18	PC0
PB3	12	17	PB7
PB4	13	16	PB6
VSS	14	15	PB5

5. Order Information

MARK	ROM (Words)	RAM (Bytes)	I/O	Timer (8 bit)	Package	Mil
MDT10P257P11	2K	72	28	1	28-DIP	***600 mil***
MDT10P257S11	2K	72	28	1	28-SOP	***300 mil***
MDT10P257SS11	2K	72	28	1	28-SSOP	***209 mil***
MDT10P257K11	2K	72	28	1	28-SKINNY	***300 mil***

6. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA3	I/O	Port A, TTL input level
PB0~PB7	I/O	Port B, TTL input level
PC0~PC7	I/O	Port C, TTL input level
RTCC	I	Real Time Clock/Counter, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
V_{dd}		Power supply
V_{ss}		Ground

7. Memory Map

2. Register Map

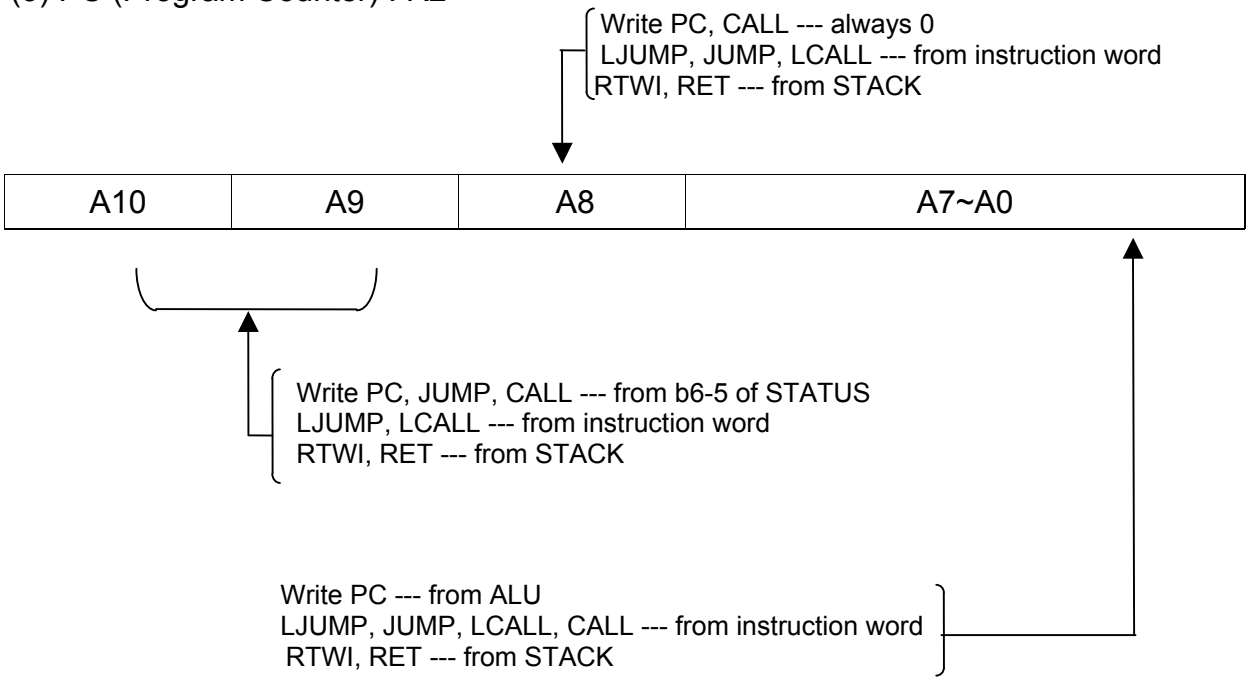
Address	Description
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS
04	MSR
05	Port A
06	Port B
07	Port C
08~0F	Internal RAM, General Purpose Register
10~1F	Internal Memory Select Register (bank 0)
30~3F	Internal Memory Select Register (bank 1)
50~5F	Internal Memory Select Register (bank 2)
70~7F	Internal Memory Select Register (bank 3)

Note : 00~0F, 20~2F, 40~4F, 60~6F are accessed to the same memory location.

2. IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

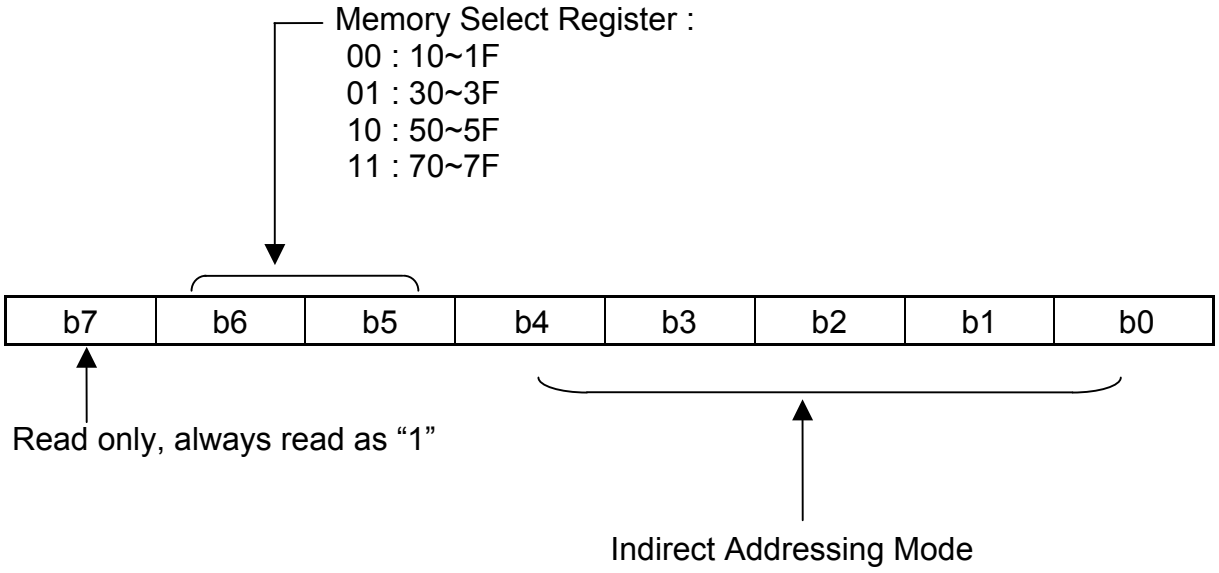
(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power loss Flag bit
4	TF	Time overflow Flag bit
6—5	page	Page select bit : 00 : 000H --- 1FFH 01 : 200H --- 3FFH 10 : 400H --- 5FFH 11 : 600H --- 7FFH
7	——	General purpose bit

(5) MSR (Memory Select Register) : R4



(6) PORT A : R5

PA3~PA0, I/O Register

(7) PORT B : R6

PB7~PB0, I/O Register

(8) PORT C : R7

PC7~PC0, I/O Register

(9) TMR (Time Mode Register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2—0	PS2—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin		
6	PHEN	Global Pull High Enable set : 0 — Enable weak internal Pull High 1 — Disable weak internal Pull High This bit will be ignored if the “I/O pull-hi” is disable in user option.		
7	WDTEN	Watchdog timer Enable set : 0 — Enable WDT 1 — Disable WDT		

(10) CPIO A, CPIO B, CPIO C (Control Port I/O Mode Register)

The CPIO register is “write-only”

＝“0”, I/O pin in output mode;

＝“1”, I/O pin in input mode.

(11) Set Pull hi mode

The Pull hi register is “write-only”

＝“0”, Disable I/O pin Pull hi

＝“1”, Enable I/O pin Pull hi

Do the CPIO instructions twice within three instructions on the same I/O port, then the second CPIO instruction will set the corresponding pull-hi of I/O pins to enable when global pull high Enable.

Correct instruction sequence to enable pull-high

Ex1:

```
LDWI   0FFH
CPIO   06H      ←First：set PortB I/O
LDWI   0FH      ←Second
```

```
CPIO   06H        ←Third：enable Pull hi of PB3-0

Ex2：
LDWI   0FFH
CPIO   06H        ←First：set PortB I/O
CPIO   06H        ←Second：Enable Pull hi of PB7-0

Incorrect instruction sequence to enable pull-high
Ex1: (over three instructions)
LDWI   0FFH
CPIO   06H        ←First：set PortB I/O
LDWI   0FFH       ←Second
NOP               ←Third
CPIO   06H        ←Fourth：set PortB I/O

Ex2：  (Different port)
LDWI   0FFH
CPIO   06H        ←First：set PortB I/O
CPIO   05H        ←set PortA I/O
```

(12) User Options by writer programming :

OSC Type	Description
Ext-R	Low cost external R oscillator
XT	Crystal oscillator
LF	Low frequency crystal oscillator
RC	Low cost RC oscillator

OST	Description
150 us\ 20 ms	OST= 150 us (for RC) or 20ms (for crystal)
20 ms\80 ms	OST= 20 ms (for RC) or 80ms (for crystal)

WDT	Description
Disable	Watchdog timer disable all the time (can be enabled by software,if software WDT enable)
Enable	Watchdog timer enable all the time (always enable)

PED	Description
Disable	PED disable
Low level	1.8V (disable during sleep)
Mid level	2.1V (disable during sleep)
L(all on)	always Enable 1.8V

Security	Description
Disable	Security Disable
Enable	Security Enable

Software WDT	Description
Enable	WDT can be enabled by software
Disable	WDT can't be enabled by software

Freq x 2	Description
Enable	System clock is doubled
Disable	System clock is the oscillation frequency

I/O pull-hi	Description
Enable	Allow software to enable independent I/O pin pull-high
Disable	Disable all pull-high resistors

CLKOUT	Description
Enable	Allow OSC2 to output CLKOUT signal
Disable	OSC2 will be floating

Reset on Err	Description
Enable	The MCU will be reset if two illegal instructions are executed continuously.
Disable	Disable the illegal instruction reset function

8. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR or WDT Reset
CPIO A	— —	1111 1111	1111 1111
CPIO B	— —	1111 1111	1111 1111
CPIO C	— —	1111 1111	1111 1111
TMR	— —	1111 1111	1111 1111
IAR	00h	—	—
RTCC	01h	xxxx xxxx	uuuu uuuu
PC	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu
MSR	04h	100x xxxx	100u uuuu
PORT A	05h	- - - - xxxx	- - - - uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu
PORT C	07h	xxxx xxxx	uuuu uuuu

Note : u = unchanged, x = unknown, - = unimplemented, read as "0"

= value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	u	u
/MCLR reset during SLEEP	1	0
WDT reset (not during SLEEP)	0	1
WDT reset during SLEEP	0	0

9. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT,stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R，t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R，t	Swap halves register	[R(0~3) ↔ R(4~7)]→t	None
011001 trrrrrrr	INCR R，t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R，	Increment register，skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R，t	Add W and register	W + R→t	C，HC，Z
011100 trrrrrrr	SUBWR R，t	Subtract W from register	R － W→t (R+/W+1→t)	C，HC，Z
011101 trrrrrrr	DECR R，t	Decrement register	R － 1→t	Z
011110 trrrrrrr	DECRSZ R，t	Decrement register， skip if zero	R － 1→t	None
010010 trrrrrrr	ANDWR R，t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI I	AND W and immediate	I ∩ W→W	Z
010011 trrrrrrr	IORWR R，t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI I	Inclu. OR W and immediate	I ∪ W→W	Z
010100 trrrrrrr	XORWR R，t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI I	Exclu. OR W and immediate	I ⊕ W→W	Z
011111 trrrrrrr	COMR R，t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R，t	Rotate right register	R(n)→R(n-1)， C→R(7) R(0)→C	C

Instruction Code	Mnemonic Operands	Function	Operating	Status
010101 trrrrrrr	RLR R，t	Rotate left register	R(n)→(n+1)， C→R(0) R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R，b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R，b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R，b	Bit Test，skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R，b	Bit Test，skip if set	Skip if R(b)=1	None
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC， PC+1→Stack	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110000 nnnnnnnn	CALL n	Call subroutine	n→PC, PC+1→Stack	None
110001 iiiiiiii	RTWI i	Return, place immediate to W	Stack→PC, i→W	None
11001n nnnnnnnn	JUMP n	JUMP to address	n→PC	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register		0	: Working register
CPIO	:	Control I/O port register		1	: General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive ‘∪’	/	:	Complement
Exclu.	:	Exclusive ‘⊕’	x	:	Don’t care
AND	:	Logic AND ‘∩’	i	:	Immediate data (8 bits)
			n	:	Immediate address

10. Electrical Characteristics

(A) Operating Voltage & Frequency

V_{dd} ： 2.3 V ~ 5.5 V

Frequency： 0 Hz ~ 20 MHz

(B) Input Voltage

@ V_{dd}＝5.0 V, Temperature＝25 ℃

	Port	Min.	Max.
V_{il}	PA, PB, PC	V_{ss}	1.0 V
	RTCC, /MCLR	V_{ss}	1.0 V
V_{ih}	PA, PB, PC	2.0 V	V_{dd}
	RTCC, /MCLR	3.3 V	V_{dd}

＊Threshold Voltage :

Port A, Port B, Port C V_{th}＝1.5 V

RTCC, /MCLR V_{il}＝1.2 V, V_{ih}＝3.1V (Schmitt Trigger)

(C) Output Voltage

@ V_{dd}＝5.0 V, Temperature＝25 ℃, the typical value as followings :

PA, PB, PC Port	
I_{oh}＝－20.0 mA	V_{oh}＝3.40 V
I_{ol}＝20.0 mA	V_{ol}＝0.50 V
I_{oh}＝－5.0 mA	V_{oh}＝4.50 V
I_{ol}＝5.0 mA	V_{ol}＝0.20 V

(D) Leakage Current

@ V_{dd}＝5.0 V, Temperature＝25 ℃, the typical value as followings :

I_{il}	－ 0.1μA (Max.)
I_{ih}	＋ 0.1 μA (Max.)

(E) Sleep Current

@WDT－Disable, Temperature＝25 ℃, the typical value as followings :

V_{dd}＝2.3 V	I_{dd}＜1.0 μA
V_{dd}＝3.0 V	I_{dd}＜1.0 μA
V_{dd}＝4.0 V	I_{dd}＜1.0 μA
V_{dd}＝5.0 V	I_{dd}＜1.0 μA
V_{dd}＝6.0 V	I_{dd}＜1.0 μA

@WDT－Enable, Temperature＝25 ℃, the typical value as followings :

V_{dd}＝2.3 V	I_{dd}＜1.0 μA
V_{dd}＝3.0 V	I_{dd}＝1.2 μA
V_{dd}＝4.0 V	I_{dd}＝3.0 μA
V_{dd}＝5.0 V	I_{dd}＝5.0 μA
V_{dd}＝6.0 V	I_{dd}＝10 μA

F) Operating Current

Temperature＝25℃, the typical value as followings :

(i) OSC Type＝RC; WDT－Enable;　@ V_{dd}＝5.0 V　PED=Disable

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
3P	4.7 K	9.16 M	1.40mA
	10.0 K	5.6 M	1.00mA
	47.0 K	1.44 M	350 μA
	100.0 K	718.4 K	250 μA
	300.0 K	245.2 K	200 μA
	470.0 K	154.8 K	180 μA
20P	4.7 K	4.72 M	820μA
	10.0 K	2.73 M	550μA
	47.0 K	649.6 K	250 μA
	100.0 K	318.4 K	200 μA
	300.0 K	107.2 K	170 μA
	470.0 K	67.6 K	160 μA
100P	4.7 K	1.68 M	400 μA
	10.0 K	934 K	300 μA
	47.0 K	212.8 K	200 μA
	100.0 K	103.2 K	175 μA
	300.0 K	34.6 K	160 μA
	470.0 K	21.8 K	150 μA

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
300P	4.7 K	716 K	300 μA
	10.0 K	392.4 K	220 μA
	47.0 K	87.6 K	170 μA
	100.0 K	42.4 K	160 μA
	300.0 K	14.2 K	155 μA
	470.0 K	8.8 K	145 μA

(ii) OSC Type＝LF (OSC1&OSC2 External Cap about 20P); WDT－Disable；PED=Disable

Voltage/Frequency	32 K (Ext 50P)	455 K	1 M	Sleep
2.3 V	5.6 μA	2.5V@21.8 μA	38.0 μA	＜1.0 μA
3.0 V	11.5 μA	47.7 μA	70.0 μA	＜1.0 μA
4.0 V	28.7 μA	92.6 μA	125.0 μA	＜1.0 μA
5.0 V	50.0 μA	150 μA	190.0 μA	＜1.0 μA
6.0 V	135.0 μA	225.0 μA	270.0 μA	＜1.0 μA

(iii) OSC Type＝XT (OSC1&OSC2 External Cap about 10P); WDT－Enable；PED=Disable

Voltage/Frequency	1 M	4 M	10 M	Sleep
2.1 V	39.0 μA	120.0 μA	280.0 μA	＜1.0 μA
3.0 V	85.0 μA	240.0 μA	480.0 μA	1.2 μA
4.0 V	160.0 μA	400.0 μA	660.0 μA	3.0 μA
5.0 V	260.0 μA	600.0 μA	1.1 mA	5.0 μA
6.0 V	400.0 μA	840.0 μA	1.5 mA	10.0 μA

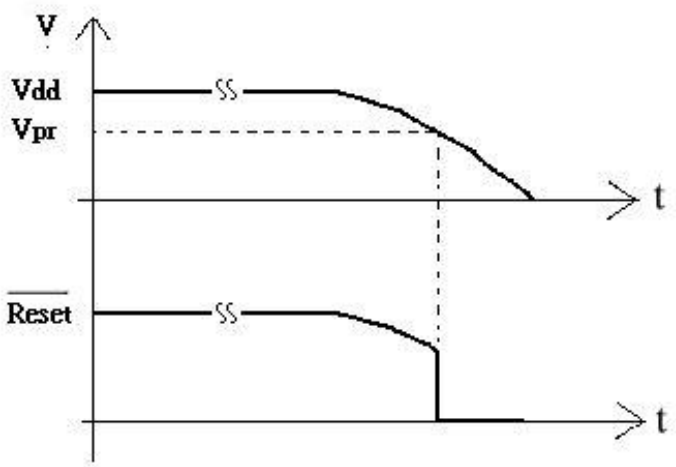
(iv) OSC Type＝EXTR ; WDT－Enable;　@ V_{dd}＝5.0 V　PED=Enable

Rext. (Ohm)		Frequency (Hz)	Current (A)
6.2 K	2.3V	6.56 M	1.7 m
	3.0V	7.10M	1.8 m
	4.0V	7.62M	2.8 m
	5.0V	7.93 M	3.8 m
	5.5V	8.02M	4.3 m
15.0 K	2.3V	3.62 M	750 u
	3.0V	3.90M	1.1 m
	4.0V	4.09M	1.7 m
	5.0V	4.19 M	2.4 m
	5.5V	4.22M	2.7 m
75.0 K	2.3V	965.7 K	220 u
	3.0V	995.7 K	330 u
	4.0V	1.01 M	600 u
	5.0V	1.02 M	880 u
	5.5V	1.02 M	1.1 m
180.0 K	2.3V	417.7 K	100 u
	3.0V	424.9 K	185 u
	4.0V	428.9 K	380 u
	5.0V	431.3 K	640 u
	5.5V	432.4 K	790 u
510.0 K	2.3V	154.2 K	45 u
	3.0V	155.5 K	110 u
	4.0V	156.3 K	280 u
	5.0V	157 K	510 u
	5.5V	157.3 K	640 u
1.1 M	2.3V	72.8 K	30 u
	3.0V	73.2 K	90 u
	4.0V	73.6 K	250 u
	5.0V	73.9 K	480 u
	5.5V	74 K	615 u
2.4 M	2.3V	33.4 K	20 u
	3.0V	33.5 K	80 u
	4.0V	33.7 K	240 u
	5.0V	33.8 K	470 u
	5.5V	33.9 K	600 u

(G) Power Edge-detector Reset Voltage (Not in Sleep Mode) (PED :Enable)

$V_{pr(Low\ level)} \leqq 1.6\sim1.8$ V V_{pr} : V_{dd} (Power Supply)

$V_{pr(Mid\ level)} \leqq 1.9\sim2.1$ V



PS. If PED_Enable then Internal Power_on_reset will be off

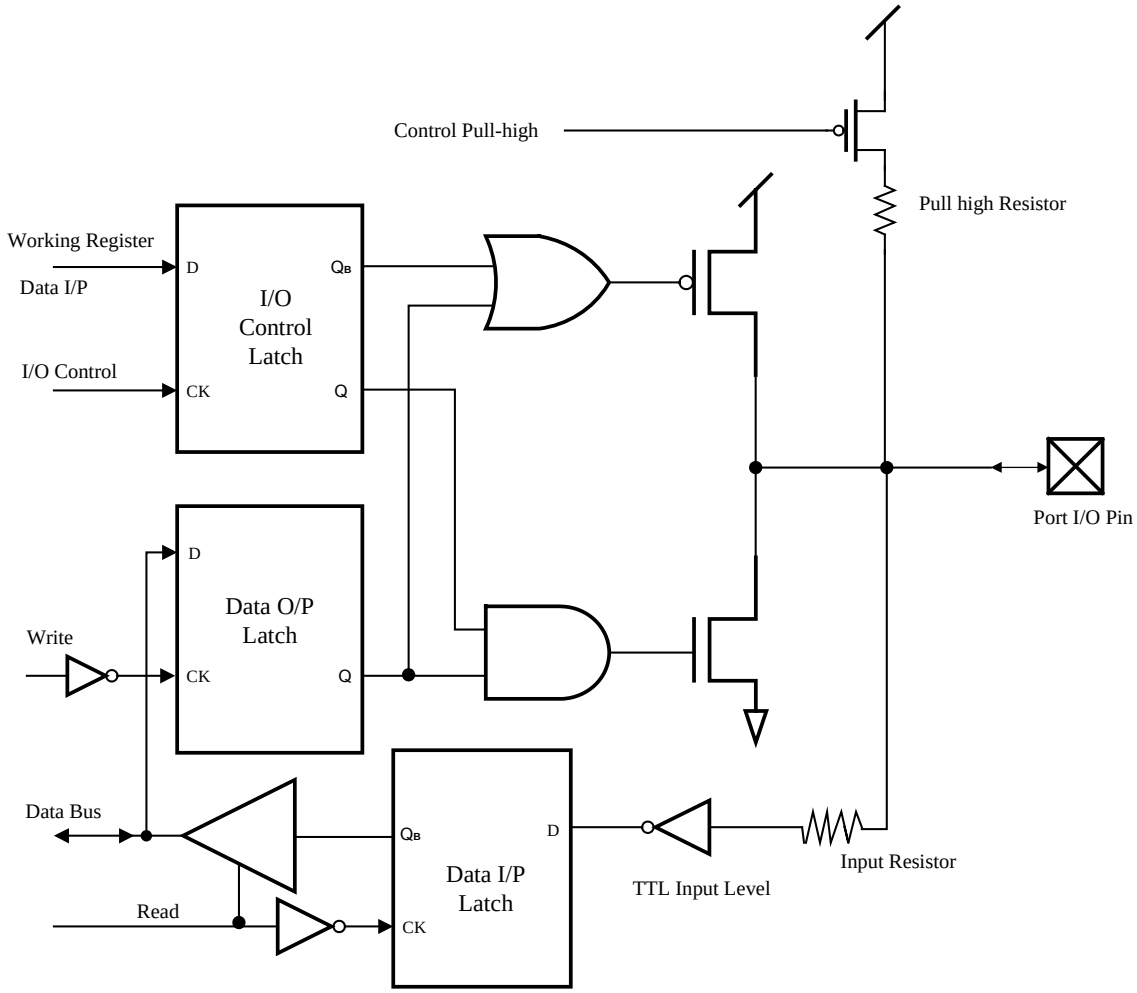
(H) The basic WDT time-out cycle time

@Temperature＝25 ℃, the typical value as followings :

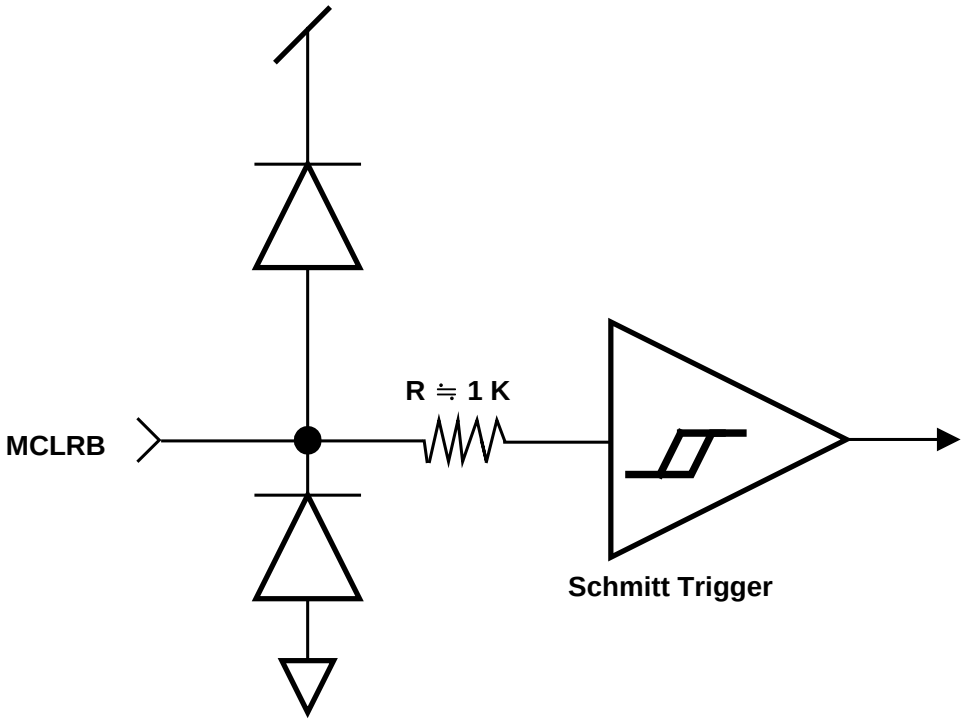
V_{dd} =5.0 V, Temperature=25℃,the typical value as followings:

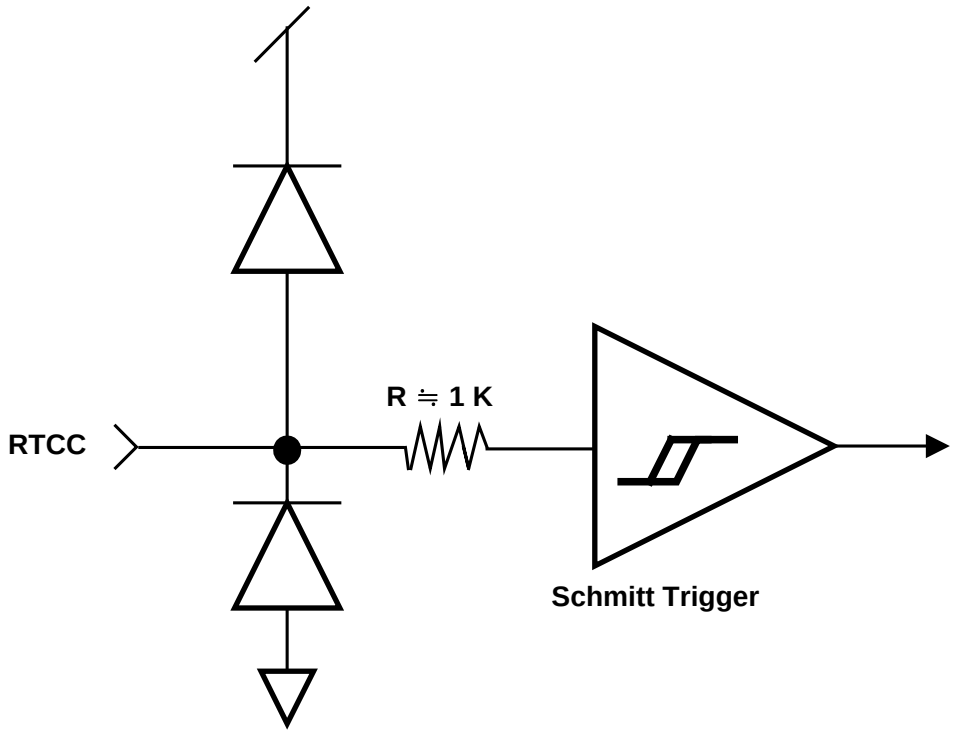
Voltage (V)	Basic WDT time-out cycle time (ms)
2.3	28.5
3.0	25.0
4.0	21.9
5.0	20.3
6.0	19.1

11. Port A ,Port B and Port C Equivalent Circuit

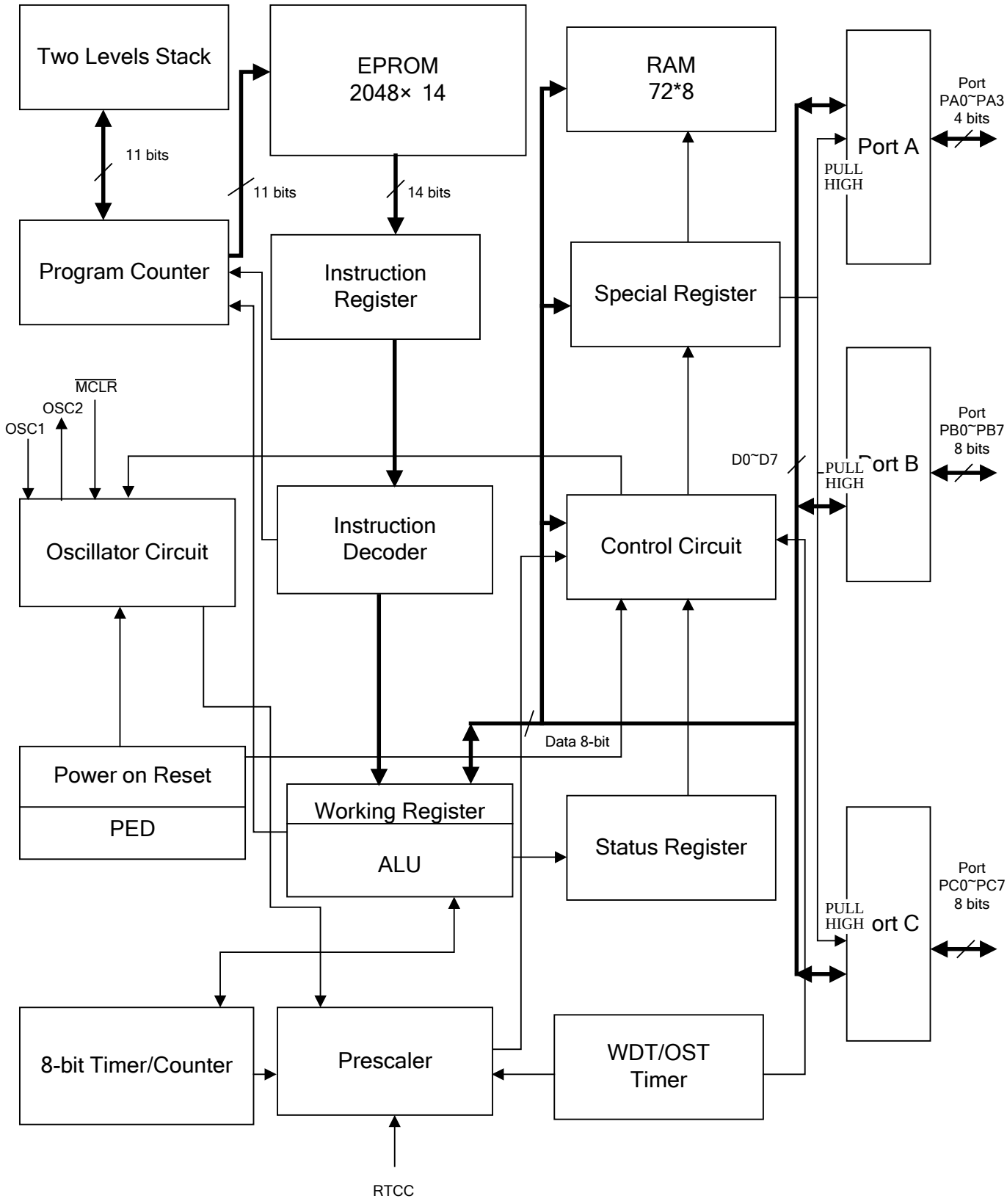


12. MCLRB and RTCC Input Equivalent Circuit





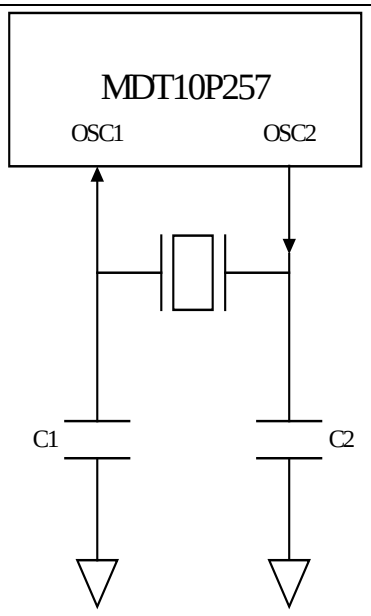
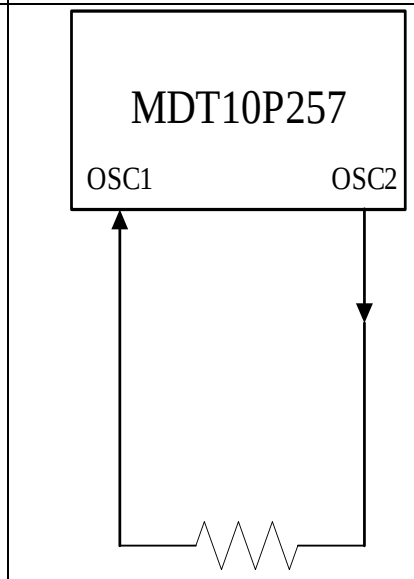
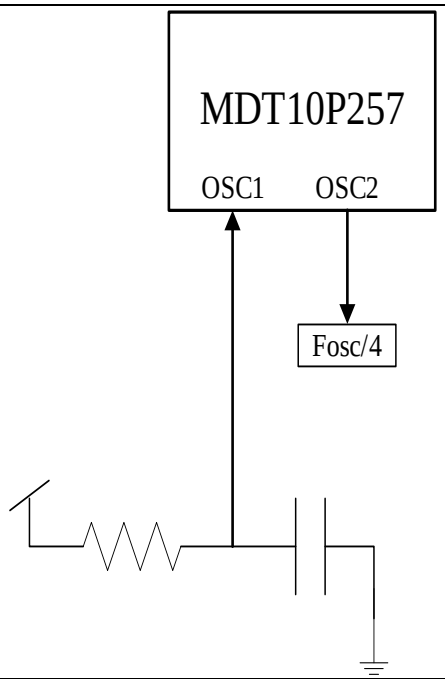
13. Block Diagram



14. External Capacitor Selection For Crystal Oscillator

@ V_{dd} = 3.0 V~ 5.0 V

Osc. Type	Resonator Freq.	C1	C2
XT	10 MHz	10 pF ~30 pF	10 pF ~50 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
	1 MHz	10 pF ~30 pF	20 pF ~50 pF
LF	1 MHz	3 pF ~5 pF	3 pF ~5 pF
	455 K	10 pF ~30 pF	20 pF ~50 pF
	32 K	10 pF ~20 pF	15 pF ~30 pF

XT Oscillator Mode LF Oscillator Mode	Ext-R Oscillator Mode	RC Oscillator Mode
		

The above values of the external capacitor are listed for reference but the higher capacitance will increases the start-up time.