

## SOT-363 Plastic-Encapsulate MOSFETS

### CJ3439KDW N channel+P Channel MOSFET

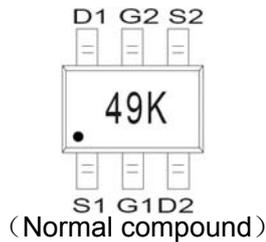
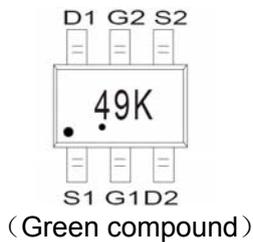
#### FEATURE

- Surface Mount Package
- Low  $R_{DS(on)}$
- Operated at Low Logic Level Gate Drive
- ESD Protected Gate
- Including a N-ch CJ3134K and a P-ch CJ3139K (independently) In a Package

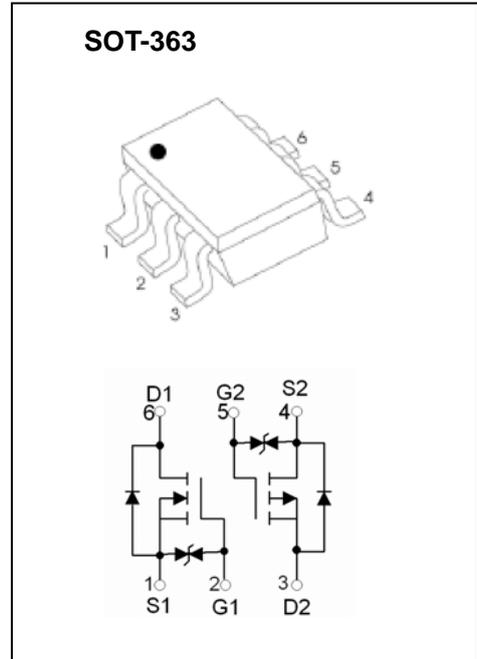
#### APPLICATION

- Load/ Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

#### MARKING



(49K=Device Code  
Solid Dot=Pin 1 indicator)



#### ABSOLUTE MAXIMUM RATINGS ( $T_a=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
<b>N-MOSFET</b>			
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current (note 1)	$I_D$	0.75	A
Pulsed Drain Current ( $t_p=10\mu\text{s}$ )	$I_{DM}$	1.8	A
<b>P-MOSFET</b>			
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current (note 1)	$I_D$	-0.66	A
Pulsed Drain Current ( $t_p=10\mu\text{s}$ )	$I_{DM}$	-1.2	A
<b>Temperature and Thermal Resistance</b>			
Thermal Resistance from Junction to Ambient (note 1)	$R_{\theta JA}$	833	$^{\circ}\text{C}/\text{W}$
Junction Temperature	$T_J$	150	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	-55~+150	$^{\circ}\text{C}$
Lead Temperature for Soldering Purposes(1/8" from case for 10 s)	$T_L$	260	$^{\circ}\text{C}$

N-ch MOSFET ELECTRICAL CHARACTERISTICS( $T_a=25^{\circ}\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>STATIC CHARACTERISTICS</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 20V, V_{GS} = 0V$			1	$\mu A$
Gate-body leakage current	$I_{GSS}$	$V_{GS} = \pm 12V, V_{DS} = 0V$			$\pm 50$	$\mu A$
Gate threshold voltage (note 2)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.35		1	V
Drain-source on-resistance(note 2)	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 0.65A$			380	$m\Omega$
		$V_{GS} = 2.5V, I_D = 0.55A$			450	$m\Omega$
		$V_{GS} = 1.8V, I_D = 0.45A$			800	$m\Omega$
Forward tranconductance(note 2)	$g_{FS}$	$V_{DS} = 10V, I_D = 0.8A$		1.6		S
Diode forward voltage	$V_{SD}$	$I_S = 0.15A, V_{GS} = 0V$			1.2	V
<b>DYNAMIC CHARACTERISTICS (note 4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 16V, V_{GS} = 0V, f = 1MHz$		79	120	pF
Output Capacitance	$C_{oss}$			13	20	pF
Reverse Transfer Capacitance	$C_{rss}$			9	15	pF
<b>SWITCHING CHARACTERISTICS (note 3,4)</b>						
Turn-on delay time	$t_{d(on)}$	$V_{GS} = 4.5V, V_{DS} = 10V,$ $I_D = 500mA, R_{GEN} = 10\Omega$		6.7		ns
Turn-on rise time	$t_r$			4.8		ns
Turn-off delay time	$t_{d(off)}$			17.3		ns
Turn-off fall time	$t_f$			7.4		ns

P-ch MOSFET ELECTRICAL CHARACTERISTICS( $T_a=25^{\circ}\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>STATIC CHARACTERISTICS</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = -20V, V_{GS} = 0V$			-1	$\mu A$
Gate-body leakage current	$I_{GSS}$	$V_{GS} = \pm 12V, V_{DS} = 0V$			$\pm 20$	$\mu A$
Gate threshold voltage (note 2)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.35		-1.1	V
Drain-source on-resistance(note 2)	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -1A$			520	$m\Omega$
		$V_{GS} = -2.5V, I_D = -0.8A$			700	$m\Omega$
		$V_{GS} = -1.8V, I_D = -0.5A$			950	$m\Omega$
Forward tranconductance(note 2)	$g_{FS}$	$V_{DS} = -10V, I_D = -0.54A$		1.2		S
Diode forward voltage	$V_{SD}$	$I_S = -0.5A, V_{GS} = 0V$			-1.2	V
<b>DYNAMIC CHARACTERISTICS (note 4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -16V, V_{GS} = 0V, f = 1MHz$		113	170	pF
Output Capacitance	$C_{oss}$			15	25	pF
Reverse Transfer Capacitance	$C_{rss}$			9	15	pF
<b>SWITCHING CHARACTERISTICS (note 3, 4)</b>						
Turn-on delay time	$t_{d(on)}$	$V_{GS} = -4.5V, V_{DS} = -10V,$ $I_D = -200mA, R_{GEN} = 10\Omega$		9		ns
Turn-on rise time	$t_r$			5.8		ns
Turn-off delay time	$t_{d(off)}$			32.7		ns
Turn-off fall time	$t_f$			20.3		ns

**Notes :**

- 1.Surface mounted on FR4 board using the minimum recommended pad size.
2. Pulse Test : Pulse width=300 $\mu s$ , duty cycle $\leq 2\%$ .
3. Switching characteristics are independent of operating junction temperature.
4. Granted by design, not subject to producing.