TCAN1044x-Q1 Automotive High Speed CAN Transceiver

ADVANCE INFORMATION

1 Features

- AEC Q100: Qualified for Automotive Applications
  - Device Temperature Grade 1: –40°C to 125°C T_A
- Meets the Requirements of ISO 11898-2:2016 and ISO 11898-5:2007 Physical Layer Standards
- Support of Classical CAN and CAN FD up to 5 Mbps
  - Short and Symmetrical Propagation Delays and Fast Loop Times for Enhanced Timing Margin
  - Higher Data Rates in Loaded CAN Networks
- I/O Voltage Range Supports 1.8 V to 5 V
- Optimized Behavior When Unpowered
  - Bus and Logic Terminals are High Impedance (No Load to Operating Bus or Application)
  - Hot Plug Capable: Power Up/Down Glitch Free Operation On Bus and RXD Output
- Meets or Exceeds the Standard Requirements:
  - SAE J2962-2 (2016) Communication Transceivers Qualification
  - GIFT/ICT
  - ISO 16845-2 High Speed Medium Access Unit Conformance
- Protection Features
  - IEC ESD Protection of Bus Terminals: ±15 kV
  - Bus Fault Protection: ±42 V
  - Undervoltage Protection On Supply Terminals
  - Driver Dominant Timeout (TXD DTO)
    - Data Rates Down to 9.2 kbps
  - Thermal Shutdown Protection (TSD)
- Junction Temperatures From: –40°C to 150°C
- Available in SOIC (8) Package and Leadless VSON (8) Package 3.0 mm x 3.0 mm with improved Automated Optical Inspection (AOI) Capability

2 Applications

- 12-V System Applications
- Automotive and Transportation
  - Advanced Driver Assistance System (ADAS)
  - Infotainment
  - Body Electronics & Lighting

3 Description

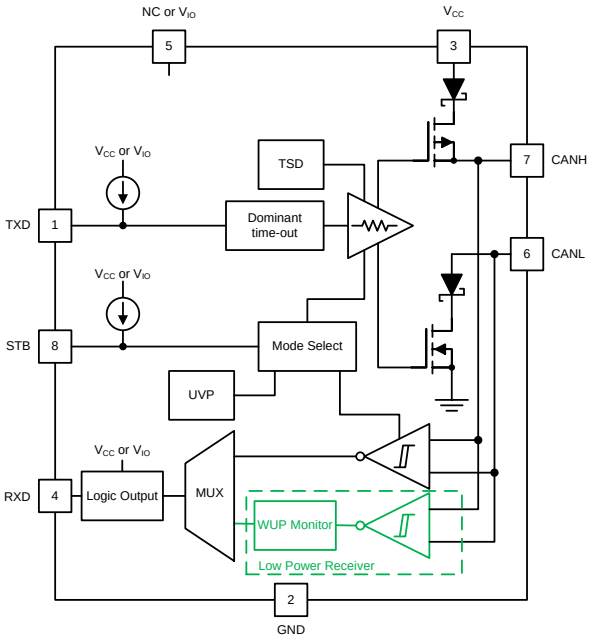
The TCAN1044x-Q1 devices are high speed Controller Area Network (CAN) transceivers that meet the physical layer requirements of the ISO 11898-2:2016 high speed CAN specification providing an interface between the CAN bus and a CAN protocol controller. The TCAN1044x-Q1 devices support both classical CAN and CAN FD networks up to 5 megabits per second (Mbps). The device part numbers with the "V" suffix include internal logic level translation via the V_{IO} terminal to allow for interfacing directly to 1.8 V, 3.3 V, or 5 V controllers. The devices have a low-power standby mode which supports remote wake-up via the ISO 11898-2:2016 defined wake-up pattern (WUP). The TCAN1044x-Q1 devices include many protection and diagnostic features including thermal shutdown (TSD), driver dominant timeout (TXD DTO), and bus fault protection up to ±42 V.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCAN1044x-Q1	SOIC (D) (8)	4.90 mm x 3.91 mm
	VSON (DRB) (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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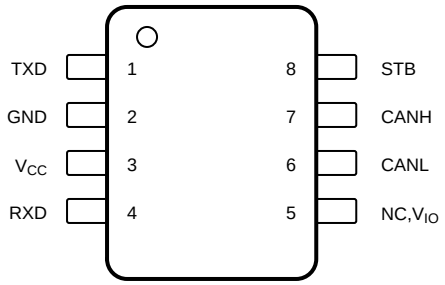
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2018	*	Initial release

5 Pin Configuration and Functions

D Package TCAN1044(V)-Q1
8-Pin SOIC
Top View



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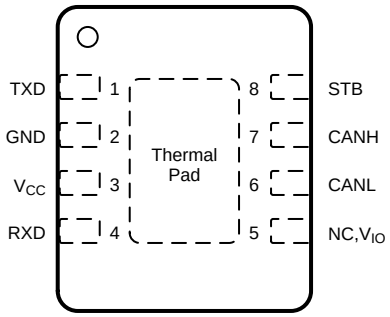
DRB Package TCAN1044(V)-Q1
8-Pin VSON
Top View



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Pin Functions

PIN			TYPE	DESCRIPTION
NAME	D	DRB		
TXD	1	1	Digital Input	CAN transmit data input (low for dominant and high for recessive bus states)
GND	2	2	GND	Ground connection
V_{CC}	3	3	Supply	5-V supply voltage
RXD	4	4	Digital Output	CAN receive data output (low for dominant and high for recessive bus states), tri-state when powered off
NC	5	5	—	No Connect (not internally connected); Devices without V_{IO}
V_{IO}			Supply	I/O supply voltage; Devices with V_{IO}
CANL	6	6	Bus I/O	Low-level CAN bus input/output line
CANH	7	7	Bus I/O	High-level CAN bus input/output line
STB	8	8	Input	Standby input for mode control, integrated pull up
Thermal PAD		—	—	Connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN Bus I/O voltage (CANH, CANL)	–42	42	V
V_{DIFF}	Max differential voltage range between CANH and CANL	-27	27	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{RXD}	RXD output terminal voltage range	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Operating virtual junction temperature range	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pins	±4000	V
			HBM classifiation level 3B for global pins CANH & CANL	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings, IEC Specification

				VALUE	UNIT
V_{ESD}	System level electro-static discharge (ESD)(1)	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2 (150pF, 330Ω): Unpowered contact discharge	±15000	V
V_{Tran}	ISO7637 ISO Pulse Transients(2)	CAN bus terminals (CANH, CANL)	Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	ISO7637 Slow transients pulse(3)	CAN bus terminals (CANH, CANL) to GND	DCC slow transient pulse	±85	V

(1) Tested according to IEC 62228-3 CAN Transcievers (2018), Section 6.4; DIN EN 61000-4.
(2) Tested according to IEC 62228-3 CAN Transcievers (2018), Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
(3) Tested according to ISO 7637-3 (2017); Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{CC}	Supply voltage - VeLIO Compliance	4.75	5	5.25	V
V_{IO}	Supply voltage for I/O level shifter	1.7		5.5	V
$I_{OH(RXD)}$	RXD terminal high level output current	–2			mA
$I_{OL(RXD)}$	RXD terminal low level output current			2	mA
T_A	Operational free-air temperature (see thermal characteristics table)	–40		125	°C

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6.5 Thermal Characteristics

THERMAL METRIC		TCAN1044x–Q1		UNIT
		D (SOIC)	DMT (VSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.1	49.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	58.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.6	23.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.8	23.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	6.4	°C/W

6.6 Power Supply Characteristics

Over recomended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current normal mode	Dominant	See Figure 6,TXD = 0 V, R_L = 60 Ω, C_L = open			70	mA
I_{CC}	Supply current normal mode	Dominant	See Figure 6, TXD = 0 V, R_L = 50 Ω, C_L = open			80	mA
I_{CC}	Supply current normal mode	Dominant with bus fault	See Figure 6, TXD = 0 V, CANH = CANL = ±25 V, R_L = open, C_L = open			180	mA
I_{CC}	Supply current normal mode	Recessive	See Figure 6, TXD = V_{CC}, R_L = 50 Ω, C_L = open, RCM = open			5	mA
I_{CC}	Supply current standby mode		See Figure 6, TXD = V_{CC}, R_L = 50 Ω, C_L = open, Devices with V_{IO}			1	µA
I_{CC}	Supply current standby mode		See Figure 6, TXD = V_{CC}, R_L = 50 Ω, C_L = open, Devices without V_{IO}			12	µA
I_{IO}	I/O supply current normal mode (Devices with V_{IO})	Dominant	RXD floating, TXD = 0 V			300	µA
I_{IO}	I/O supply current normal mode (Devices with V_{IO})	Recessive	RXD floating, TXD = V_{CC}			35	µA
I_{IO}	I/O supply current standby mode (Devices with V_{IO})		RXD floating, TXD = V_{CC}			11	µA
UV_{VCC}	Rising under voltage detection on V_{CC} for protected mode				4.2	4.4	V
UV_{VCC}	Falling under voltage detection on V_{CC} for protected mode			3.5	4	4.5	V
UV_{VIO}	Rising under voltage detection on V_{IO} (Devices with V_{IO})					1.65	V
UV_{VIO}	Falling under voltage detection on V_{IO} (Devices with V_{IO})			1.4			V

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6.7 Dissipation Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5 V, V_{IO} = 1.8 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		V
		V_{CC} = 5 V, V_{IO} = 3.3 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5 V, V_{IO} = 5 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5.5 V, V_{IO} = 1.8 V, T_J= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_J= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_J= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
T_{TSD}	Thermal shutdown temperature			192		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			10		

6.8 Electrical Characteristics

Over recomended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(D)}$	Dominant output voltage normal mode	CANH	See Figure 4 and Figure 7, TXD = 0 V, R_L = 60 Ω, C_L = open	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(R)}$	Recessive output voltage normal mode		See Figure 4 and Figure 7, TXD = V_{CC}, R_L = open	2	0.5 x V_{CC}	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		See Figure 7 and Figure 16, R_{TERM} = 60 Ω, C_L = open, C_{SPLIT} = 4.7 nF	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)		See Figure 4 and Figure 7, R_L = 60 Ω, C_L = open	–400		400	mV
$V_{OD(D)}$	Differential output voltage normal mode Dominant		See Figure 4 and Figure 7, TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open	1.5		3	V
			See Figure 4 and Figure 7, TXD = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open	1.4		3.3	V
			See Figure 4 and Figure 7, TXD = 0 V, R_L = 2240 Ω, C_L = open	1.5		5	V
$V_{OD(R)}$	Differential output voltage normal mode Recessive		See Figure 4 and Figure 7, TXD = V_{CC}, R_L = 60 Ω, C_L = open	–120		12	mV
			See Figure 4 and Figure 7, Normal mode, TXD = V_{CC}, R_L = open, C_L = open	–50		50	mV
$V_{O(STB)}$	Bus output voltage standby mode		CANH, no load	-0.1	0	0.1	V
			CANL, no load	-0.1	0	0.1	V
			CANH - CANL, no load	-0.2	0	0.2	V
$I_{OS(DOM)}$	Short-circuit steady-state output current, Dominant		See Figure 4 and Figure 12, Normal mode, -15 V ≤ $V_{(CAN\_H)}$ ≤ 40 V, TXD = 0 V	–115			mA
			See Figure 4 and Figure 12, Normal mode, -15 V ≤ $V_{(CAN\_L)}$ ≤ 40 V, TXD = 0 V			115	mA

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Electrical Characteristics (continued)

Over recomended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OS(REC)}$	Short-circuit steady-state output current; Recessive	See Figure 4 and Figure 12, Normal mode, –27 V ≤ V_{BUS} ≤ 32 V, V_{BUS} = CANH = CANL	–5		5	mA
Receiver Electrical Characteristics						
V_{IT}	Input threshold voltage normal mode	See Figure 8, Table 1, and Table 6 -12 V ≤ V_{CM} ≤ 12 V	500		900	mV
$V_{IT(STB)}$	Input threshold standby mode	See Figure 8, Table 1, and Table 6 -12 V ≤ V_{CM} ≤ 12 V	400		1150	mV
$V_{DIFF(DOM)}$	Normal mode dominant state differential input voltage range	See Figure 8, Table 1, and Table 6 -12 V ≤ V_{CM} ≤ 12 V	0.9		9	V
$V_{DIFF(DOM)}$	Standby mode dominant state differential input voltage range	See Figure 8, Table 1, and Table 6 -12 V ≤ V_{CM} ≤ 12 V	1.15		9	V
$V_{DIFF(REC)}$	Normal mode recessive state differential input voltage range	See Figure 8, Table 1, and Table 6 -12 V ≤ V_{CM} ≤ 12 V	-4		0.5	V
$V_{DIFF(REC)}$	Standby mode recessive state differential input voltage range	See Figure 8, Table 1, and Table 6 -12 V ≤ V_{CM} ≤ 12 V	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold normal mode	See Figure 8, Table 1, and Table 6 -12 V ≤ V_{CM} ≤ 12 V		100		mV
V_{CM}	Common mode range normal and standby modes	See Figure 8 and Table 6	–12		12	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{CC} , V_{IO} = V_{CC}			20	pF
C_{ID}	Differential input capacitance	TXD = V_{CC} , V_{IO} = V_{CC}			10	pF
R_{ID}	Differential input resistance	Normal mode, TXD = V_{CC} = V_{IO} = 5 V -12 V ≤ V_{CM} ≤ 12 V	40		90	kΩ
R_{IN}	Single ended input resistance (CANH or CANL)		20		45	kΩ
$R_{IN(M)}$	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5V	–1%		1%	
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 × V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 × V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 × V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0 V, V_{CC} = V_{IO} = 5.5 V	–200	-100	–20	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
C_I	Input Capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t)+2.5 V		5		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level input voltage	Devices without V_{IO} See Figure 8, I_O = –2 mA	0.8 × V_{CC}			V
V_{OH}	High-level input voltage	Devices with V_{IO} See Figure 8, I_O = –2 mA	0.8 × V_{IO}			V
V_{OL}	Low-level input voltage	Devices without V_{IO} See Figure 8, I_O = 2 mA			0.2 × V_{CC}	V
V_{OL}	Low-level input voltage	Devices with V_{IO} See Figure 8, I_O = 2 mA			0.2 × V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 × V_{CC}			V

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Electrical Characteristics (continued)

Over recomended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 × V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 × V_{IO}	V
I_{IH}	High-level input leakage current STB	V_{CC} = V_{IO} = STB = 5.5 V	–2		2	µA
I_{IL}	Low-level input leakage current STB	V_{CC} = V_{IO} = 5.5 V, STB = 0 V	–20		–2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.5V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA

6.9 Switching Characteristics

Over recomended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See Figure 9 , Normal mode, V_{IO} = 2.8 V to 5 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		100	180	ns
		See Figure 9 , Normal mode, V_{IO} = 1.8 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		150	255	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	See Figure 9 , Normal mode, V_{IO} = 2.8 V to 5 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		110	180	ns
		See Figure 9 , Normal mode, V_{IO} = 1.8 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		150	255	ns
t_{MODE}	Mode change time, from Normal to Standby or from Standby to Normal	See Figure 10			20	µs
t_{WK_FILTER}	Filter time for a valid wake-up pattern	See Figure 14	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value	See Figure 14	0.8		5	ms
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	See Figure 7 R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		75		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			65		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			20		ns
t_R	Differential output signal rise time			45		ns
t_F	Differential output signal fall time			45		ns
t_{TXD_DTO}	Dominant timeout	See Figure 11, R_L = 60 Ω, C_L = 100 pF	1.2		4.0	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	See Figure 8 $C_{L(RXD)}$ = 15 pF		65		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			50		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns
FD Timing Characteristics						

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Switching Characteristics (continued)

Over recomended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	See Figure 9, STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	435		530	ns
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns		155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns		400		550	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns		120		220	ns
t_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-65		40	ns
t_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns		-45		15	ns

6.10 Typical Characteristics

Graph Placeholder

Figure 1. $V_{OD(D)}$ over Temperature

Graph Placeholder

Figure 2. $V_{OD(D)}$ over V_{CC}

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7 Parameter Measurement Information

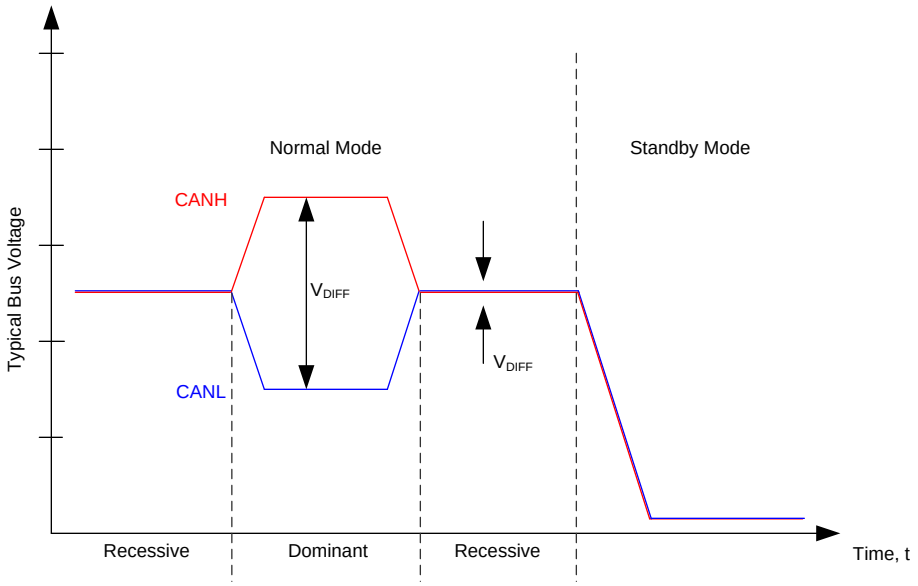
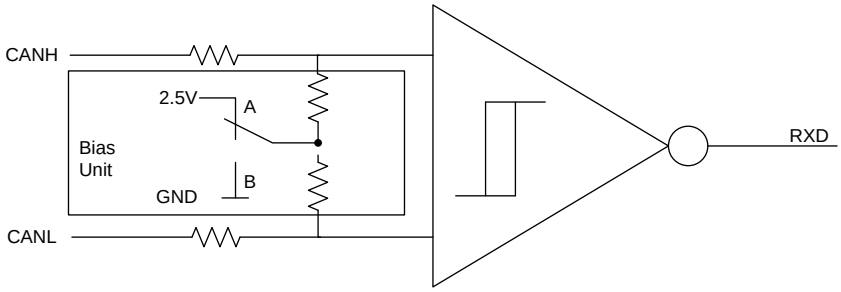


Figure 3. Bus States



A. Normal Mode
B. Standby Mode (Low Power)

Figure 4. Simplified Recessive Common Mode Bias Unit and Receiver

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Parameter Measurement Information (continued)

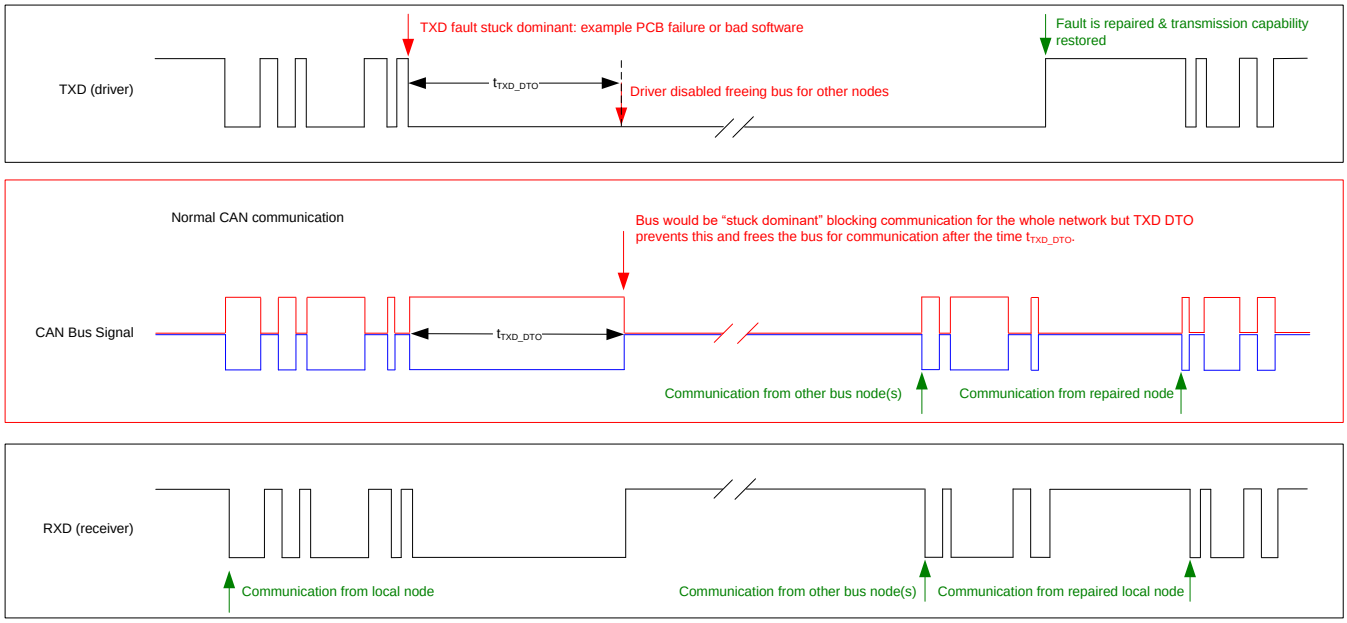

Figure 5. Example Timing Diagram for TXD Dominant Timeout

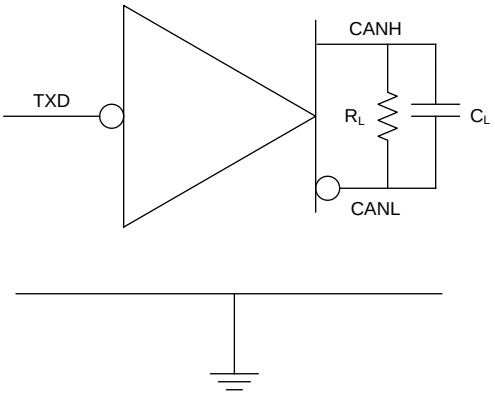

Figure 6. I_{CC} Test Circuit

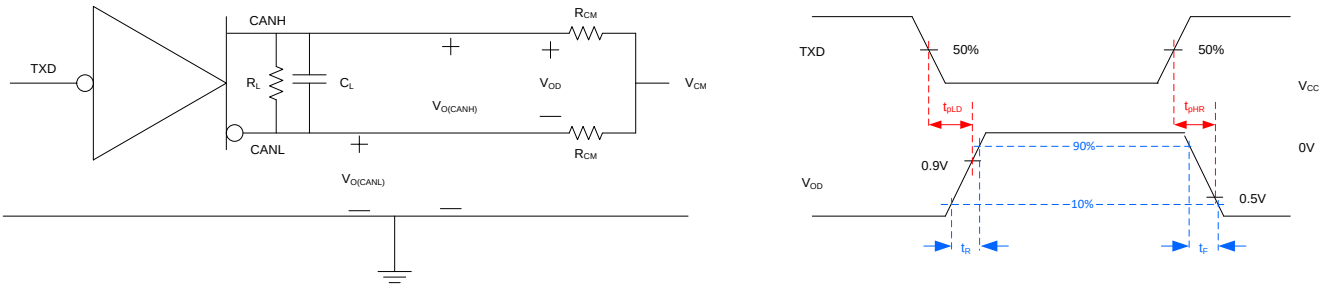

Figure 7. Driver Test Circuit and Measurement

ADVANCE INFORMATION

Parameter Measurement Information (continued)

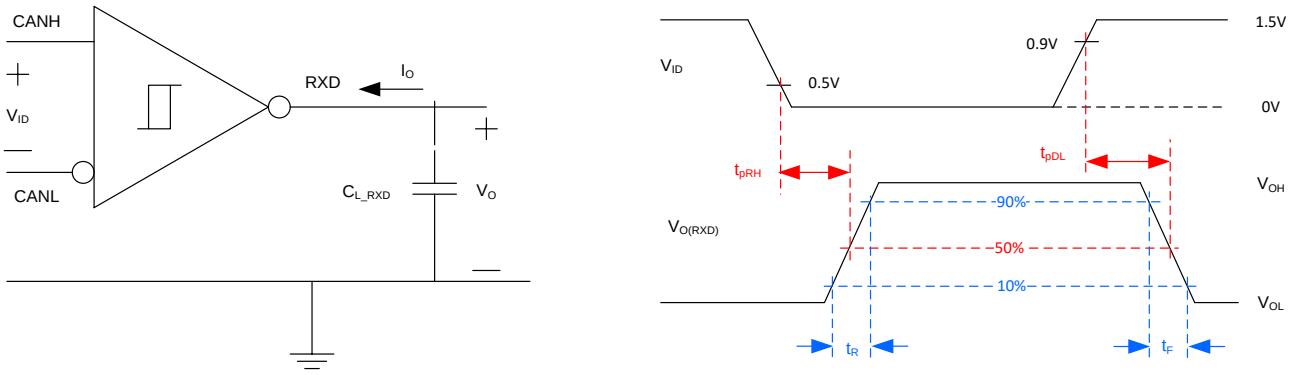

Figure 8. Receiver Test Circuit and Measurement

Table 1. Receiver Differential Input Voltage Threshold Test (See Figure 8)

Input			Output	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	RXD	
-11.5 V	-12.5 V	1000 mV	L	V_{OL}
12.5 V	11.5 V	1000 mV	L	
-8.55 V	-9.45 V	900 mV	L	
9.45 V	8.55 V	900 mV	L	
-8.25 V	-9.25 V	500 mV	H	V_{OH}
9.25 V	8.25 V	500 mV	H	
-11.8 V	-12.2 V	400 mV	H	
12.2 V	11.8 V	400 mV	H	
Open	Open	X	H	

ADVANCE INFORMATION

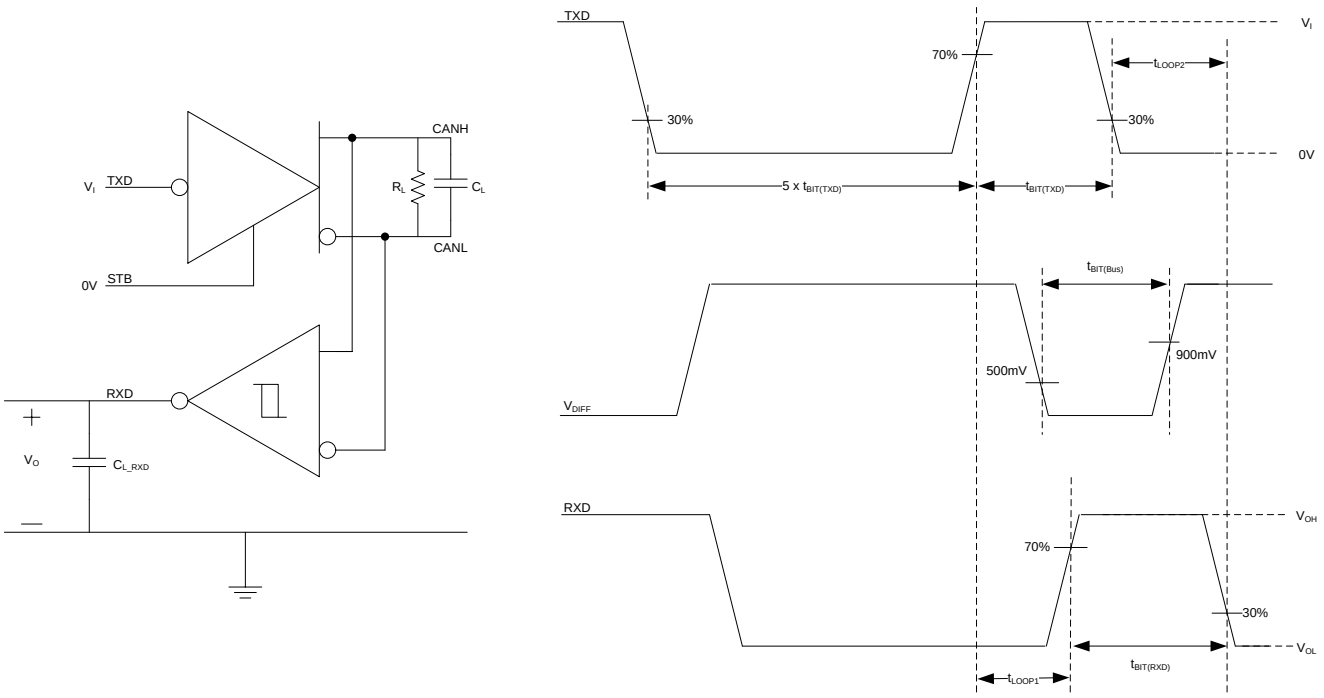

Figure 9. Transmitter and Receiver Timing Test Circuit and Measurement

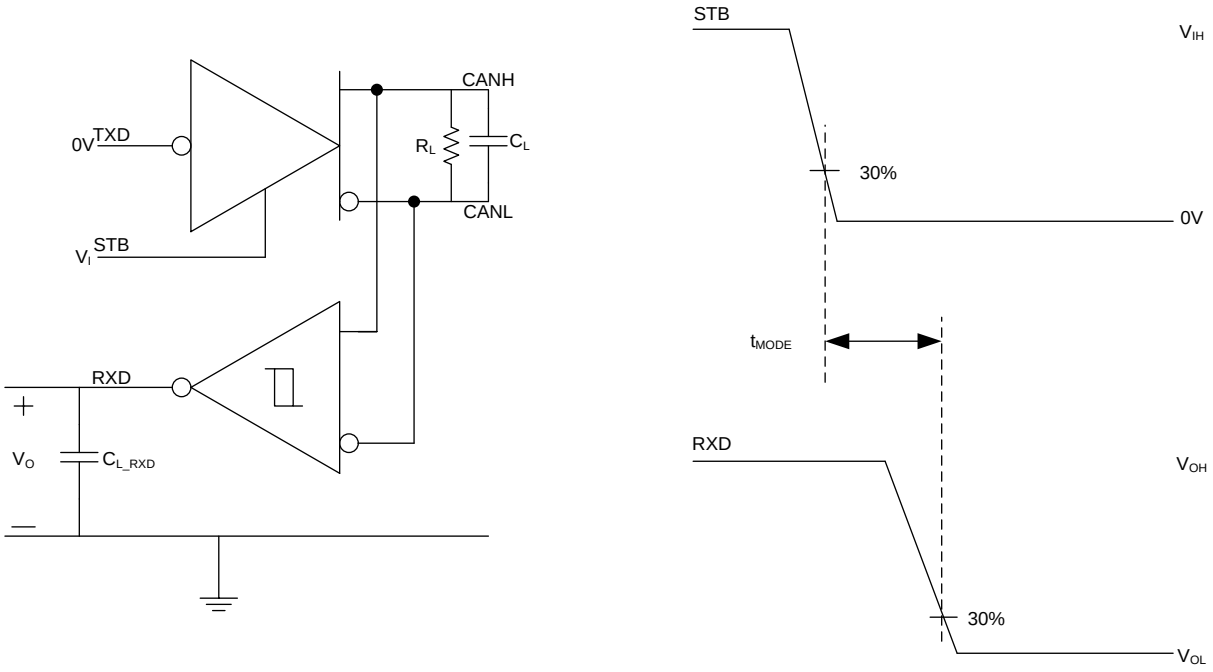

Figure 10. t_{MODE} Test Circuit and Measurement

ADVANCE INFORMATION

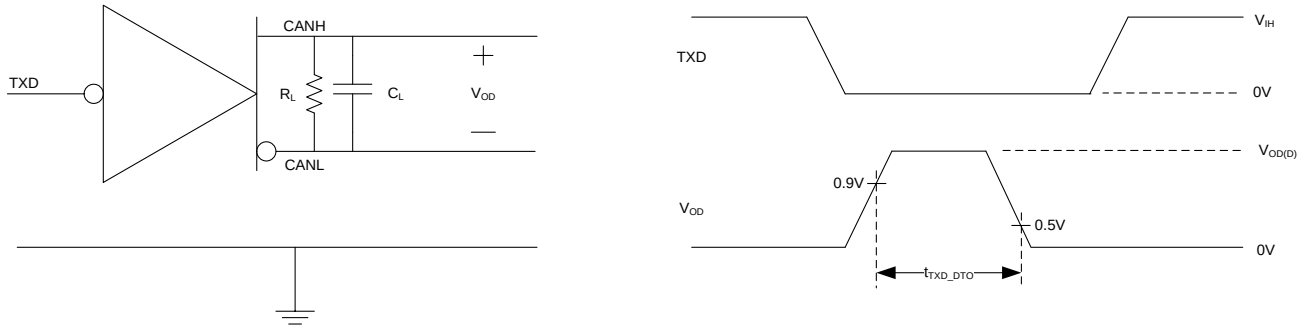

Figure 11. TXD Dominant Timeout Test Circuit and Measurement

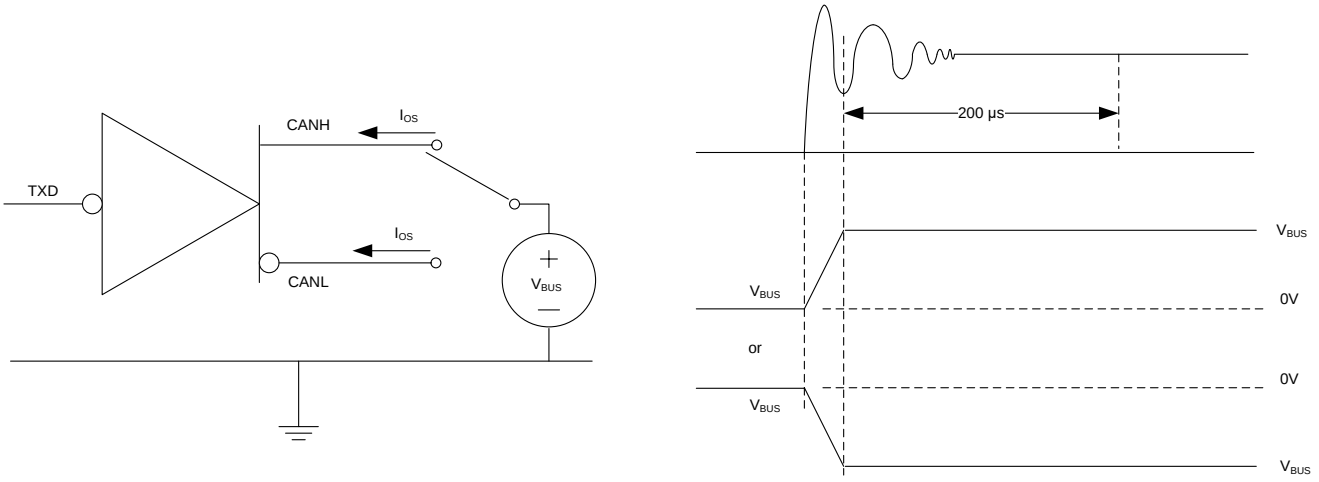

Figure 12. Driver Short-Circuit Current Test and Measurement

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8 Detailed Description

8.1 Overview

The TCAN1044x-Q1 devices meet or exceed the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The devices have been certified to the requirements of ISO 11898-2:2016 and ISO 11898-5:2007 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The TCAN1044x-Q1 devices provides differential transmit capability to the CAN bus and differential receive capability from the CAN bus. The device includes many protection features providing device and CAN bus robustness. The TCAN1044x-Q1 supports CAN and CAN FD (Flexible Data Rate) up to 5 Mbps.

8.1.1 Functional Block Diagrams

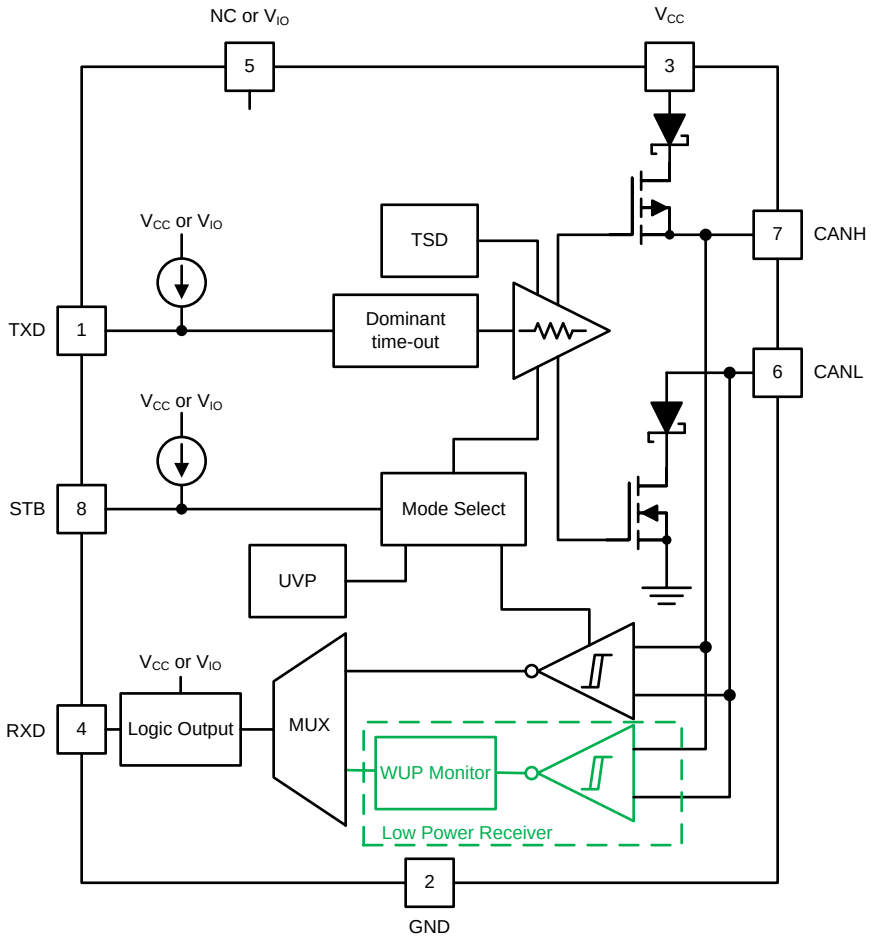

Figure 13. TCAN1044(V)-Q1 Block Diagram

8.2 Feature Description

8.2.1 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 3 and Figure 4.

A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD terminal. A recessive bus state is when the bus is biased to V_{CC} / 2 via the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the TXD and RXD terminals.

ADVANCE INFORMATION

Feature Description (continued)

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, in this case the differential voltage of the bus will be greater than the differential voltage of a single driver.

The host controller of the CAN node uses the TXD terminal to drive the bus and will receive data from the bus on the RXD terminal. Using the TCAN1044x-Q1 devices allows for the I/O voltage to be level shifted between 1.8 V to 5 V for the host controller via the V_{IO} pin.

Transceivers with low power standby (STB) mode have a third bus state where the bus terminals are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 3 and Figure 4.

8.2.2 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout constant of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on TXD terminal, thus clearing the dominant time out. The receiver remains active and the RXD terminal will reflect the activity on the CAN bus and the bus terminals will be biased to recessive level during a TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

8.2.3 CAN Bus Short Circuit Current Limiting

The TCAN1044x-Q1 devices have several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting in dominant and recessive states. The devices have TXD dominant timeout which prevents permanently having the higher short circuit current of dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings the average short circuit current should be used. The percentage dominant is limited by the TXD dominant timeout and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

NOTE

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%\text{Transmit} \times [(\%\text{REC\_Bits} \times I_{OS(SS)\_REC}) + (\%\text{DOM\_Bits} \times I_{OS(SS)\_DOM})] + [\%\text{Receive} \times I_{OS(SS)\_REC}] \quad (2)$$

ADVANCE INFORMATION

Feature Description (continued)

Where:

- $IO_{S(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance, other network components, and the power supply used to generate V_{CC}.

8.2.4 Thermal Shutdown

If the junction temperature of the devices exceed the thermal shutdown threshold the TCAN1044x-Q1 turns off the CAN driver circuitry thus blocking the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the TCAN1044x-Q1 drops below the thermal shutdown temperature of the device. The CAN bus terminals will be biased to recessive level during a thermal shutdown fault and the receiver to RXD path will remain operational. If the fault condition that caused the thermal shutdown is still present, the temperature may rise again and the device will enter thermal shutdown again. Prolonged operation with thermal shutdown conditions may affect device reliability. The thermal shutdown circuit includes hysteresis to avoid oscillation of the driver output.

8.2.5 Under Voltage Lockout (UVLO) and Unpowered Device

The V_{CC} supply terminal has under voltage detection circuitry which places the device in a protected mode if an under voltage fault occurs. This protects the bus during an under voltage event on the V_{CC} terminal. If V_{CC} enters an under voltage fault condition, the RXD terminal is tri-stated (high impedance) and the device does not pass any signals from the bus, including any remote wake-up events (WUP). If the device is in normal mode and V_{CC} supply is lost, or has a brown out that triggers the UVLO, the device will transition to a protected mode.

The device is designed to be an "ideal passive" or “no load” to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered, so they will not load the bus. This is critical if some nodes of the network will be unpowered while the rest of the of network remains operational. Logic terminals also have low leakage currents when the device is unpowered so they will not load other circuits which may remain powered.

Table 2. TCAN1044x-Q1without V_{IO} Under Voltage Protection

V_{CC}	DEVICE STATE	BUS	RXD
> UV_{VCC}	Operational	Per Operating Mode	Per Operating Mode
< UV_{VCC}	Protected	High Impedance	High Impedance

Once an under voltage condition is cleared and the V_{CC} supply has returned to valid level the device will typically need t_{MODE} to transition to normal operation. The host controller should not attempt to send or receive messages until this transition time has expired. If STB is low and V_{CC} has an under voltage event, the device will go into a protected mode which disables the wake-up receiver and places the RXD output into a high impedance state.

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Table 3. TCAN1044x-Q1 with V_{IO} Under Voltage Protection

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors Bus
< UV_{VCC}	> UV_{VIO}	Protected	High Impedance	High (Recessive)
> UV_{VCC}	< UV_{VIO}	Protected	Recessive	High Impedance
< UV_{VCC}	< UV_{VIO}	Protected	High Impedance	High Impedance

8.3 Device Functional Modes

8.3.1 Operating Modes

The TCAN1044x-Q1 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high level (V_{STB} = V_{CC} or V_{STB} = VIO on devices with V_{IO}) to the STB input terminal.

Table 4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Terminal
High	Low current standby mode with bus wake-up	Disabled	Low power receiver and bus monitor enable	High (Recessive) until wake-up, then filtered mirrors of bus state. See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

8.3.2 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD output.

8.3.3 Standby Mode

This is the low power mode of the device. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request will be output to RXD (driven low) as shown in Figure 14.The local CAN protocol controller should monitor RXD for transitions (high to low) and reactivate the TCAN1044x-Q1 to normal mode by pulling the STB terminal low. The CAN bus terminals are weakly pulled to GND during this mode, see Figure 4.

8.3.4 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN1044x-Q1 offers a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request will be indicated to the controller by a falling edge and low corresponding to a "filtered" dominant on the RXD output of the TCAN1044x-Q1 terminal.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ will always be detected as part of a WUP and thus a wake request will always be generated. See Figure 14 for the timing diagram of the wake-up pattern.

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The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any CAN or CAN FD message to initiate a wake-up request.

ISO 11898-2:2016 has two sets of times for a short and long wake up filter times. The t_{WK_FILTER} timing for the TCAN1044x-Q1 device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back to back bit times at 1 Mbps triggers the filter in either bus state.

For an additional layer of robustness and to prevent false wake ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the part remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 14 for the timing diagram of the wake up pattern with wake timeout feature.

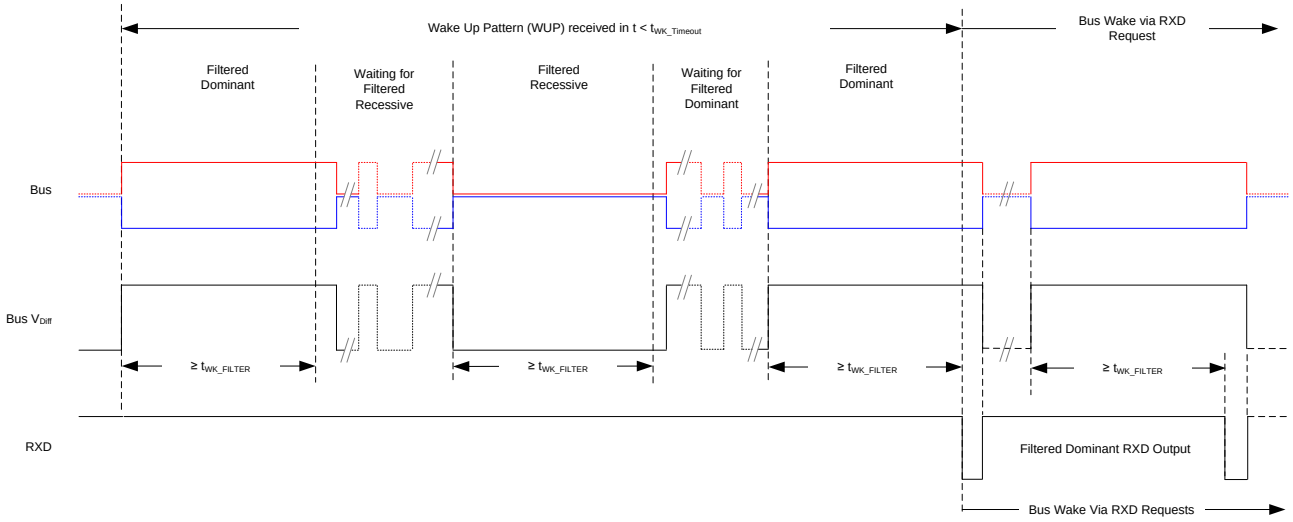

Figure 14. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

8.3.5 Driver and Receiver Function

The digital logic input and output levels for the TCAN1044x-Q1 are CMOS levels with respect to V_{CC} or V_{IO} for compatibility with protocol controllers having 1.8 V to 5 V logic or I/O levels.

Table 5. Driver Function Table

Device Mode	TXD INPUT(1)	BUS OUTPUTS(2)		DRIVEN BUS STATE(3)
		CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Biased recessive
Standby	X	Z	Z	Weak pull down to ground

(1) H = high level, L = low level, X = irrelevant
(2) H = high level, L = low level, Z = high Z receiver bias
(3) For Bus state and bias see Figure 3 and Figure 4

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Table 6. Receiver Function Table Normal and Standby Mode

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD TERMINAL(1)
Normal	$V_{ID} \geq 0.9$ V	Dominant	L
	0.5 V < V_{ID} < 0.9 V	Undefined	Undefined
	$V_{ID} \leq 0.5$ V	Recessive	H
Standby	$V_{ID} \geq 1.15$ V	Dominant	H L if a remote wake event occurred See Figure
	0.4 V < V_{ID} < 1.15 V	Undefined	
	$V_{ID} \leq 0.4$ V	Recessive	
Any	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level

8.3.6 Floating Terminals

The TCAN1044x-Q1 has internal pull-ups on critical terminals to place the device into known states if the terminal floats. See Table 7: Terminal Bias for details on terminal bias conditions.

Table 7. Terminal Bias

TERMINAL	PULL UP or PULL DOWN	COMMENT
TXD	Pull-up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB terminal towards low power standby mode to prevent excessive system power

The internal bias should not be relied upon as only termination, especially in noisy environments but should be considered a failsafe protection. Special care needs to be taken when the device is used with MCUs utilizing open drain outputs. TXD is weakly internally pulled up. The TXD pull up strength and CAN bit timing require special consideration when this device is used with an open drain TXD output on the controller CAN controller. An adequate external pull up resistor must be used to ensure that the TXD output of the CAN controller maintains adequate bit timing input to the CAN transceiver.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

The TCAN1044x-Q1 transceivers are typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. Figure 15 shows a typical application configuration for 5 V controller applications. The bus termination is shown for illustrative purposes.

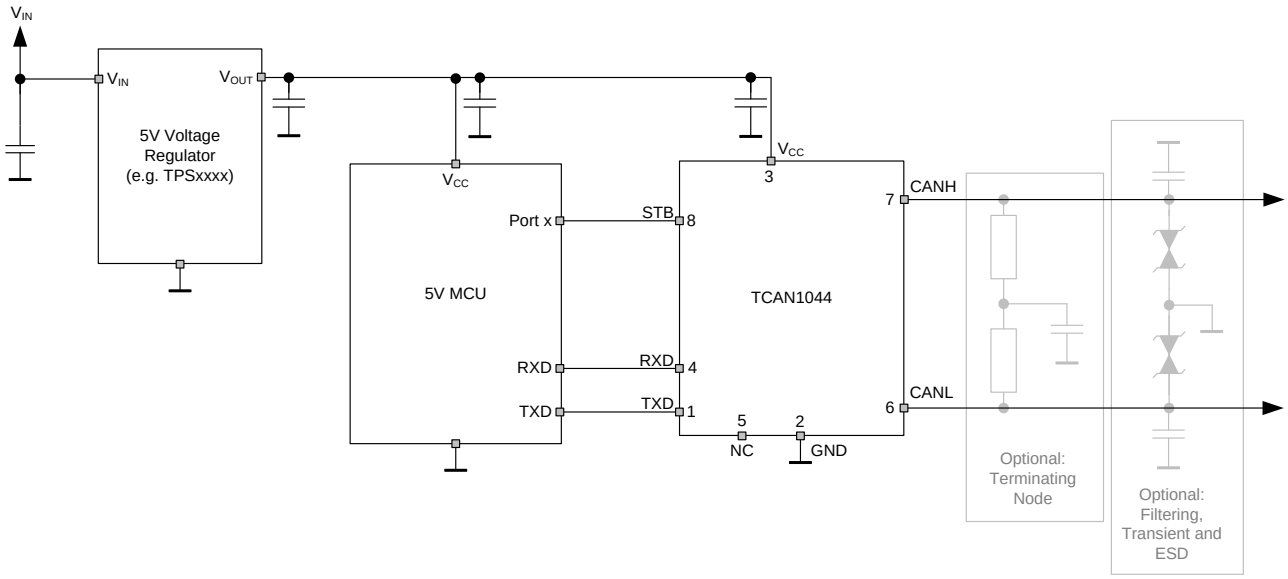

Figure 15. Typical TCAN1044-Q1 Transceiver Application Using 5 V IO Connections

ADVANCE INFORMATION

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 CAN Termination

The ISO 11898-2:2016 standard specifies the interconnection to be a single twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node but is generally not recommended, especially if the node may be removed from the bus. Termination must be carefully placed so that it is not removed from the bus. System level CAN implementations such as CANopen allow for different termination and cabling concepts, for example, to add cable length.

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then split termination may be used, see Figure 16. Split termination improves the electromagnetic emissions behavior of the network by reducing fluctuations in the bus.

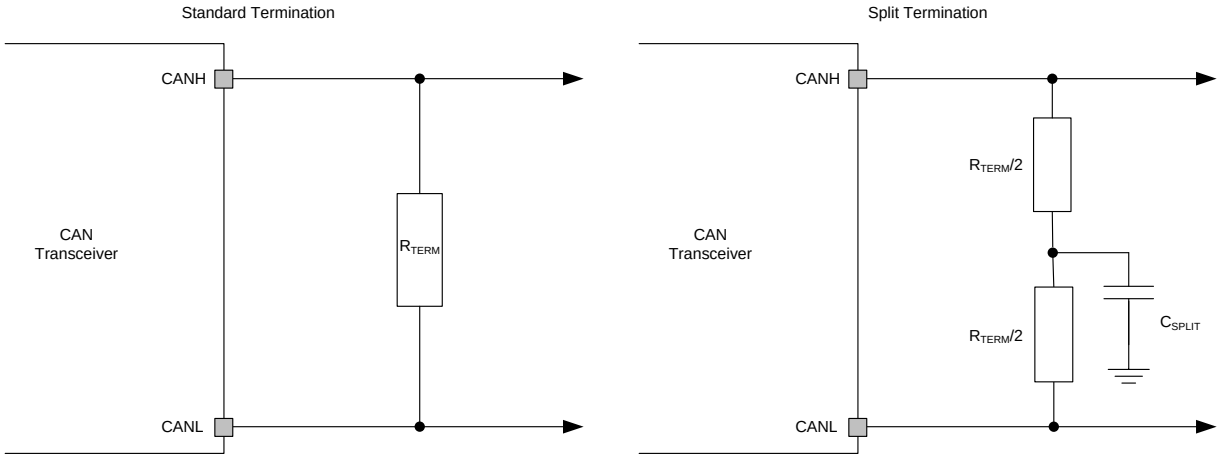

Figure 16. CAN Bus Termination Concepts

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Typical Application (continued)

9.2.2 Detailed Design Procedures

9.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application can have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1044x-Q1 family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1044x-Q1 family is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45Ω bus load. The differential input resistance of the TCAN1044x-Q1 is a minimum of 40 kΩ. If 100 TCAN1044x-Q1 transceivers are in parallel on a bus, this is equivalent to a 400-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of approximately 52 Ω. Therefore, the TCAN1044x-Q1 family theoretically supports over 100 transceivers on a single bus segment. However for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

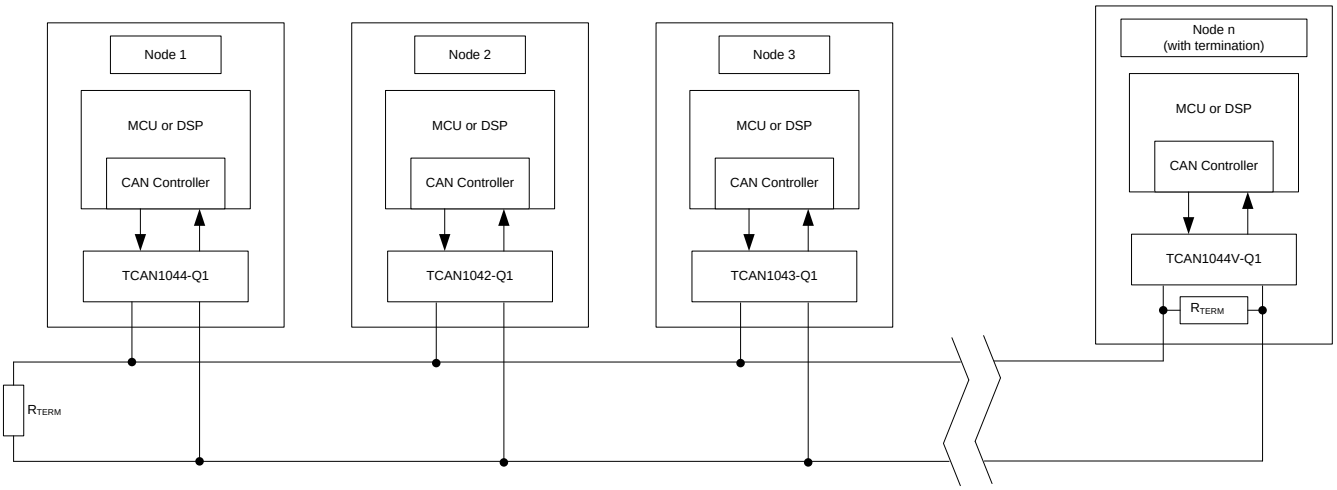

Figure 17. TCAN1044(V)-Q1 Typical CAN Bus

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Typical Application (continued)

9.2.3 Application Curves

Graph Placeholder

Figure 18. TBD

Graph Placeholder

Figure 19. TBD

9.3 System Examples

The TCAN1044x-Q1 CAN transceivers are typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. Typical application configuration for 1.8 V to 3.3 V controller applications are shown in Figure 20. The bus termination is shown for illustrative purposes.

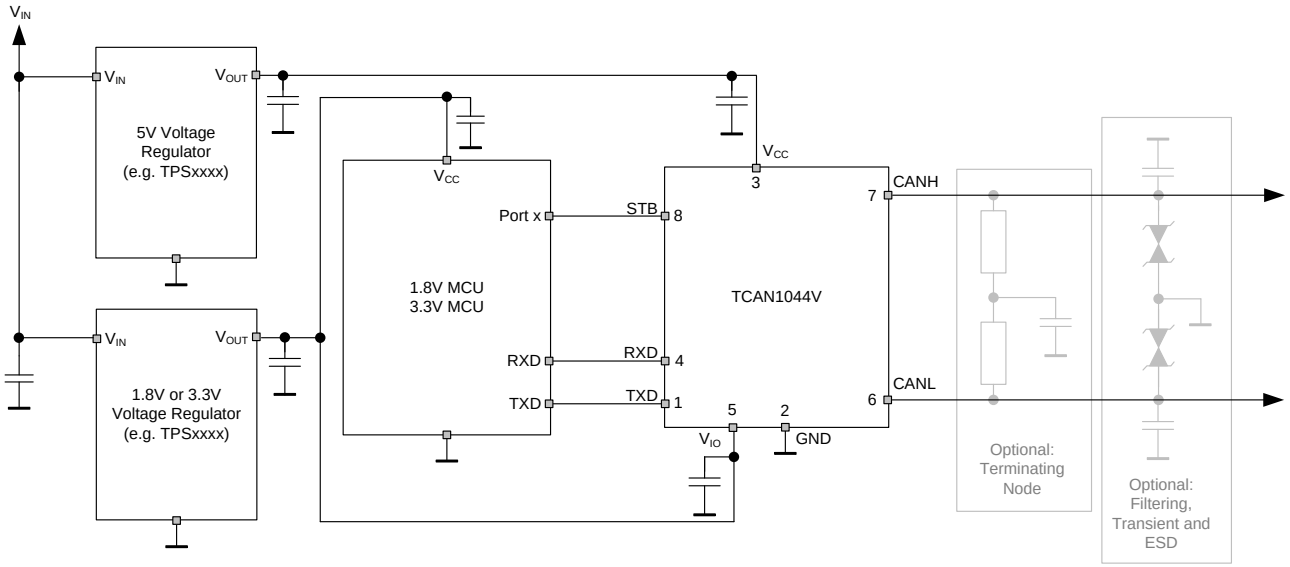

Figure 20. Typical TCAN1044V-Q1 Transceiver Application Using 3.3 V IO Connections

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10 Power Supply Recommendations

The TCAN1044x-Q1 device is designed to operate with a main V_{CC} input voltage supply range between 4.5 V and 5.5 V. The TCAN1044x-Q1 implements an I/O level shifting supply input, V_{IO}, designed for a range between 1.8 V and 5.5 V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100 nF, should be placed near the CAN transceiver's main V_{CC} supply terminal in addition to bypass capacitors. A decoupling capacitance, typically 100 nF, should be placed near the CAN transceiver's V_{IO} supply terminal in addition to bypass capacitors.

11 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

11.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. In this layout example for protection a transient voltage suppression (TVS) device, D1, has been used. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use V_{CC} and ground planes to provide low inductance. Note that high frequency current follows the path of least impedance and not the path of least resistance.
- Bypass and bulk capacitors should be placed as close as possible to the supply terminals V_{CC} and V_{IO} of transceiver.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- This layout example shows how split termination could be implemented on the CAN node. This is where the termination is split into two resistors, R6 and R7, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination. See CAN Termination, CAN Bus Short Circuit Current Limiting and Equation 2 for information on termination concepts and power ratings needed for the termination resistor(s).
- To limit current of digital lines serial resistors may be used. Examples are R2, R3 and R4.
- Terminal 1 is shown for the TXD input of the device with R1 as an optional pull-up resistor. If an open drain host controller is used this is mandatory to ensure the bit timing into the device is met.
- Terminal 8 is shown with R4 assuming the mode terminal STB, is used. If the device is used in normal mode only, R4 is not needed and the pads of C4 could be used for the pull down resistor R5 to GND.

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11.2 Layout Example

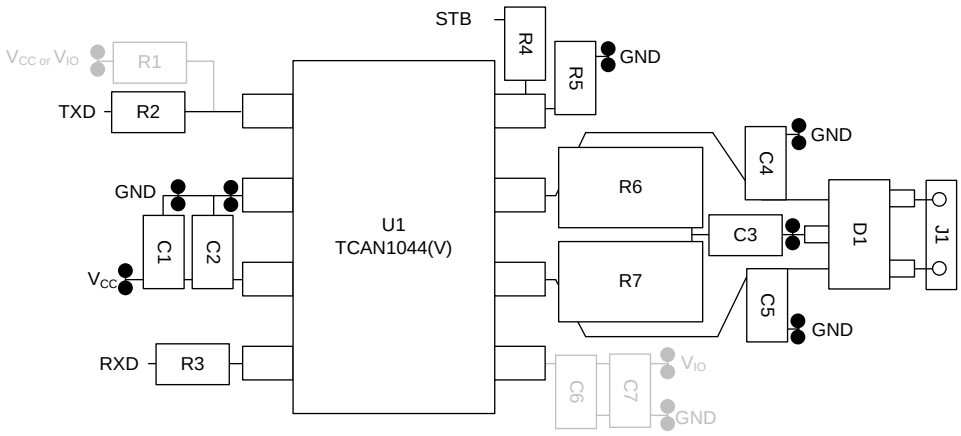


Figure 21. TCAN1044(V)-Q1 Layout Example

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 8. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TCAN1044-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1044V-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTCAN1044DRQ1	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
PTCAN1044VDRQ1	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
TCAN1044DRBQ1	PREVIEW	SON	DRB	8	121	TBD	Call TI	Call TI	-40 to 125		
TCAN1044DRBRQ1	PREVIEW	SON	DRB	8	3000	TBD	Call TI	Call TI	-40 to 125		
TCAN1044DRQ1	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		
TCAN1044VDRBQ1	PREVIEW	SON	DRB	8	121	TBD	Call TI	Call TI	-40 to 125		
TCAN1044VDRBRQ1	PREVIEW	SON	DRB	8	3000	TBD	Call TI	Call TI	-40 to 125		
TCAN1044VDRQ1	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

DRB 8

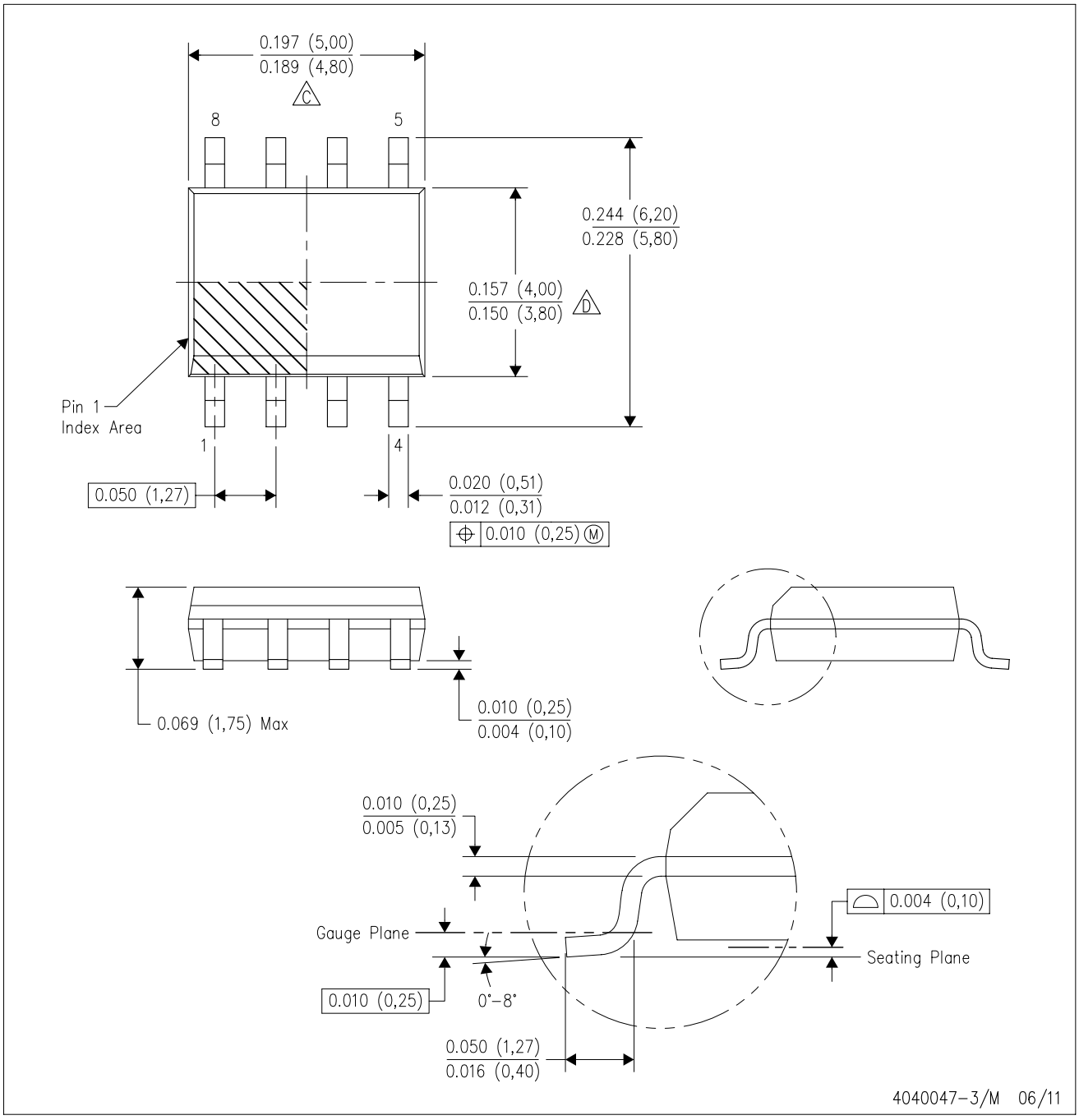
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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