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AK7735A**Dual DSP with 4chADC + 4chDAC + 4chSRC****1. General Description**

The AK7735A is a highly integrated digital signal processor, including a 24-bit stereo ADC with MIC gain amplifiers, a 24-bit stereo ADC with input selector, two 32-bit stereo DACs, 2 stereo sampling rate convertors supporting the sampling frequency up to 192kHz and dual DSPs for Audio process. Each DSP has 3072step/fs (when fs=48kHz) parallel processing power. As the AK7735A is a RAM based DSP, it is freely programmable for user requirements of acoustic effects. The AK7735A is available in a 48-pin LQFP package.

2. Features

- **Dual DSP: (DSP1 and DSP2 have the same specification. Memory areas are shared by them)**
 - Word length: 28-bit (Simple floating point supported)
 - Instruction cycle: Max. 6.8ns (3072fs at fs=48kHz)
 - Multiplier: 24 x 24 → 48-bit (Double precision arithmetic available)
 - Divider: 24 / 24 → 24-bit (Floating point normalization function)
 - ALU: 52-bit Arithmetic Operation (with 4bits overflow margin)
 - Program RAM: 4096-word x 36-bit
 - Coefficient RAM: 6144-word x 24-bit
 - Data RAM: 4096-word x 28-bit
 - Delay RAM: 12288-word x 28-bit
 - JX pins (Interrupt)
 - Independent Power Management Function for DSP1, DSP2
- **ADC1: 24-bit Stereo ADC with MIC Gain Amplifiers**
 - Sampling Frequency: fs = 8kHz ~ 192kHz
 - Channel Independent Analog Gain Amplifiers (0~18dB(2dB Step), 18~36dB(3dB Step))
 - Differential Input or Single-ended Input
 - ADC Characteristics S/N: 106dB (fs=48kHz, Differential Input, MIC Gain=0dB)
 - Channel Independent Digital Volume Control (24dB~-103dB, 0.5dB Step, Mute)
 - Digital HPF for DC Offset Cancelling
 - Low Noise MIC Power Output: 1ch
 - 4 types of Digital Filter for Sound Color Selection
- **ADC2: 24-bit Stereo ADC with Input Selector**
 - Sampling Frequency: fs = 8kHz ~ 192kHz
 - Analog Input Selector: Differential Input x1 or Single-ended Input x2
or Pseudo-differential Input x 1
 - ADC Characteristics S/N: 106dB (fs=48kHz, Differential Input)
 - Channel Independent Digital Volume (24dB ~ -103dB, 0.5dB Step, Mute)
 - Digital HPF for DC Offset Cancelling
 - 4 types of Digital Filter for Sound Color Selection

- **DAC: Advanced 32bit DAC**
 - 2ch x 2
 - Sampling Frequency: $f_s = 8\text{kHz} \sim 192\text{kHz}$
 - Single-ended Output
 - DAC Characteristics S/N: 108dB ($f_s=48\text{kHz}$)
 - Channel Independent Digital Volume Control (12dB ~ -115dB, 0.5dB Step, Mute)
 - 4 types of Digital Filter for Sound Color Selection
- **SRC:**
 - 2ch x 2
 - FSI = 8kHz ~ 192kHz, FSO = 8kHz ~ 192kHz (FSO/FSI = 0.167 ~ 6.0)
- **Digital Interfaces**
 - Digital Input Port x 4 (Max 32ch, in TDM mode)
 - Digital Output Port x 4 (Max 32ch, in TDM mode)
 - Independent LRCK/BICK port x 3
 - Data Format: MSB 32, 24bit / LSB 24, 20, 16bit / I²S
 - PCM Short / Long Frame Supported
 - TDM Format Supported (Max:8ch / 256fs, $f_s=96\text{kHz}$)
- **PLL Circuit**
- **μP Interface: SPI(Max 6MHz) / I²C(400kHz Fast Mode, 1MHz Fast Mode Plus)**
- **Power Supply:**
 - Analog: AVDD: 3.0V ~ 3.6V (Typ. 3.3V)
 - Digital: LVDD: 3.0V ~ 3.6V (Typ. 3.3V) (3.3V → 1.2V regulator integrated)
 - I/F VDD33: 3.0V ~ 3.6V (Typ. 3.3V)
 - TVDD: 1.7V ~ 3.6V (Typ. 3.3V)
- **Operating Temperature Range: $T_a = -40 \sim 85^\circ\text{C}$**
- **Package: 48-pin LQFP (7mm x 7mm, 0.5mm pitch)**

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4. Block Diagrams

■ Block Diagram

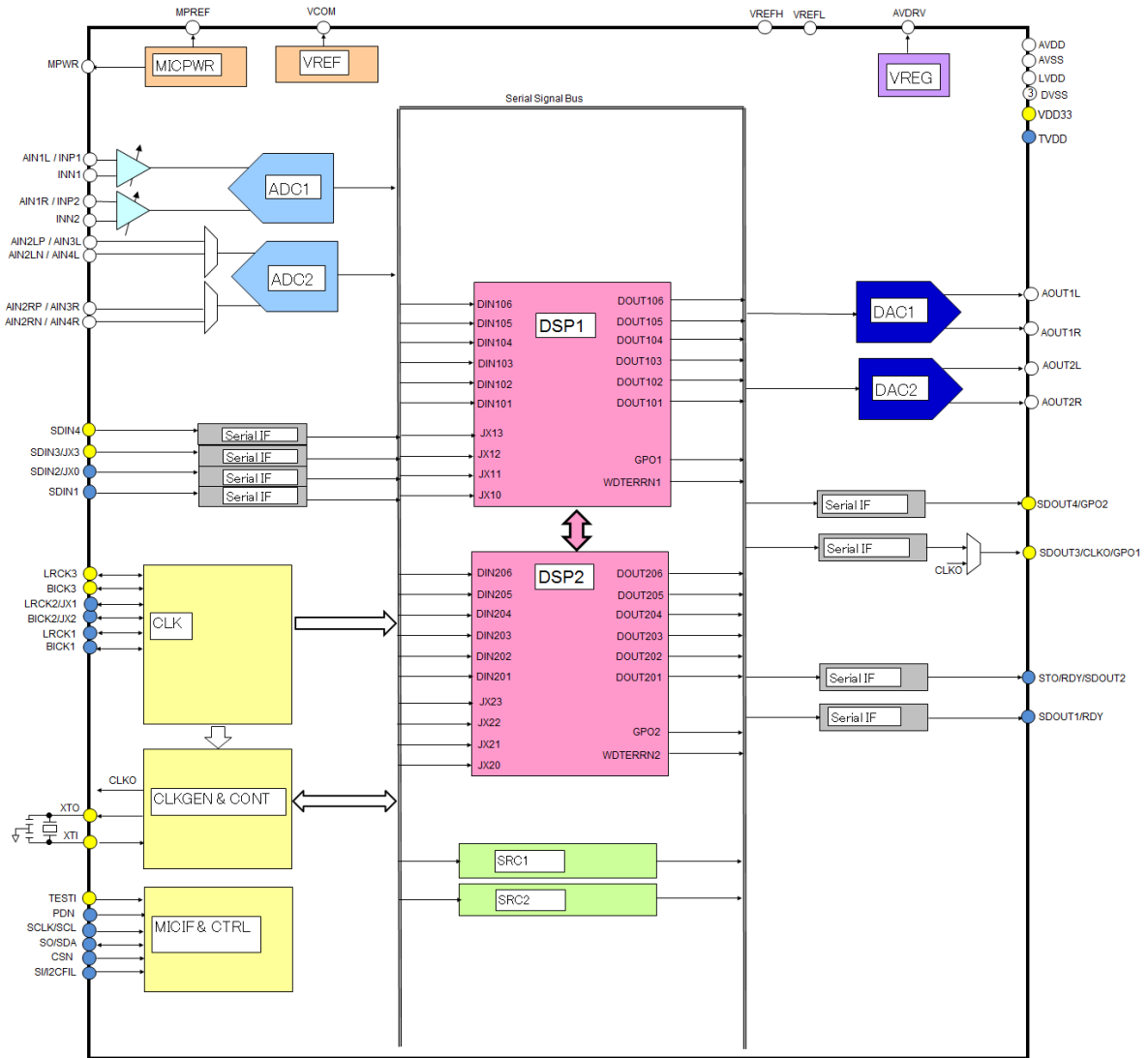


Figure 1. Block Diagram

■ DSP Block Diagram

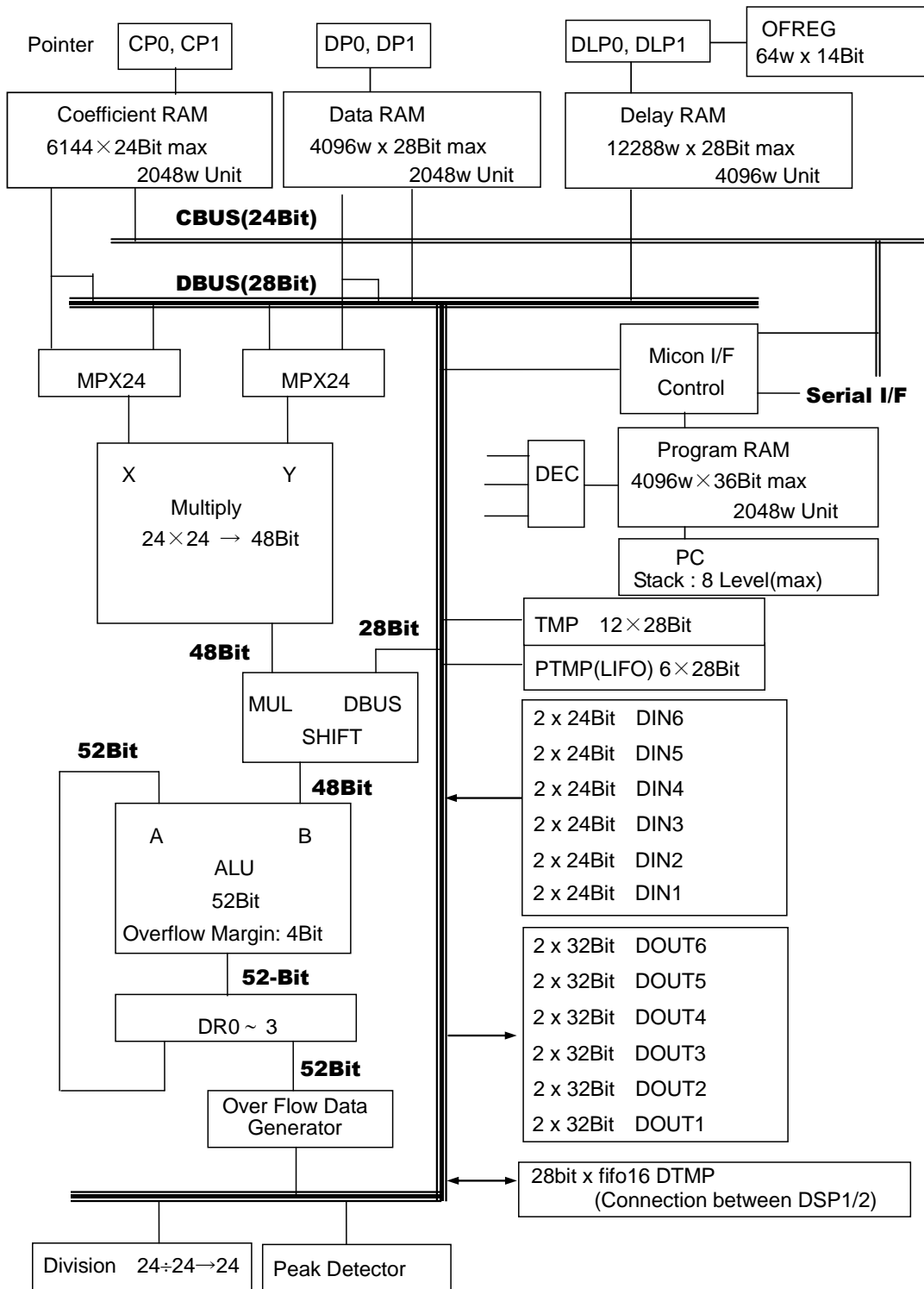


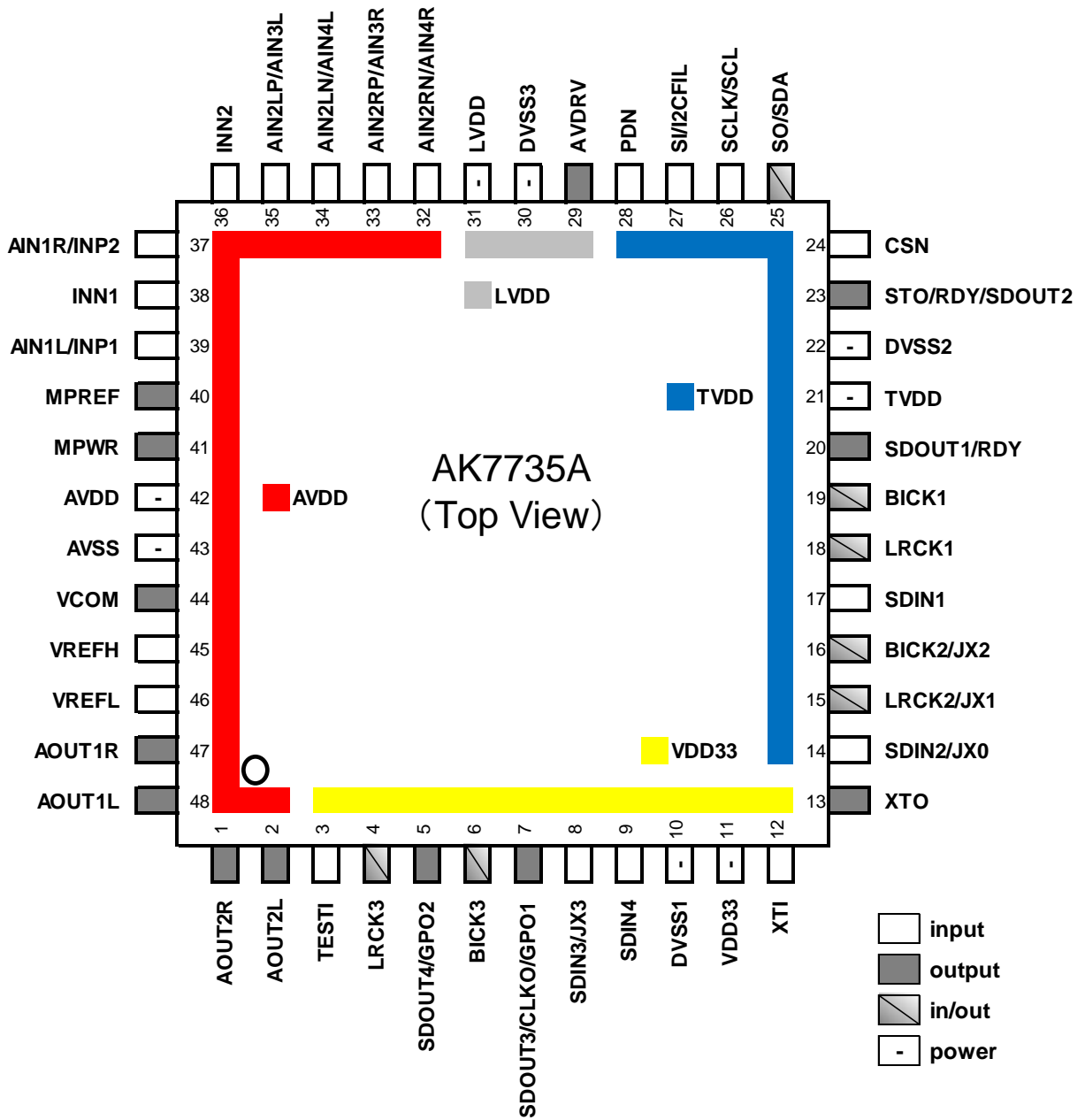
Figure 2. DSP Block Diagram

Note

* 1. Coefficient RAM, Data RAM, Delay RAM, Program RAM areas are shared by DSP1 and DSP2 and the sizes are configurable by control registers.

5. Pin Configurations and Functions

■ Pin Configurations



■ Pin Functions

No.	Pin Name	I/O	Function	Supply Power
1	AOUT2R	O	DAC2 Rch Analog Output Pin This pin outputs "Hi-Z" during power-down state.	AVDD
2	AOUT2L	O	DAC2 Lch Analog Output Pin This pin outputs "Hi-Z" during power-down state.	AVDD
3	TESTI	I	Test Input Pin It must be tied "L".	VDD33
4	LRCK3	I/O	LR Channel Select Clock 3 Pin	VDD33
5	SDOUT4	O	Serial Data Output 4 Pin	VDD33
	GPO2	O	GPO Output 2 Pin (GPO Output of DSP2)	
6	BICK3	I/O	Serial Bit Clock 3 Pin	VDD33
7	SDOUT3	O	Serial Data Output 3 Pin	VDD33
	CLKO	O	Master Clock Output Pin	
	GPO1	O	GPO Output 1 Pin (GPO Output of DSP1)	
8	SDIN3	I	Serial Data Input 3 Pin	VDD33
	JX3	I	External Conditional Jump Input 3 Pin	
9	SDIN4	I	Serial Data Input 4 Pin	VDD33
10	DVSS1	-	Digital Ground 1 Pin 0V	-
11	VDD33	-	Digital I/F Power Supply Pin 3.0~3.6V (typ.3.3V)	-
12	XTI	I	Crystal Oscillator Input Pin When using a crystal oscillator, connect it between XTI and XTO. When not using XTI pin, leave this pin open.	VDD33
13	XTO	O	Crystal Oscillator Output Pin When using a crystal oscillator, connect it between XTI and XTO. When not using a crystal oscillator, leave this pin open.	VDD33
14	SDIN2	I	Serial Data Input 2 Pin	TVDD
	JX0	I	External Conditional Jump Input 0 Pin	
15	LRCK2	I/O	LR Channel Select Clock 1 Pin	TVDD
	JX1	I	External Conditional Jump Input 1 Pin	
16	BICK2	I/O	Serial Bit Clock 2 Pin	TVDD
	JX2	I	External Conditional Jump Input 2 Pin	
17	SDIN1	I	Serial Data Input 1 Pin	TVDD
18	LRCK1	I/O	LR Channel Select Clock 1 Pin	TVDD
19	BICK1	I/O	Serial Bit Clock 1 Pin	TVDD
20	SDOUT1	O	Serial Data Output 1 Pin	TVDD
	RDY	O	RDY Signal Output Pin	
21	TVDD	-	Digital I/F Power Supply Pin 1.7~3.6V (typ.3.3V)	-
22	DVSS2	-	Digital Ground 2 Pin 0V	-

No.	Pin Name	I/O	Function	Supply Power
23	STO	O	Status Output Pin This pin outputs "L" during power-down state.	TVDD
	RDY	O	RDY Signal Output Pin	
	SDOUT2	O	Serial Data Output 2 Pin	
24	CSN	I	SPI Mode SPI I/F Chip Select Pin During power-down state or when SPI I/F is not in use, leave this pin "H" level.	TVDD
		I	I ² C Mode I ² C I/F Chip Address Pin This pin must be pulled up or pulled down.	
25	SO	O	Serial Data Output Pin for SPI I/F This pin outputs "Hi-Z" during power-down state. This pin must be pulled up or pulled down.	TVDD
	SDA	I/O	Serial Data In/Output Pin for I ² C I/F This pin outputs "Hi-Z" during power-down state.	
26	SCLK	I	Serial Data Clock Input Pin for SPI I/F	TVDD
	SCL	I	Serial Data Clock Input Pin for I ² C I/F	
27	SI	I	Serial Data Input Pin for SPI I/F	TVDD
	I2CFIL	I	I ² C I/F Mode Select Input Pin I2CFIL = "L": Fast Mode (400kHz) I2CFIL = "H": Fast Mode Plus (1MHz) (should be fixed to TVDD2)	
28	PDN	I	Power-down Pin Use this pin to power down the AK7735A. The PDN pin should be held "L" when power is supplied.	TVDD
29	AVDRV	O	VREG Output Pin Connect a 2.2μF(±30%) ceramic capacitor between this pin and DVSS3. Do not connect this pin to an external circuit.	LVDD
30	DVSS3	-	Digital Ground 3 Pin 0V	-
31	LVDD	-	Digital Core Power Supply Pin 3.0~3.6V (typ.3.3V)	-

No.	Pin Name	I/O	Function	Supply Power
32	AIN2RN	I	ADC2 Rch Inverted Differential Input 2 Pin ADC2 Rch Pseudo-Differential Ground Input Pin	AVDD
	AIN4R	I	ADC2 Rch Single-ended Input 4 Pin	
33	AIN2RP	I	ADC2 Rch Non-inverted Differential Input 2 Pin ADC2 Rch Pseudo-Differential Signal Input Pin	AVDD
	AIN3R	I	ADC2 Rch Single-ended Input 3 Pin	
34	AIN2LN	I	ADC2 Lch Inverted Differential Input 2 Pin ADC2 Lch Pseudo-Differential Ground Input Pin	AVDD
	AIN4L	I	ADC2 Lch Single-ended Input 4 Pin	
35	AIN2LP	I	ADC2 Lch Non-inverted Differential Input 2 Pin ADC2 Lch Pseudo-Differential Signal Input Pin	AVDD
	AIN3L	I	ADC2 Lch Single-ended Input 3 Pin	
36	INN2	I	ADC1 Rch Inverted Differential Input 2 Pin	AVDD
37	AIN1R	I	ADC1 Rch Single-ended Input 1 Pin	AVDD
	INP2	I	ADC1 Rch Non-inverted Differential Input 2 Pin	
38	INN1	I	ADC1 Lch Inverted Differential Input 1 Pin	AVDD
39	AIN1L	I	ADC1 Lch Single-ended Input 1 Pin	AVDD
	INP1	I	ADC1 Lch Non-inverted Differential Input 1 Pin	
40	MPREF	O	Ripple Filter Pin for Microphone Power Supply Connect a 1 μ F ceramic capacitor between this pin and AVSS. Do not connect this pin to an external circuit.	AVDD
41	MPWR	O	Power Supply Output Pin for Microphone This pin outputs "Hi-Z" during power-down state.	AVDD
42	AVDD	-	Analog Power Supply Pin 3.0~3.6V (typ.3.3V)	-
43	AVSS	-	Analog Ground Pin 0V	-
44	VCOM	O	Analog Common Voltage Output Pin Connect a 2.2 μ F ceramic capacitor between this pin and AVSS. Do not connect this pin to an external circuit. This pin outputs "L" during power-down state.	AVDD
45	VREFH	I	Analog High-level Reference Voltage Input Pin Connect this pin to AVDD.	AVDD
46	VREFL	I	Analog Low-level Reference Voltage Input Pin Connect this pin to AVSS.	AVDD
47	AOUT1R	O	DAC1 Rch Analog Output Pin This pin outputs "Hi-Z" during power-down state.	AVDD
48	AOUT1L	O	DAC1 Lch Analog Output Pin This pin outputs "Hi-Z" during power-down state.	AVDD

■ Handling of Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	MPREF, MPWR, AIN1L/INP1, INN1, AIN1R/INP2, INN2, AIN2LP/AIN3L, AIN2LN/AIN4L, AIN2RP/AIN3R, AIN2RN/AIN4R, AOUT1L, AOUT1R, AOUT2L, AOUT2R	Open
Digital	XTI, XTO, SDOUT1/RDY, STO/RDY/SDOUT2, SDOUT3/CLKO/GPO1, SDOUT4/GPO2	Open
	SDIN4, SDIN3/JX3, SDIN2/JX0, SDIN1, LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, LRCK3, BICK3, TESTI	Connect to DVSS1/DVSS2

Table 1. Handling of Unused Pins

■ Internal Pulled-down Pins Status

No.	Pin Name	Power Down Status PDN pin = "L"	Power Down Release PDN pin = "H" (Slave mode)	Power Down Release PDN pin = "H" (Master mode)
3	TESTI	Pulled-down (25kΩ)	Pulled-down (25kΩ)	Pulled-down (25kΩ)
18	LRCK1	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
19	BICK1	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
15	LRCK2/JX1	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
16	BICK2/JX2	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
4	LRCK3	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
6	BICK3	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
20	SDOUT1/RDY	Pulled-down (50kΩ)	Output	Output
23	STO/RDY/SDOUT2	Pulled-down (50kΩ)	Output	Output
7	SDOUT3/CLKO/GPO1	Pulled-down (50kΩ)	Output	Output
5	SDOUT4/GPO2	Pulled-down (50kΩ)	Output	Output
29	AVDRV	Pulled-down (70Ω)	Output	Output

Table 2. Internal Pulled-down Pins Status

Note

* 2. Typical resistance value when LVDD=TVDD=VDD33=3.3V.

■ Power-down Status of Output Pins

No	Pin Name	I/O	Power-down Status	No	Pin Name	I/O	Power-down Status
44	VCOM	O	"L" Output	4	LRCK3	I/O	Input
40	MPREF	O	"L" Output	6	BICK3	I/O	Input
41	MPWR	O	"Hi-Z" Output	25	SO/SDA	I/O	"Hi-Z" Output
48	AOUT1L	O	"Hi-Z" Output	20	SDOUT1/RDY	O	"L" Output (Pulled-down)
47	AOUT1R	O	"Hi-Z" Output	23	STO/RDY/SDOUT2	O	"L" Output (Pulled-down)
2	AOUT2L	O	"Hi-Z" Output	7	SDOUT3/CLKO/GPO1	O	"L" Output (Pulled-down)
1	AOUT2R	O	"Hi-Z" Output	5	SDOUT4/GPO2	O	"L" Output (Pulled-down)
18	LRCK1	I/O	Input	13	XTO	O	"Hi-Z" Output
19	BICK1	I/O	Input	29	AVDRV	O	"L" Output (Pulled-down)
15	LRCK2/JX1	I/O	Input				
16	BICK2/JX2	I/O	Input				

Table 3. Power-down Status of Output Pins

6. Absolute Maximum Ratings

(AVSS=DVSS1=DVSS2=DVSS3=0V * 3)

Parameter	Symbol	Min.	Max.	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital1(Core)	LVDD	-0.3	4.3	V
Digital2(I/F)	TVDD	-0.3	4.3	V
Digital3(I/F)	VDD33	-0.3	4.3	V
Difference (AVSS, DVSS1, DVSS2, DVSS3) * 3	Δ GND	-0.3	0.3	V
Input Current (except power supply pins)	IIN	—	\pm 10	mA
Analog Input Voltage * 4	VINA	-0.3	(AVDD+0.3) or 4.3	V
Digital Input Voltage * 5	VIND1	-0.3	(TVDD+0.3) or 4.3	V
Digital Input Voltage * 6	VIND2	-0.3	(VDD33+0.3) or 4.3	V
Ambient Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Notes

- * 3. All voltages are with respect to ground. AVSS and DVSS1-3 must be connected to the same ground.
- * 4. The maximum analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
- * 5. The maximum digital input voltage of SDIN1, SDIN2/JX0, LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, PDN, SCLK/SCL, CSN and SI/I2CFIL pins is smaller value between (TVDD+0.3)V and 4.3V.
- * 6. The maximum digital input voltage of SDIN3/JX3, SDIN4, LRCK3, BICK3, TEST1 and XT1 pins is smaller value between (VDD33+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS1=DVSS2=DVSS3=0V * 3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supplies					
Analog	AVDD	3.0	3.3	3.6	V
Digital1(Core)	LVDD	3.0	3.3	3.6	V
Digital2(I/F)	TVDD	1.7	3.3	3.6	V
Digital3(I/F)	VDD33	3.0	3.3	3.6	V
Difference1	AVDD – LVDD	-0.1	0	0.1	V
Difference2	AVDD – VDD33	-0.1	0	0.1	V
Difference3	LVDD – VDD33	-0.1	0	0.1	V
Difference4	LVDD – TVDD	-0.1	-	-	V

Notes

- * 7. The power-up sequence with AVDD, DVDD, TVDD and VDD33 is not critical. The PDN pin should be held “L” when power is supplied. The PDN pin is allowed to be “H” after all power supplies are applied and settled.
- * 8. Do not turn off the power supply of the AK7735A with the power supply of the peripheral device turned on. When using the I²C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD or less voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

■ Analog Characteristics

1. MIC AMP

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V;
ADC1VL/R bits="0")

Parameter		Min.	Typ.	Max.	Unit	
MIC AMP	Input Impedance	14	20	26	kΩ	
	Gain	MGNL[3:0]bits=0x0, MGNR[3:0]bits=0x0	-1	0	1	dB
		MGNL[3:0]bits=0x1, MGNR[3:0]bits=0x1	1	2	3	
		MGNL[3:0]bits=0x2, MGNR[3:0]bits=0x2	3	4	5	
		MGNL[3:0]bits=0x3, MGNR[3:0]bits=0x3	5	6	7	
		MGNL[3:0]bits=0x4, MGNR[3:0]bits=0x4	7	8	9	
		MGNL[3:0]bits=0x5, MGNR[3:0]bits=0x5	9	10	11	
		MGNL[3:0]bits=0x6, MGNR[3:0]bits=0x6	11	12	13	
		MGNL[3:0]bits=0x7, MGNR[3:0]bits=0x7	13	14	15	
		MGNL[3:0]bits=0x8, MGNR[3:0]bits=0x8	15	16	17	
		MGNL[3:0]bits=0x9, MGNR[3:0]bits=0x9	17	18	19	
		MGNL[3:0]bits=0xA, MGNR[3:0]bits=0xA	20	21	22	
		MGNL[3:0]bits=0xB, MGNR[3:0]bits=0xB	23	24	25	
		MGNL[3:0]bits=0xC, MGNR[3:0]bits=0xC	26	27	28	
		MGNL[3:0]bits=0xD, MGNR[3:0]bits=0xD	29	30	31	
		MGNL[3:0]bits=0xE, MGNR[3:0]bits=0xE	32	33	34	
MGNL[3:0]bits=0xF, MGNR[3:0]bits=0xF	35	36	37			

2. MIC Bias Output

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V;
Measurement Frequency =20Hz~20kHz)

Parameter		Min.	Typ.	Max.	Unit
MIC Bias	Output Voltage * 9	2.3	2.5	2.7	V
	Load Resistance	2	-	-	kΩ
	Load Capaitance	-	-	30	pF
	Output Noise (A-weighted)	-	-114	-108	dBV

Note

* 9. Output voltage is proportional to AVDD (0.76 x AVDD).

3. MIC AMP + ADC1

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V; Signal Frequency =1kHz; 24bit Data; BICK=64fs; @fs=48kHz, Measurement Frequency BW=20Hz ~ 20kHz; @fs=96kHz,192kHz, BW=20Hz ~ 40kHz; ADC1VL/R bits="0"; MGNL/R[3:0] bits=0x0(0dB); Differential Input, Unless otherwise specified.)

Parameter		Min.	Typ.	Max.	Unit
Resolution		-	-	24	Bit
Input Full Scale Voltage * 10	Differential Input * 13	±2.1	±2.3	±2.5	Vpp
	Differential Input * 14	±0.264	±0.290	±0.315	
	Differential Input * 15	±2.55	±2.83	±3.11	
Input Full Scale Voltage * 11	Single-ended Input * 13	2.1	2.3	2.5	Vpp
	Single-ended Input * 14	0.264	0.290	0.315	
	Single-ended Input * 15	2.55	2.83	3.11	
S/(N+D) (-1dBFS)	fs=48kHz * 13	85	95	-	dB
	fs=48kHz * 14	-	87	-	
	fs=96kHz * 13	-	92	-	
	fs=96kHz * 14	-	84	-	
	fs=192kHz * 13	-	92	-	
	fs=192kHz * 14	-	84	-	
Dynamic Range (-60dBFS)	fs=48kHz (A-weighted) * 13	98	106	-	dB
	fs=48kHz (A-weighted) * 14	-	95	-	
	fs=96kHz * 13	-	99	-	
	fs=96kHz * 14	-	89	-	
	fs=192kHz * 13	-	99	-	
	fs=192kHz * 14	-	89	-	
S/N	fs=48kHz (A-weighted) * 13	98	106	-	dB
	fs=48kHz (A-weighted) * 14	-	95	-	
	fs=96kHz * 13	-	99	-	
	fs=96kHz * 14	-	89	-	
	fs=192kHz * 13	-	99	-	
	fs=192kHz * 14	-	89	-	
Inter-Channel Isolation * 12		90	105	-	dB
Channel Gain Mismatch		-	0.0	0.3	dB
CMRR * 16		60	80	-	dB

Notes

- * 10. INP1, INN1, INP2 and INN2 pins. When using differential input mode, it is prohibited to input signal to only one side like pseudo differential input.
- * 11. AIN1L and AIN1R pins.
- * 12. Inter-channel isolation with -1dBFS signal input.
- * 13. ADC1VL/R bits = "0", MGNL/R[3:0] bits = 0x0(0dB). Input full-scale voltage is proportional to AVDD (0.7 x AVDD).
- * 14. ADC1VL/R bits = "0", MGNL/R[3:0] bits = 0x9(+18dB). Input full-scale voltage is proportional to AVDD (0.088 x AVDD).
- * 15. ADC1VL/R bits = "1", MGNL/R[3:0] bits = 0x0(0dB). Input full-scale voltage is proportional to AVDD (0.86 x AVDD).
- * 16. Common mode rejection ratio when inputting 1kHz, 100mVpp sine wave to both differential inputs. The value refers to the case when inputting a 1kHz, ±100mVpp sine wave as differential input.

4. ADC2

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V; Signal Frequency =1kHz; 24bit Data; BICK=64fs; @fs=48kHz, Measurement Frequency BW=20Hz ~ 20kHz; @fs=96kHz,192kHz, BW=20Hz ~ 40kHz; ADC2VL/R bits="0"; Differential Input, Unless otherwise specified.)

Parameter		Min.	Typ.	Max.	Unit
Resolution		-	-	24	bit
Input Impedance		14	20	26	kΩ
Input Full Scale Voltage * 17	Differential Input * 19	±2.1	±2.3	±2.5	Vpp
	Differential Input * 20	±2.55	±2.83	±3.11	
Input Full Scale Voltage * 18	Single-ended Input * 19	2.1	2.3	2.5	Vpp
	Pseudo-differential Input * 20	2.55	2.83	3.11	
S/(N+D) (-1dBFS)	fs=48kHz	85	95	-	dB
	fs=96kHz	-	92	-	
	fs=192kHz	-	92	-	
Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	98	106	-	dB
	fs=96kHz	-	99	-	
	fs=192kHz	-	99	-	
S/N	fs=48kHz (A-weighted)	98	106	-	dB
	fs=96kHz	-	99	-	
	fs=192kHz	-	99	-	
Inter-Channel Isolation * 12		90	105	-	dB
Channel Gain Mismatch		-	0.0	0.3	dB
CMRR (Differential Input) * 16		60	80	-	dB
CMRR (Pseudo-differential Input) * 21		55	75	-	dB

Notes

- * 17. AIN2LP, AIN2LN, AIN2RP and AIN2RN pins.
- * 18. AIN3L, AIN3R, AIN4L, AIN4R pins and AIN2LP, AIN2RP pins when AD2PSDE bit = "1".
- * 19. ADC2VL/R bits = "0". Input full-scale voltage is proportional to AVDD (0.7 x AVDD).
- * 20. ADC2VL/R bits = "1". Input full-scale voltage is proportional to AVDD (0.86 x AVDD).
- * 21. Common mode rejection ratio when inputting 1kHz, 100mVpp sine wave to both pseudo-differential signal input and ground inputs. The value refers to the case when inputting a 1kHz, 100mVpp sine wave as pseudo-differential input.

5. DAC

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V; Signal Frequency =1kHz; 32bit Data; BICK=64fs; @fs=48kHz, Measurement Frequency BW=20Hz ~ 20kHz; @fs=96kHz,192kHz, Measurement Frequency BW=20Hz ~ 40kHz)

Parameter		Min.	Typ.	Max.	Unit
Resolution		-	-	32	bit
Output Voltage * 22		2.55	2.83	3.11	Vpp
S/(N+D) (0dBFS)	fs=48kHz	80	91	-	dB
	fs=96kHz	-	89	-	
	fs=192kHz	-	89	-	
Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	100	108	-	dB
	fs=96kHz	-	101	-	
	fs=192kHz	-	101	-	
S/N	fs=48kHz (A-weighted)	100	108	-	dB
	fs=96kHz	-	101	-	
	fs=192kHz	-	101	-	
Inter-Channel Isolation (fin=1kHz) * 23		90	110	-	dB
Channel Gain Mismatch		-	0.0	0.7	dB
Load Resistance * 24		10	-	-	kΩ
Load Capaitance		-	-	30	pF

Notes

- * 22. The output voltage when 0dBFS signal input. The output voltage is proportional to AVDD (0.86 x AVDD).
- * 23. Inter-channel isolation between each DAC of Lch and Rch with 0dBFS signal input. (AOUT1L and AOUT1R, and AOUT2L and AOUT2R)
- * 24. to AC load

6. SRC

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V; Signal Frequency =1kHz; 24bit Data; Measurement Frequency BW=20Hz ~ FSO/2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Resolution		-	-	24	bit
Input Sample Rate	FSI	8	-	192	kHz
Output Sample Rate	FSO	8	-	192	kHz
THD+N (Input=1kHz, 0dBFS)					
Audio Mode (SRCFAUD bit = "1", SRCFEC bit = "0")					
FSO/FSI=192kHz/48kHz		-	-122	-	dB
FSO/FSI=44.1kHz/48kHz		-	-125	-	dB
FSO/FSI=48kHz/88.2kHz		-	-122	-	dB
FSO/FSI=48kHz/96kHz		-	-133	-	dB
FSO/FSI=44.1kHz/96kHz		-	-116	-	dB
FSO/FSI=48kHz/192kHz		-	-133	-	dB
FSO/FSI=8kHz/48kHz		-	-130	-	dB
Voice Mode (SRCFAUD bit = "0", SRCFEC bit = "0")					
FSO/FSI=24kHz/32kHz		-	-95	-	dB
FSO/FSI=16kHz/24kHz		-	-98	-	dB
FSO/FSI=24kHz/44.1kHz		-	-78	-	dB
FSO/FSI=16kHz/44.1kHz		-	-69	-	dB
FSO/FSI=8kHz/32kHz		-	-130	-	dB
Dynamic Range (Input=1kHz, -60dBFS)					
Audio Mode (SRCFAUD bit = "1", SRCFEC bit = "0")					
FSO/FSI=192kHz/48kHz		-	132	-	dB
FSO/FSI=44.1kHz/48kHz		-	136	-	dB
FSO/FSI=48kHz/88.2kHz		-	136	-	dB
FSO/FSI=48kHz/96kHz		-	135	-	dB
FSO/FSI=44.1kHz/96kHz		-	136	-	dB
FSO/FSI=48kHz/192kHz		-	136	-	dB
FSO/FSI=8kHz/48kHz		-	130	-	dB
Voice Mode (SRCFAUD bit = "0", SRCFEC bit = "0")					
FSO/FSI=24kHz/32kHz		-	134	-	dB
FSO/FSI=16kHz/24kHz		-	137	-	dB
FSO/FSI=24kHz/44.1kHz		-	132	-	dB
FSO/FSI=16kHz/44.1kHz		-	128	-	dB
FSO/FSI=8kHz/32kHz		-	130	-	dB
Dynamic Range (Input=1kHz, -60dBFS, A-weighted) FSO/FSI=44.1kHz/48kHz		-	137	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	0.167	-	6	

■ Power Consumption

(Ta=25°C; AVDD=LVDD=VDD33=3.0~3.6V(Typ=3.3V, Max=3.6V); TVDD=1.7~3.6V(Typ=3.3V, Max=3.6V); AVSS=DVSS1=DVSS2=DVSS3=0V; fs=192kHz; BICK=64fs; Master Mode; SDOUT1~4/LRCK1~3/BICK1~3=Output; CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Up * 25 (PDN pin = "H")	AVDD	-	23	33	mA
	LVDD	-	55	98	mA
	TVDD	-	4	6	mA
	VDD33	-	5	8	mA
Power-Down (PDN pin = "L")	AVDD	-	0.01	-	mA
	LVDD	-	0.01	-	mA
	TVDD	-	0.01	-	mA
	VDD33	-	0.01	-	mA

Note

* 25. The current of LVDD changes depending on the system frequency and contents of DSP program.

9. Digital Filter Characteristics
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■ **ADC Block**

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

1. Sharp Roll-Off Filter (ADSD bit = "0", ADSL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 26	0dB ~ -0.06dB	PB	0	-	22.1	kHz
	-3.0dB	PB	-	23.7	-	kHz
Stopband * 26		SB	27.8	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~20kHz		ΔGD	-	0	-	1/fs
Group Delay * 27		GD	-	20	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	0.9	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 26	0dB ~ -0.06dB	PB	0	-	44.2	kHz
	-3.0dB	PB	-	47.5	-	kHz
Stopband * 26		SB	55.6	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~40kHz		ΔGD	-	0	-	1/fs
Group Delay * 27		GD	-	20	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 26	0dB ~ -0.04dB	PB	0	-	83.7	kHz
	-3.0dB	PB	-	96.0	-	kHz
Stopband * 26		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~40kHz		ΔGD	-	0	-	1/fs
Group Delay * 27		GD	-	16	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.8	-	Hz

2. Slow Roll-Off Filter (ADSD bit = "0", ADSL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 26	0dB ~ -0.074dB	PB	0	-	12.5	kHz
	-3.0dB	PB	-	19.2	-	kHz
Stopband * 26		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~20kHz		Δ GD	-	0	-	1/fs
Group Delay * 27		GD	-	8	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	0.9	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 26	0dB ~ -0.074dB	PB	0	-	25	kHz
	-3.0dB	PB	-	38.5	-	kHz
Stopband * 26		SB	73.0	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~40kHz		Δ GD	-	0	-	1/fs
Group Delay * 27		GD	-	8	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 26	0dB ~ -0.1dB	PB	0	-	31.1	kHz
	-3.0dB	PB	-	62.3	-	kHz
Stopband * 26		SB	145.9	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~40kHz		Δ GD	-	0	-	1/fs
Group Delay * 27		GD	-	9	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.8	-	Hz

3. Short Delay Sharp Roll-Off Filter (ADSD bit = "1", ADSL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 26	0dB ~ -0.06dB	PB	0	-	22.1	kHz
	-3.0dB	PB	-	23.7	-	kHz
Stopband * 26		SB	27.8	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~20kHz		Δ GD	-	-	2.6	1/fs
Group Delay * 27		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	0.9	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 26	0dB ~ -0.06dB	PB	0	-	44.2	kHz
	-3.0dB	PB	-	47.5	-	kHz
Stopband * 26		SB	55.6	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~40kHz		Δ GD	-	-	2.6	1/fs
Group Delay * 27		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 26	0dB ~ -0.04dB	PB	0	-	83.7	kHz
	-3.0dB	PB	-	96.0	-	kHz
Stopband * 26		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~40kHz		Δ GD	-	-	0.2	1/fs
Group Delay * 27		GD	-	7	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.8	-	Hz

4. Short Delay Slow Roll-Off Filter (ADSD bit = "1", ADSL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 26	0dB ~ -0.074dB	PB	0	-	12.5	kHz
	-3.0dB	PB	-	19.2	-	kHz
Stopband * 26		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~20kHz		Δ GD	-	-	2.6	1/fs
Group Delay * 27		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	0.9	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 26	0dB ~ -0.074dB	PB	0	-	25	kHz
	-3.0dB	PB	-	38.5	-	kHz
Stopband * 26		SB	73.0	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~40kHz		Δ GD	-	-	2.6	1/fs
Group Delay * 27		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 26	0dB ~ -0.1dB	PB	0	-	31.1	kHz
	-3.0dB	PB	-	63.2	-	kHz
Stopband * 26		SB	145.9	-	-	kHz
Stopband Attenuation		SA	85.0	-	-	dB
Group Delay Distortion : 0Hz~40kHz		Δ GD	-	-	0.5	1/fs
Group Delay * 27		GD	-	7	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.8	-	Hz

Notes

- * 26. The passband and stopband frequencies are proportional to fs (sampling rate). High-pass filter characteristics are not included. A reference value of each gain amplitude is the maximum value of frequency response.
- * 27. Delay time caused by the digital filter calculation. This time is measured from an analog signal input until 24-bit data of both channels are set into the output register. It includes group delay by HPF.

■ DAC Block

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

1. Sharp Roll-Off Filter (DASD bit = "0", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 28	±0.05dB	PB	0	-	21.7	kHz
	-3.0dB	PB	-	23.4	-	kHz
Passband Ripple * 29		PR	-0.0032	-	0.0032	dB
Stopband * 28		SB	26.3	-	-	kHz
Stopband Attenuation * 31, * 32		SA	80.0	-	-	dB
Group Delay * 30		GD	-	27.3	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 20kHz			-0.3	-	0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 28	±0.05dB	PB	0	-	43.5	kHz
	-3.0dB	PB	-	46.8	-	kHz
Passband Ripple * 29		PR	-0.0032	-	0.0032	dB
Stopband * 28		SB	52.5	-	-	kHz
Stopband Attenuation * 31, * 32		SA	80.0	-	-	dB
Group Delay * 30		GD	-	27.3	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 40kHz			-0.5	-	0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 28	±0.05dB	PB	0	-	87.0	kHz
	-3.0dB	PB	-	93.6	-	kHz
Passband Ripple * 29		PR	-0.0032	-	0.0032	dB
Stopband * 28		SB	105.0	-	-	kHz
Stopband Attenuation * 31, * 32		SA	80.0	-	-	dB
Group Delay * 30		GD	-	27.3	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 80kHz			-1.9	-	0.1	dB

Notes

- * 28. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB = 0.4535 × fs, SB = 0.546 × fs"
- * 29. Pass-band gain amplitude of double over sampling filter at the first step of Interpolator.
- * 30. Delay time caused by the digital filter calculation. This time is measured from setting of the 16/20/24/32-bit impulse data to the input registers to output of the analog peak signal.
- * 31. The output level with a 1kHz, 0dB sine wave input is defined as 0dB.
- * 32. Band width of Stopband Attenuation ranges from 0Hz to fs.

2. Slow Roll-Off Filter (DASD bit = "0", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 33	±0.05dB	PB	0	-	8.8	kHz
	-3.0dB	PB	-	19.8	-	kHz
Passband Ripple * 29		PR	-0.043	-	0.043	dB
Stopband * 33		SB	42.7	-	-	kHz
Stopband Attenuation * 31, * 32		SA	73.0	-	-	dB
Group Delay * 30		GD	-	6.8	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 20kHz			-5.0	-	0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 33	±0.05dB	PB	0	-	17.7	kHz
	-3.0dB	PB	-	39.5	-	kHz
Passband Ripple * 29		PR	-0.043	-	0.043	dB
Stopband * 33		SB	85.3	-	-	kHz
Stopband Attenuation * 31, * 32		SA	73.0	-	-	dB
Group Delay * 30		GD	-	6.8	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 40kHz			-5.2	-	0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 33	±0.05dB	PB	0	-	35.5	kHz
	-3.0dB	PB	-	79.0	-	kHz
Passband Ripple * 29		PR	-0.043	-	0.043	dB
Stopband * 33		SB	171.0	-	-	kHz
Stopband Attenuation * 31, * 32		SA	73.0	-	-	dB
Group Delay * 30		GD	-	6.8	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 80kHz			-5.9	-	0.1	dB

Note

* 33. The passband and stopband frequencies are proportional to fs (sampling rate).

"PB = 0.185 × fs, SB = 0.888 × fs"

3. Short Delay Sharp Roll-Off Filter (DASD bit = "1", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 28	±0.05dB	PB	0	-	21.7	kHz
	-3.0dB	PB	-	23.4	-	kHz
Passband Ripple * 29		PR	-0.0031	-	0.0031	dB
Stopband * 28		SB	26.3	-	-	kHz
Stopband Attenuation * 31, * 32		SA	80.0	-	-	dB
Group Delay * 30		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 20kHz			-0.3	-	0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 28	±0.05dB	PB	0	-	43.5	kHz
	-3.0dB	PB	-	46.8	-	kHz
Passband Ripple * 29		PR	-0.0031	-	0.0031	dB
Stopband * 28		SB	52.5	-	-	kHz
Stopband Attenuation * 31, * 32		SA	80.0	-	-	dB
Group Delay * 30		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 40kHz			-0.5	-	0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 28	±0.05dB	PB	0	-	87.0	kHz
	-3.0dB	PB	-	93.6	-	kHz
Passband Ripple * 29		PR	-0.0031	-	0.0031	dB
Stopband * 28		SB	105.0	-	-	kHz
Stopband Attenuation * 31, * 32		SA	80.0	-	-	dB
Group Delay * 30		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 80kHz			-1.9	-	0.1	dB

4. Short Delay Slow Roll-Off Filter (DASD bit = "1", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 34	±0.05dB	PB	0	-	12.0	kHz
	-3.0dB	PB	-	21.1	-	kHz
Passband Ripple * 29		PR	-0.05	-	0.05	dB
Stopband * 34		SB	41.5	-	-	kHz
Stopband Attenuation * 31, * 32		SA	82.0	-	-	dB
Group Delay * 30		GD	-	5.3	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 20kHz			-4.8	-	0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 34	±0.05dB	PB	0	-	24.2	kHz
	-3.0dB	PB	-	42.1	-	kHz
Passband Ripple * 29		PR	-0.05	-	0.05	dB
Stopband * 34		SB	83.0	-	-	kHz
Stopband Attenuation * 31, * 32		SA	82.0	-	-	dB
Group Delay * 30		GD	-	5.3	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 40kHz			-5.0	-	0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 34	±0.05dB	PB	0	-	48.4	kHz
	-3.0dB	PB	-	84.3	-	kHz
Passband Ripple * 29		PR	-0.05	-	0.05	dB
Stopband * 34		SB	165.9	-	-	kHz
Stopband Attenuation * 31, * 32		SA	82.0	-	-	dB
Group Delay * 30		GD	-	5.3	-	1/fs
Digital Filter + SCF + SMF * 31						
Frequency Response : 0 ~ 80kHz			-5.7	-	0.1	dB

Note

* 34. The passband and stopband frequencies are proportional to fs (sampling rate).

"PB = 0.252 × fs, SB = 0.864 × fs"

■ SRC Block

($T_a = -40 \sim 85^\circ\text{C}$; $AVDD = 3.0 \sim 3.6\text{V}$; $LVDD = 3.0 \sim 3.6\text{V}$; $TVDD = 1.7 \sim 3.6\text{V}$; $VDD33 = 3.0 \sim 3.6\text{V}$; $AVSS = DVSS1 = DVSS2 = DVSS3 = 0\text{V}$)

1. Audio Mode (SRCFAUD bit = "1", SRCFEC bit = "0")

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Passband	-0.01dB $0.980 \leq \text{FSO/FSI} \leq 6.000$	PB	0	-	0.4583FSI	kHz
	-0.01dB $0.900 \leq \text{FSO/FSI} < 0.990$	PB	0	-	0.4167FSI	kHz
	-0.01dB $0.533 \leq \text{FSO/FSI} < 0.909$	PB	0	-	0.2182FSI	kHz
	-0.01dB $0.490 \leq \text{FSO/FSI} < 0.539$	PB	0	-	0.2177FSI	kHz
	-0.01dB $0.450 \leq \text{FSO/FSI} < 0.495$	PB	0	-	0.1948FSI	kHz
	-0.01dB $0.225 \leq \text{FSO/FSI} < 0.455$	PB	0	-	0.1312FSI	kHz
	-0.50dB $0.167 \leq \text{FSO/FSI} < 0.227$	PB	0	-	0.0658FSI	kHz
Stopband	$0.980 \leq \text{FSO/FSI} \leq 6.000$	SB	0.5417FSI	-	-	kHz
	$0.900 \leq \text{FSO/FSI} < 0.990$	SB	0.5021FSI	-	-	kHz
	$0.533 \leq \text{FSO/FSI} < 0.909$	SB	0.2974FSI	-	-	kHz
	$0.490 \leq \text{FSO/FSI} < 0.539$	SB	0.2812FSI	-	-	kHz
	$0.450 \leq \text{FSO/FSI} < 0.495$	SB	0.2604FSI	-	-	kHz
	$0.225 \leq \text{FSO/FSI} < 0.455$	SB	0.1802FSI	-	-	kHz
	$0.167 \leq \text{FSO/FSI} < 0.227$	SB	0.0970FSI	-	-	kHz
Passband Ripple	$0.225 \leq \text{FSO/FSI} \leq 6.000$	PR	-	-	± 0.01	dB
	$0.167 \leq \text{FSO/FSI} < 0.227$	PR	-	-	± 0.50	dB
Stopband Attenuation	$0.450 \leq \text{FSO/FSI} \leq 6.000$	SA	95.2	-	-	dB
	$0.167 \leq \text{FSO/FSI} < 0.455$	SA	85.0	-	-	dB
Group Delay * 35 ($T_s = 1/f_s$)	GD	-	67 ($55/\text{FSI} + 12/\text{FSO}$)	-	-	T_s

Note

* 35. This value is SRC block only. It is the time from a rising edge of input LRCK after data is input to a rising edge of output LRCK just before the data is output when there is no phase difference between input and output LRCK.

2. Voice Mode (SRCFAUD bit = “0”, SRCFEC bit = “0”)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	$0.980 \leq \text{FSO/FSI} \leq 6.000$	PB	0	-	0.4583FSI	kHz
	-0.01dB	$0.900 \leq \text{FSO/FSI} < 0.990$	PB	0	-	0.4167FSI	kHz
	-0.50dB	$0.711 \leq \text{FSO/FSI} < 0.910$	PB	0	-	0.3420FSI	kHz
	-0.50dB	$0.653 \leq \text{FSO/FSI} < 0.718$	PB	0	-	0.3007FSI	kHz
	-0.50dB	$0.450 \leq \text{FSO/FSI} < 0.660$	PB	0	-	0.2230FSI	kHz
	-0.50dB	$0.327 \leq \text{FSO/FSI} < 0.455$	PB	0	-	0.1417FSI	kHz
	-0.50dB	$0.225 \leq \text{FSO/FSI} < 0.330$	PB	0	-	0.1018FSI	kHz
Stopband		$0.980 \leq \text{FSO/FSI} \leq 6.000$	SB	0.5417FSI	-	-	kHz
		$0.900 \leq \text{FSO/FSI} < 0.990$	SB	0.5021FSI	-	-	kHz
		$0.711 \leq \text{FSO/FSI} < 0.910$	SB	0.3735FSI	-	-	kHz
		$0.653 \leq \text{FSO/FSI} < 0.718$	SB	0.3320FSI	-	-	kHz
		$0.450 \leq \text{FSO/FSI} < 0.660$	SB	0.2490FSI	-	-	kHz
		$0.327 \leq \text{FSO/FSI} < 0.455$	SB	0.1660FSI	-	-	kHz
		$0.225 \leq \text{FSO/FSI} < 0.330$	SB	0.1248FSI	-	-	kHz
Passband Ripple		$0.900 \leq \text{FSO/FSI} \leq 6.000$	PR	-	-	± 0.01	dB
		$0.167 \leq \text{FSO/FSI} \leq 0.910$	PR	-	-	± 0.50	dB
Stopband Attenuation		$0.900 \leq \text{FSO/FSI} \leq 6.000$	SA	95.2	-	-	dB
		$0.653 \leq \text{FSO/FSI} < 0.909$	SA	90.0	-	-	dB
		$0.450 \leq \text{FSO/FSI} \leq 0.660$	SA	70.0	-	-	dB
		$0.167 \leq \text{FSO/FSI} < 0.455$	SA	60.0	-	-	dB
Group Delay * 35 ($T_s=1/f_s$)		GD	-	67 $(55/\text{FSI}+12/\text{FSO})$	-	-	T_s

3. Echo Canceller Mode (SRCFEC bit = “1”)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	$0.167 \leq \text{FSO/FSI} \leq 6.000$	PB	0	-	0.4583FSI	kHz
Stopband		$0.167 \leq \text{FSO/FSI} \leq 6.000$	SB	0.5417FSI	-	-	kHz
Passband Ripple		$0.167 \leq \text{FSO/FSI} \leq 6.000$	PR	-	-	± 0.01	dB
Stopband Attenuation		$0.167 \leq \text{FSO/FSI} \leq 6.000$	SA	95.2	-	-	dB
Group Delay * 35 ($T_s=1/f_s$)			GD	-	67 $(55/\text{FSI}+12/\text{FSO})$	-	T_s

10. DC Characteristics

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
High-Level Input Voltage 1 * 36	VIH1	75%TVDD	-	-	V	
Low-Level Input Voltage 1 * 36	VIL1	-	-	25%TVDD	V	
High-Level Input Voltage 2 * 37	VIH2	75%VDD33	-	-	V	
Low-Level Input Voltage 2 * 37	VIL2	-	-	25%VDD33	V	
SCL, SDA High-Level Input Voltage	VIH3	70%TVDD	-	-	V	
SCL, SDA Low-Level Input Voltage	VIL3	-	-	30%TVDD	V	
High-Level Output Voltage Iout= -100μA * 38	VOH1	TVDD-0.3	-	-	V	
Low-Level Output Voltage Iout=100μA * 38	VOL1	-	-	0.3	V	
High-Level Output Voltage Iout= -100μA * 39	VOH2	VDD33-0.3	-	-	V	
Low-Level Output Voltage Iout=100μA * 39	VOL2	-	-	0.3	V	
SDA Low-Level Output Voltage	Fast Mode					
	TVDD ≥ 2.0V (Iout=3mA)	VOL3	-	-	0.4	V
	TVDD < 2.0V (Iout=3mA)	VOL3	-	-	20%TVDD	V
	Fast Mode Plus					
	TVDD ≥ 2.0V (Iout=20mA)	VOL3	-	-	0.4	V
	TVDD < 2.0V (Iout=3mA)	VOL3	-	-	20%TVDD	V
Input Leak Current * 40	Iin	-	-	±10	μA	
Input Leak Current, Pulled down pins Power Down * 41, * 43	Iid	-	66	-	μA	
Input Leak Current, Pulled down pins Power Down Release * 42, * 43	Iid	-	72	-	μA	
Input Leak Current, TEST1 pin	Iid	-	132	-	μA	
Input Leak Current, XT1 pin	Iix	-	17	-	μA	

Notes

- * 36. SDIN1, SDIN2/JX0, LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, PDN, SCLK/SCL, CSN and SI/I2CFIL pins. The SCL pin is not included.
- * 37. SDIN3/JX3, SDIN4, LRCK3, BICK3, TEST1 and XT1 pins
- * 38. SDOUT1/RDY, STO/RDY/SDOUT2 and SO/SDA pins. The SDA pin is not included.
- * 39. SDOUT3/CLKO/GPO1 pin and SDOUT4/GPO2 pin
- * 40. Except internal pulled-down pins and the XT1 pin.
- * 41. When the AK7735A is powered down (PDN pin = "L"), the pull down resistors of LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, LRCK3 and BICK3 pins is 50kΩ (Typ. @3.3V).
- * 42. When the AK7735A is powered up (PDN pin = "H"), the pull down resistors of LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, LRCK3 and BICK3 pins is 46kΩ (Typ. @3.3V).
- * 43. Leak current in case of inputting 3.3V when LVDD=TVDD=VDD33=3.3V.

11. Switching Characteristics

■ System Clock

($T_a = -40 \sim 85^\circ\text{C}$; $AVDD = 3.0 \sim 3.6\text{V}$; $LVDD = 3.0 \sim 3.6\text{V}$; $TVDD = 1.7 \sim 3.6\text{V}$; $VDD33 = 3.0 \sim 3.6\text{V}$; $AVSS = DVSS1 = DVSS2 = DVSS3 = 0\text{V}$; $C_L = 20\text{pF}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XTI Input Timing					
a) X'tal Oscillator					
Input Frequency	fXTI	11.2896	-	18.432	MHz
b) XTI Clock Input					
Duty Cycle		40	50	60	%
Input Frequency	fXTI	0.256	-	24.576	MHz
CLKO Output Timing					
Output Frequency	fCLKO	2.048	-	24.576	MHz
Duty Cycle	dCLKO	-	50	-	%
LRCK/BICK Input Timing (Slave Mode)					
LRCK Input Timing					
Frequency	fs	8	-	192	kHz
BICK Input Timing					
Frequency * 44	fBCLK	0.256	-	24.576	MHz
Pulse Width Low	tBCLKL	0.4 / fBCLK	-	-	ns
Pulse Width High	tBCLKH	0.4 / fBCLK	-	-	ns
LRCK/BICK Output Timing (PLL Master Mode)					
LRCK Output Timing					
Frequency	fs	8	-	192	kHz
Pulse Width High					
PCM Mode	tLRCKH	-	1/fBCLK	-	ns
Except PCM Mode	tLRCKH	-	50	-	%
BICK Output Timing					
Frequency * 44	fBCLK	0.256	-	24.576	MHz
Duty	dBCLK	-	50	-	%

Note

* 44. Required to meet the following expression: $fBCLK \geq 2 \times fs \times (\text{Input/Output Data Length})$.

■ Power Down

($T_a = -40 \sim 85^\circ\text{C}$; $AVDD = 3.0 \sim 3.6\text{V}$; $LVDD = 3.0 \sim 3.6\text{V}$; $TVDD = 1.7 \sim 3.6\text{V}$; $VDD33 = 3.0 \sim 3.6\text{V}$; $AVSS = DVSS1 = DVSS2 = DVSS3 = 0\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width * 45	tRST	600	-	-	ns

Note

* 45. The PDN pin must be "L" when power up the AK7735A.

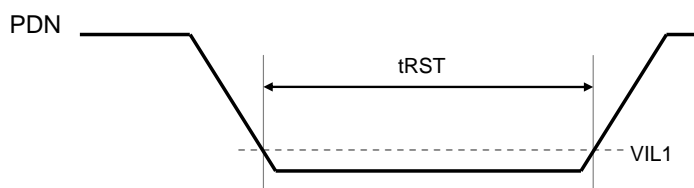


Figure 3. Reset Timing

■ Serial Data Interface (SDIN1 ~ SDIN4, SDOUT1 ~ SDOUT4)

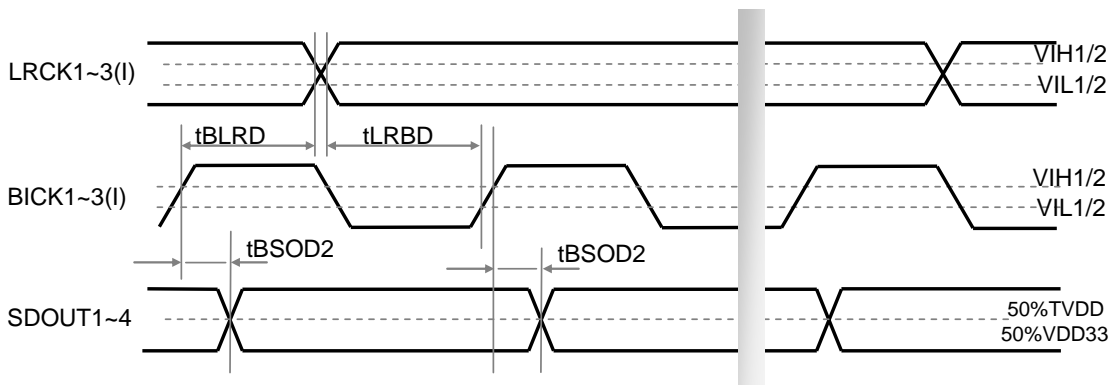
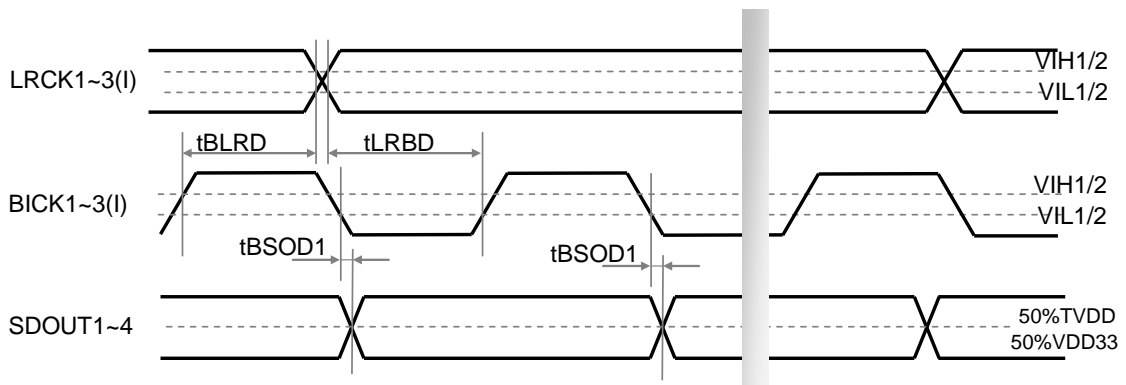
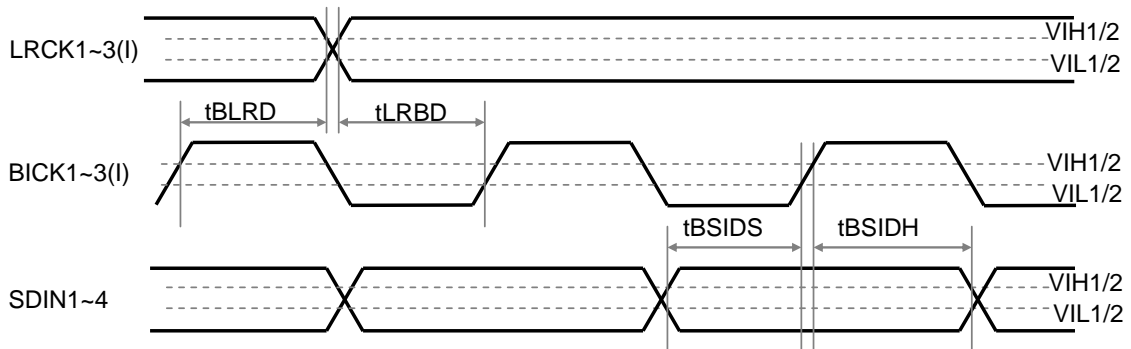
(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK “↑” to LRCK * 46	tBLRD	10	-	-	ns
Delay Time from LRCK to BICK “↑” * 46	tLRBD	10	-	-	ns
Serial Data Input Latch Setup Time	tBSIDS	10	-	-	ns
Serial Data Input Latch Hold Time	tBSIDH	5	-	-	ns
Delay Time from BICK “↓” to Serial Data Output * 47	tBSOD1	-	-	20	ns
Delay Time from BICK “↑” to Serial Data Output * 46, * 48	tBSOD2	5	-	30	ns
Master Mode					
BICK Frequency	fBCLK	-	32, 48, 64, 128, 256	-	fs
BICK Duty Cycle		-	50	-	%
Delay Time from BICK “↓” to LRCK * 47	tMBL	-10	-	10	ns
Serial Data Input Latch Setup Time	tBSIDS	10	-	-	ns
Serial Data Input Latch Hold Time	tBSIDH	10	-	-	ns
Delay Time from BICK “↓” to Serial Data Output * 47, * 48	tBSOD	-	-	10	ns

Notes

- * 46. It is measured from BICK “↓” when the BICK polarity is inverted by setting BCKPx bit = “1”.
- * 47. It is measured from BICK “↑” when the BICK polarity is inverted by setting BCKPx bit = “1”.
- * 48. Set SDOPHx bit to “1” and the data from SDOUTx pin is output based on BICK “↑” when BICK speed is more than 12.288MHz such as when using TDM256 mode with 96kHz sampling frequency or TDM128 mode with 192kHz sampling frequency in slave mode. SDOPHx bit must be set to “0” in master mode.

1. Slave Mode



2. Master Mode

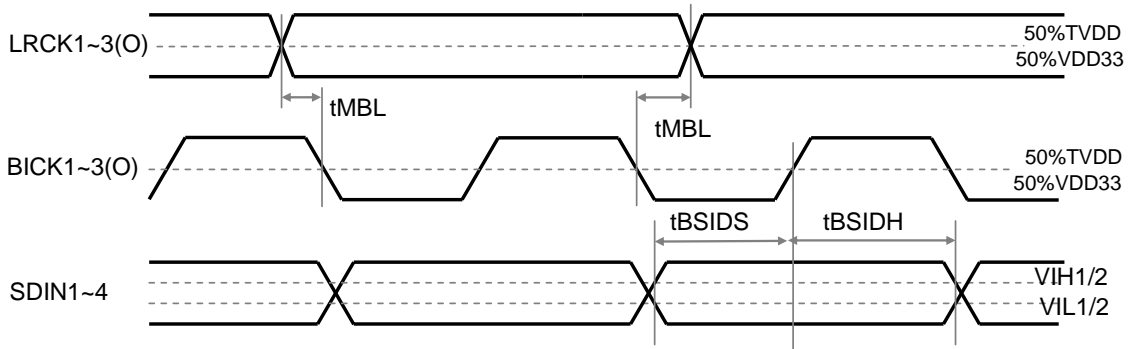


Figure 7. Serial Interface Input Timing in Master Mode

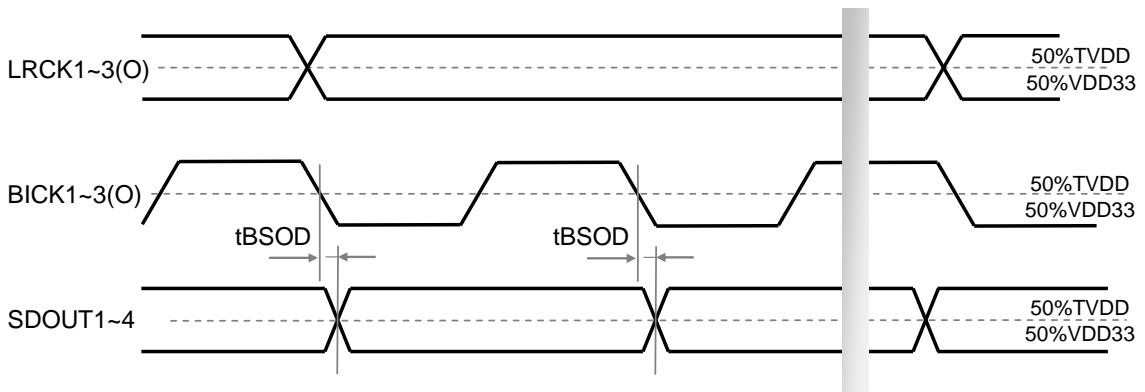


Figure 8. Serial Interface Output Timing in Master Mode (SDOPHx bit = "0")

■ SPI Interface

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; CL=20pF)

1. SPI Low Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
μP Interface Signal					
SCLK Frequency * 50	fSCLK	-	-	3.0	MHz
SCLK Low-level Width	tSCLKL	160	-	-	ns
SCLK High-level Width	tSCLKH	160	-	-	ns
Microcontroller → AK7735A					
CSN High-level Width	tWRQH	300	-	-	ns
From CSN “↑” to PDN “↑”	tRST	360	-	-	ns
From PDN “↑” to CSN “↓”	tIRRQ	1	-	-	ms
From CSN “↓” to SCLK “↓”	tWSC	300	-	-	ns
From SCLK “↑” to CSN “↑”	tSCW	480	-	-	ns
SI Latch Setup Time	tSIS	120	-	-	ns
SI Latch Hold Time	tSIH	120	-	-	ns
AK7735A → Microcontroller					
Delay Time from SCLK “↓” to SO Output	tSOS	-	-	120	ns
SO Output Hold Time from SCLK “↑” * 49	tSOH	120	-	-	ns

2. SPI High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
μP Interface Signal					
SCLK Frequency * 50	fSCLK	-	-	6	MHz
SCLK Low-level Width	tSCLKL	72	-	-	ns
SCLK High-level Width	tSCLKH	72	-	-	ns
Microcontroller → AK7735A					
CSN High-level Width	tWRQH	150	-	-	ns
From CSN “↑” to PDN “↑”	tRST	180	-	-	ns
From PDN “↑” to CSN “↓”	tIRRQ	1	-	-	ms
From CSN “↓” to SCLK “↓”	tWSC	150	-	-	ns
From SCLK “↑” to CSN “↑”	tSCW	240	-	-	ns
SI Latch Setup Time	tSIS	60	-	-	ns
SI Latch Hold Time	tSIH	60	-	-	ns
AK7735A → Microcontroller					
Delay Time from SCLK “↓” to SO Output	tSOS	-	-	60	ns
SO Output Hold Time from SCLK “↑” * 49	tSOH	60	-	-	ns

Notes

- * 49. Except when writing the 24th bit (8 bits command + 16 bits address) of the command code. This will be the 8th bit (8 bits command) with “write preparation data read command (0x24, 0x25, 0x26 and 0x27)”.
- * 50. Dummy command writing for switching to SPI interface from I²C interface and control register access can always be made in SPI high speed mode (Max. 6MHz). DSP RAM area can be accessed in SPI low speed mode (Max. 3MHz) in clock reset state (CKRESETN bit = “0”) and can also be accessed in SPI high speed mode (Max. 6MHz) when PLL is locked (CKRESETN bit = “1” and PLL is locked). It is necessary to set DLRDY bit to “1” when accessing to the DSP RAM area while PLL is unlocked.

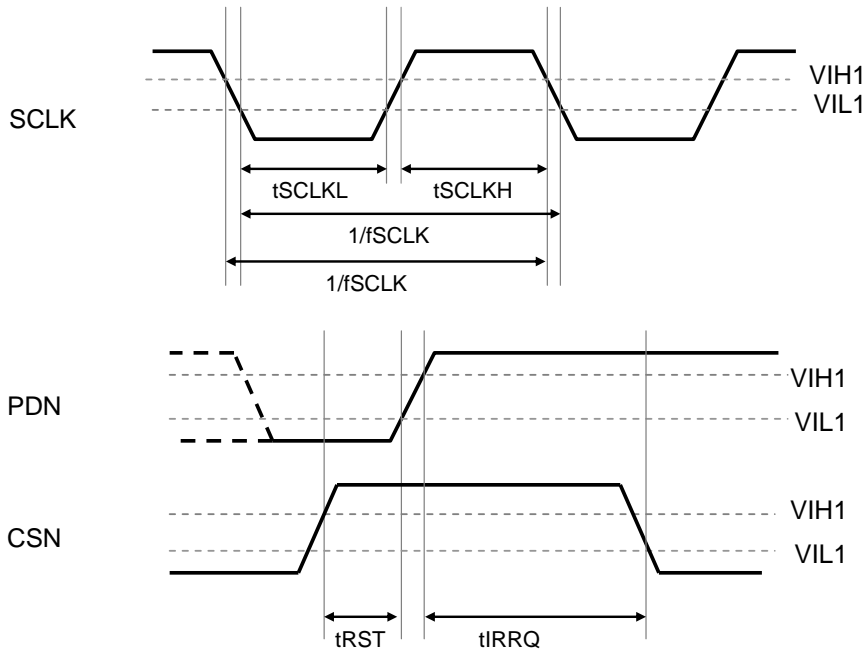


Figure 9. SPI Interface Timing 1

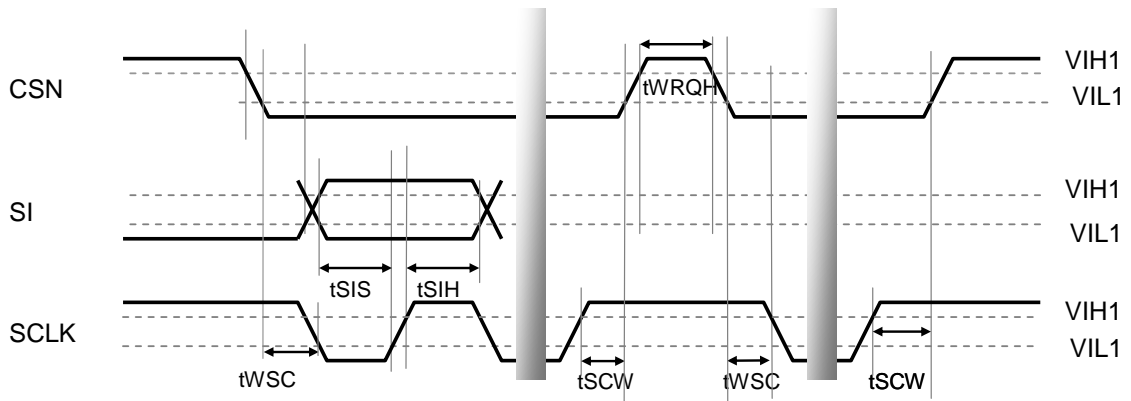


Figure 10. SPI Interface Timing 2 (Microcontroller → AK7735A)

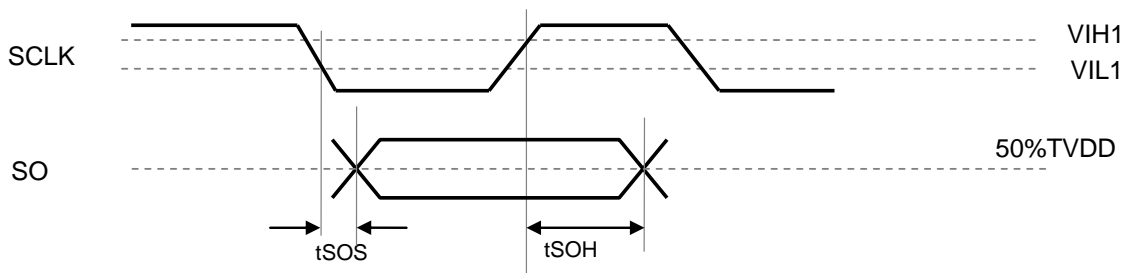


Figure 11. SPI Interface Timing 3 (AK7735A → Microcontroller)

■ I²C Interface

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

1. I²C: Fast Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
I ² C Timing					
SCL clock frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF

2. I²C: Fast Mode Plus

Parameter	Symbol	Min.	Typ.	Max.	Unit
I ² C Timing					
SCL clock frequency	fSCL	-	-	1	MHz
Bus Free Time Between Transmissions	tBUF	0.5	-	-	μs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.26	-	-	μs
Clock Low Time	tLOW	0.5	-	-	μs
Clock High Time	tHIGH	0.26	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.26	-	-	μs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.05	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.12	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.12	μs
Setup Time for Stop Condition	tSU:STO	0.26	-	-	μs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	550	pF

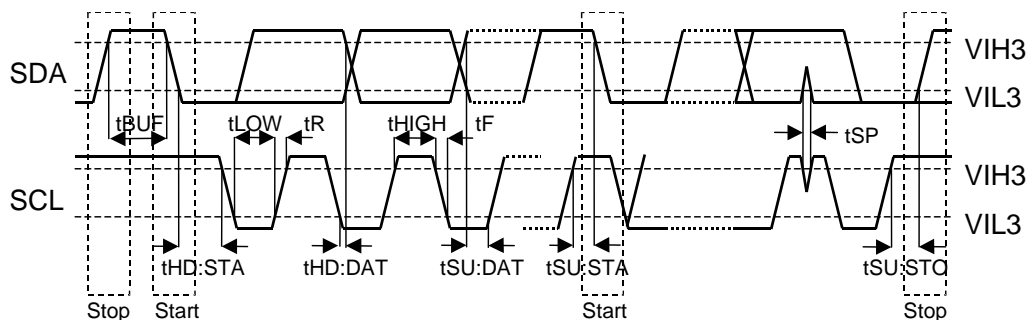


Figure 12. I²C Interface Timing

12. Recommended External Circuits

■ Connection Diagram

1. I²C Interface

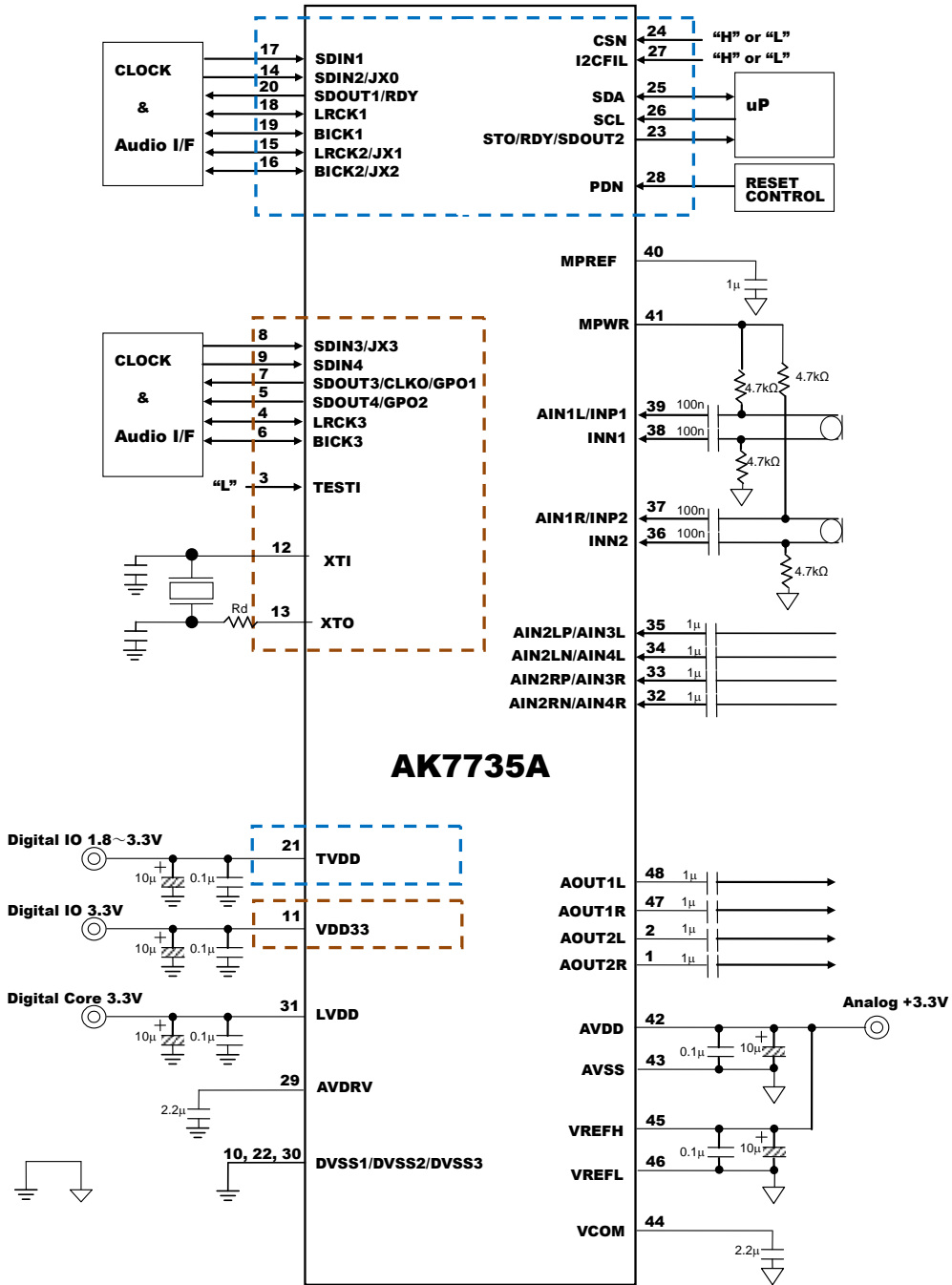


Figure 13. I²C Interface Connection Example

2. SPI Interface

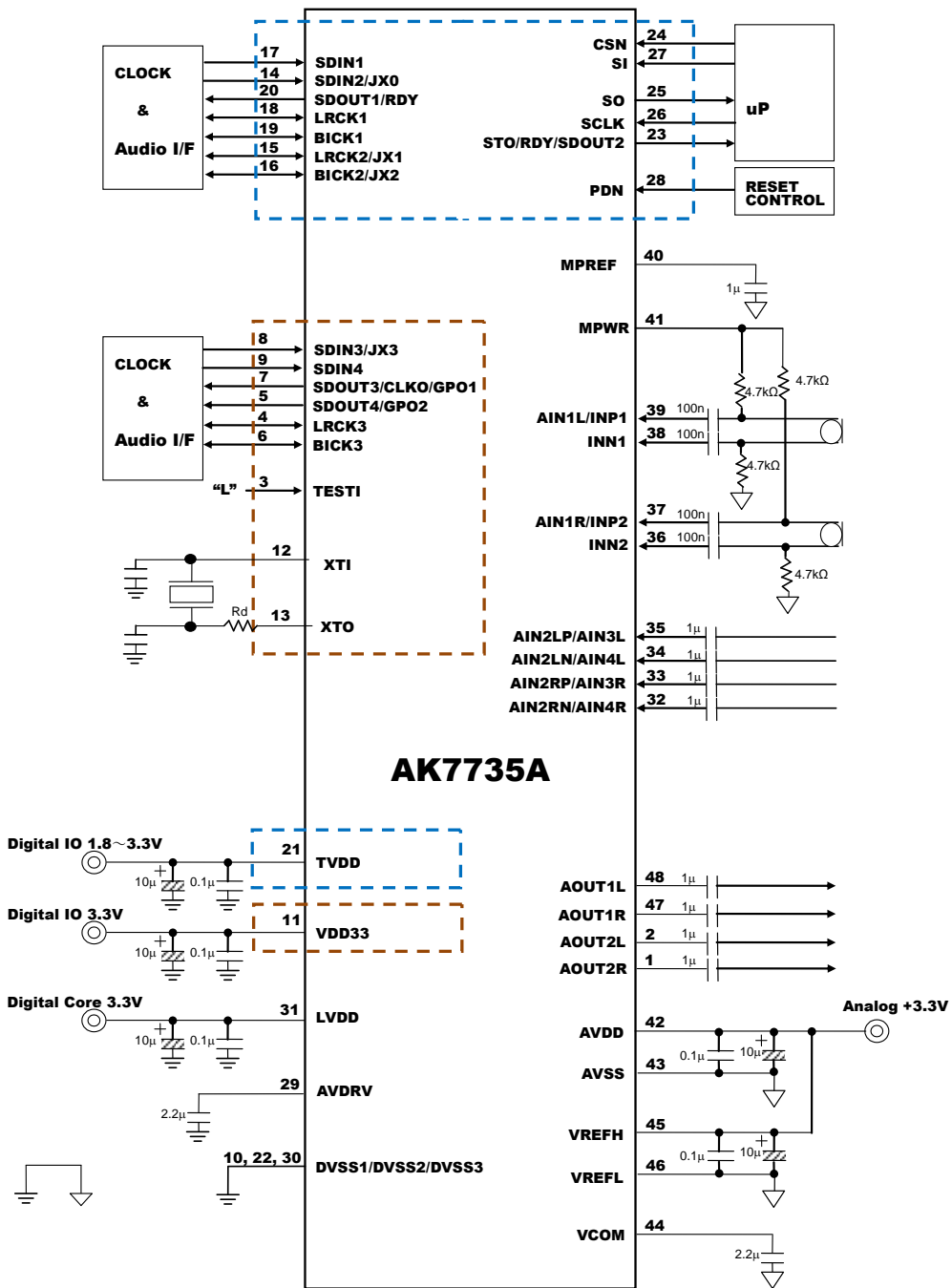


Figure 14. SPI Interface Connection Example

■ Peripheral Circuit

1. Ground

AVSS, DVSS1, DVSS2 and DVSS3 should be connected to the same ground. Decoupling capacitors, particularly ceramic capacitors of small capacity, should be placed at positions as close as possible to the AK7735A.

2. Reference Voltage

VCOM is a common voltage of this chip and the VCOM pin outputs AVDD/2. A 2.2 μ F ceramic capacitor should be connected between the VCOM pin and AVSS.

Do not connect the VCOM pin to any external devices. Digital signal lines, especially clock signal line should be kept away as far as possible from this pin in order to avoid unwanted coupling into the AK7735A.

3. Analog Input

The analog input signal is input to the analog modulator of the AK7735A. The maximum input voltage at differential input pins is ± 2.30 Vpp (Typ.) or ± 2.83 Vpp (Typ.). The maximum input voltage at single-ended input pins is 2.30Vpp (Typ.) or 2.83Vpp (Typ.). The output code format is 2's complements. The internal HPF removes the DC offset.

After power-down is released, the internal operating point level AVDD/2 occurs on analog input pins of the AK7735A. Concerning the internal operating point formation circuit, each input pin has impedance of 25k Ω (Typ.). The pins that are connected to AC coupling capacitors require start-up time (time constant).

The AK7735A samples the analog inputs at 6.144MHz when fs=48kHz, 96kHz or 192kHz. The AK7735A includes an anti-aliasing filter (RC filter), and no external low-pass filter is necessary in front of the ADC. However, an external low-pass filter should be connected before the ADC for the signal which has large out-of-band noise such as D/A converted signals.

The analog power supply to the AK7735A is +3.3V (Typ.). Voltage of AVDD + 0.3V or larger, voltage of AVSS - 0.3V or smaller, and current of 10mA or larger must not be applied to analog input pins. Excessive current will damage the internal protection circuit and will cause latch-up, damaging the IC. Accordingly, if the external analog circuit voltage is ± 15 V, the analog input pins must be protected from signals which are equal or larger than absolute maximum ratings.

4. Analog Output

The analog output is single-ended and the output signal range is typically 0.857 x AVDD Vpp centered on VCOM. The digital input data format is two's complement. Positive full-scale output corresponds to 0x7FFFFFFF (@32bit) input code, Negative full scale is 0x80000000 (@32bit) and VCOM voltage ideally is 0x00000000 (@32bit). The Out-of-Band noise (shaping noise) generated by the internal delta-sigma modulator is attenuated by an integrated switched capacitor filter (SCF) and a continuous time filter (CTF).

5. Crystal Oscillator

The resistor and capacitor values for the oscillator RC circuit are shown blow.

Oscillator	R1 (Max) (* 51)	C0 (Max) (* 51)	XTI, XTO pin Capacity
12.288MHz	120Ω	2.5pF	22pF
18.432MHz	80Ω	2.5pF	15pF

Table 4. Recommended Resistance and Capacitance with Crystal Oscillator

* 51. Values above are for a sureface-mount type crystal.

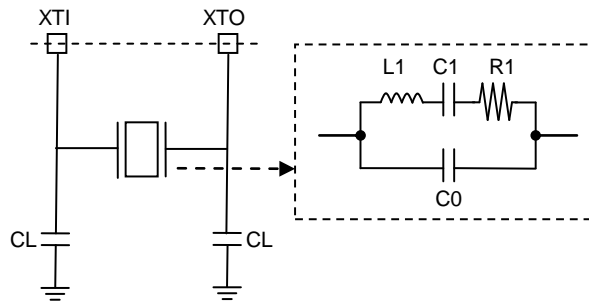
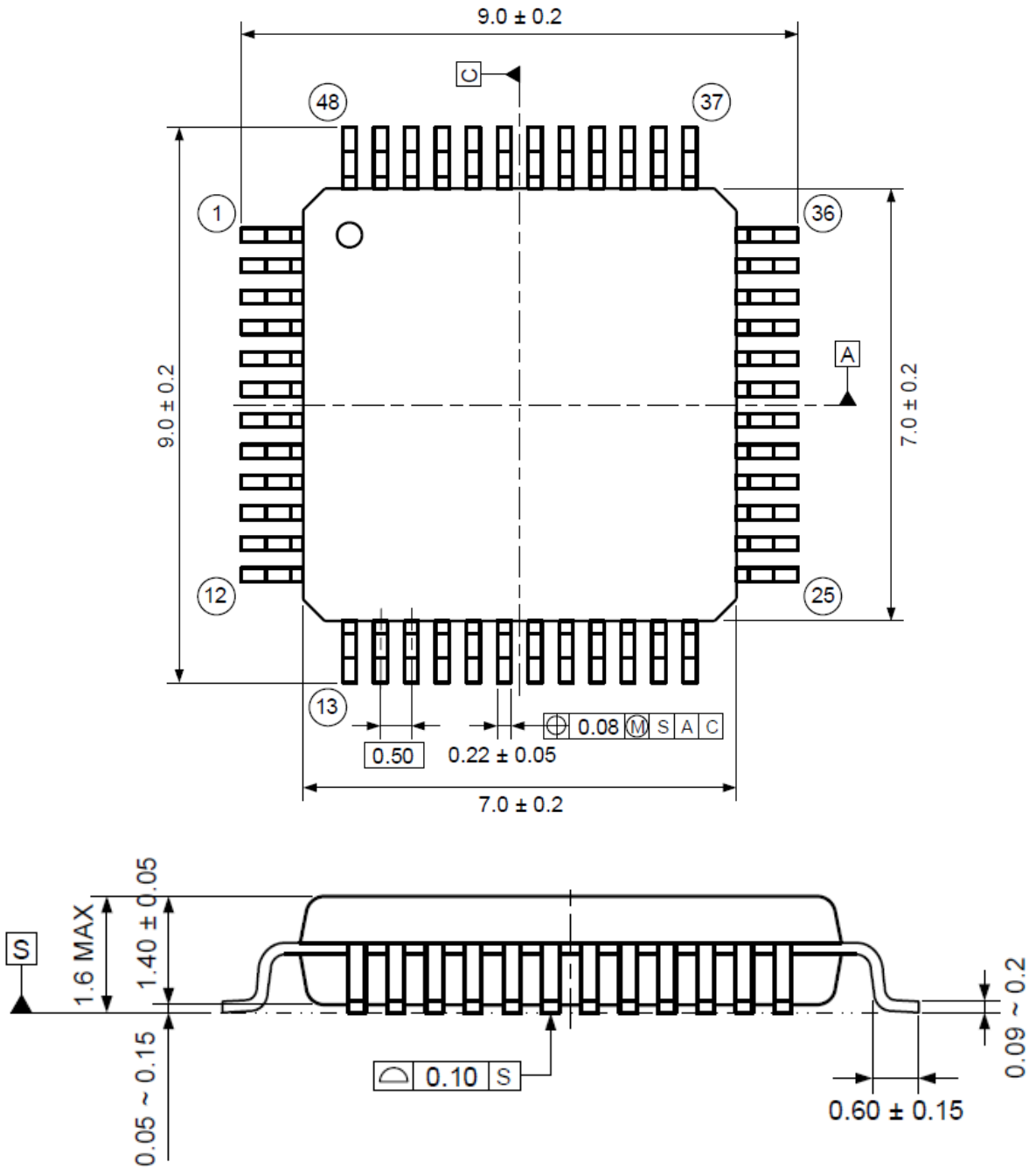


Figure 15. Electric Equivalent Circuit of Crystal Oscillator

13. Package

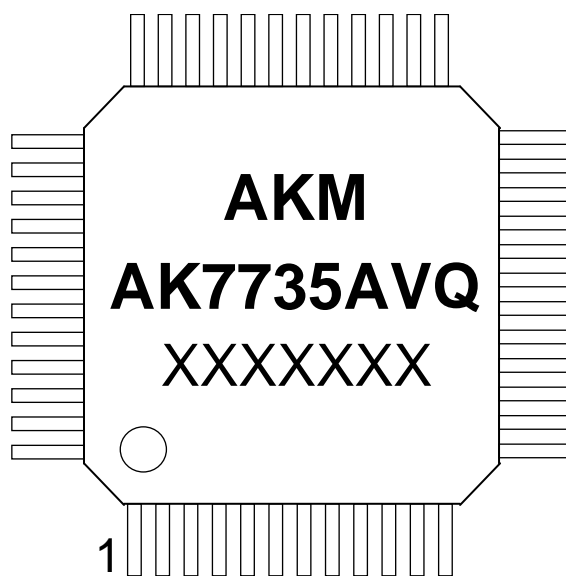
■ Outline Dimensions



■ Material and Lead Finish

Package: Epoxy, Halogen (Br and Cl) free
 Lead frame: Copper
 Lead-finish: Soldering (Pb free) plate

■ **Marking**



- 1) Pin #1 indication
- 2) Date Code: XXXXXXX (7 digits)
- 3) Marking Code: AK7735AVQ
- 4) Asahi Kasei Logo

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