PAH8011ET: Low Power Optical Heart Rate Monitor Chip

General Description

The PAH8011ET is a low power CMOS-process optical heart rate monitor chip with integrated DSP that is packaged together with three chip-on-board LEDs: two Green and one Infrared into a single package supporting Heart Rate Detection (HRD) function. It is based on optical sensing technology that captures higher resolution image than the traditional photodiode. The images are then processed through the integrated DSP to attain processed PPG (Photoplethysmogram) data for use in deducing heart rate.

Key Features

- Support heart rate detection function
- SRAM buffer support
- Integrated ultra-low power mode, while in power-down mode
- Hardware power-down support
- Invisible light for touch detection function
- Optical coating resistance ambient light
- Integrated chip-on-board LEDs with wavelength of 525nm and 940nm
- Communication interface options
  - I^2C
  - Four-Wire SPI
- I^2C interface up to 1 Mbit/s
- SPI interface up to 10 Mbit/s

Applications

- Heart Rate Monitor Accessories
- Wearables: Smartwatch, Wrist Band

Key Parameters

Parameter	Value
Operating Temperature, Tj	-35 to +80 °C
System Clock	4 MHz
Supply Voltage	VDDM: 3.1 – 3.6 V* VDDLED: 3.3 – 4.5 V VDDIO: 1.62 – 3.6 V VDDA/VDDD: 1.7 – 1.9 V Analog: 1.8 V Digital: 1.8 V
Power Consumption @ 3.3V **Note:** Including LED current, without I/O toggling	Active: Printing Cover: 90 µA Double Injection + Wall Cover : 180 µA IR Touch Detection: 15µA Power-down: 1µA
Heart Rate Measurement Range	30 - 240 bpm
Package Size	3.6 x 6.36 x 1.0 mm

* Refer to Section 9.16 Supply Voltage Registers

Ordering Information

Part Number	Package Type
PAH8011ET-IP	21-Pin LGA

RoHS compliant

For any additional inquiries, please contact us at
http://www.pixart.com/contact.asp

*Disclaimer:

The PAH8011ET-IP is not designed for usage in medical device. In addition, the data and information of heart rate measurement provided by this chip may not be completely accurate and may exceed heart rate tolerance as per the specification stated in the document due to different factors, such as interference with signal from external sources, incorrect wearing position and changes in weather conditions or user's body condition.

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1.0 Introduction

1.1 Overview

The PAH8011ET a low power and good performance optical heart rate monitor chip. It is integrated with DSP and built-in with 2 Green LEDs, 1 Infrared LED in a single package. It comes with two communication interfaces, which are I^2C supporting up to 1 Mbit/s and Four-Wire SPI supporting up to 10 Mbit/s. The SRAM buffer of 1596 bytes is supported for the power saving at the host.

The Figure 1 shows the architecture block diagram of the device. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

Note: Throughout this document PAH8011ET Low Power Optical Heart Rate Monitor Chip is referred to as the PAH8011ET.

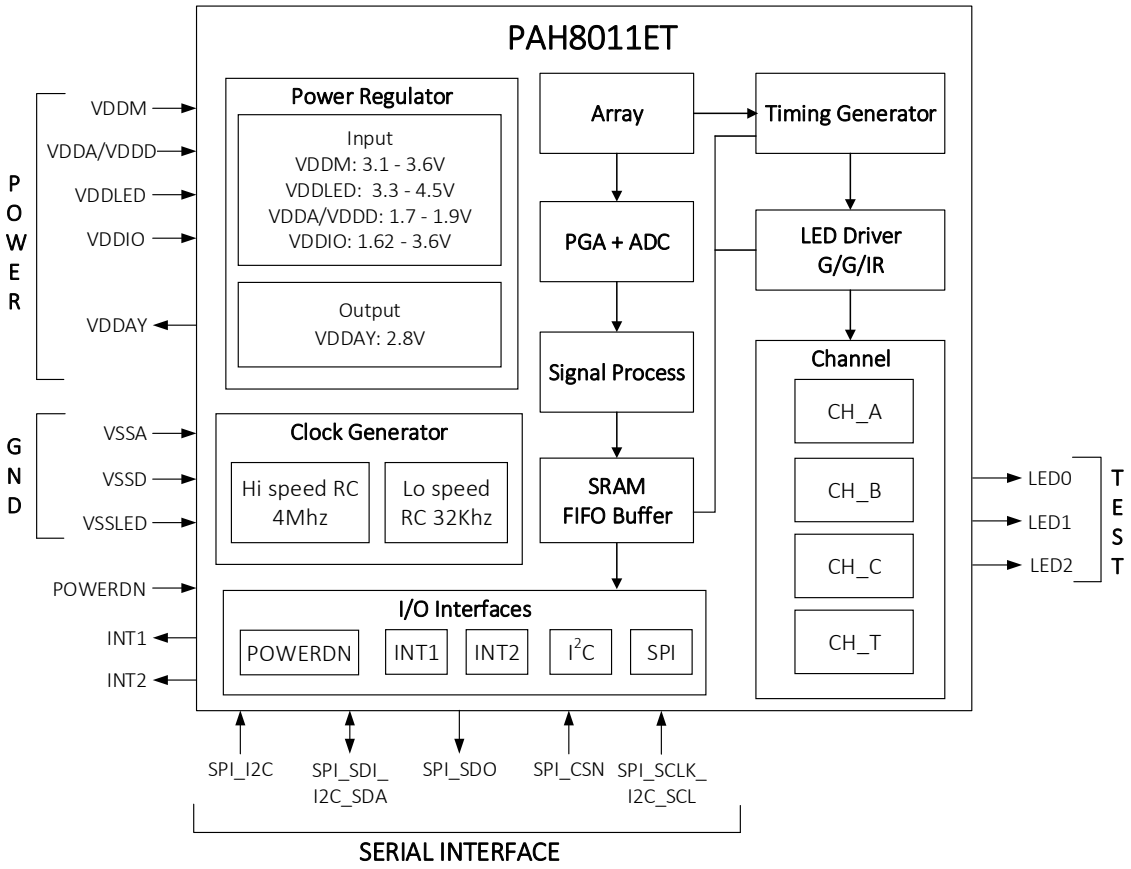


Figure 1. Functional Block Diagram

1.2 Terminology

Term	Description
GND	Ground
BiDir	Bi-Directional
PPG	Photoplethysmogram
Touch	Touch detection for wear on or wear off

1.3 Signal Description

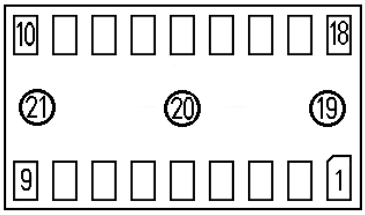


Figure 2. Pin Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
Functional Group:		Power Supplies	
3	VDDIO	Input	I/O Power Supply (1.62 - 3.6V)
5	VSSA	GND	Analog Ground
6	VDDAY	Output	Internal regulator output. Must connect 0.1µF capacitor to GND
7	VSSLED	GND	LED Ground
8	VDDM	Input	Analog main power supply (3.1 - 3.6V) for internal power regulator
9	VDD_LED01	Input	IR/Green LED Anode. Provide VDDM supply voltage or power supply (3.3 – 4.5V)
10	VDDA	Input	Analog power supply (1.7 - 1.9V). Must connect 0.1µF capacitor to GND
11	VDDD	Input	Digital power supply (1.7 - 1.9V). Must connect 0.1µF capacitor to GND
12	VSSD	GND	Digital Ground
18	VDD_LED2	Input	Green LED Anode. Provide VDDM supply voltage or power supply (3.3 – 4.5V)
Functional Group:		Interface	
1	SPI_SCLK_I2C_SCL	Input	4-wire SPI/ I^2C: Clock
2	SPI_SDI_I2C_SDA	BiDir	4-wire SPI: Data input I^2C: Data input-output
16	SPI_SDO	Output	4-wire SPI: Data output. Connect to GND when I^2C Interface
17	SPI_CSN	Input	4-wire SPI: Chip Select. Active Low. Connect to GND when I^2C Interface
Functional Group:		Functional I/O	
4	INT1	Output	Data ready interrupt. Default is edge sensitive interrupt, can be changed to level sensitive interrupt (high active) in INT_Type register
13	SPI_I2C	Input	Interface Selection I^2C: Pull down (Tie to GND) 4-wire SPI: Pull high (Tie to VDDIO)
14	INT2	Output	Touch interrupt. Default is edge sensitive interrupt, can be changed to level sensitive interrupt (high active) in INT_Type register
15	POWERDN	Input	Hardware control to enter Power Down Mode. Connect to GND when not used Level High: Enter Power Down Mode Level Low: Leave Power Down Mode
Functional Group:		Reserved	
19	LED2	RSV	Reserved for LED2 test pin, is only used by probe
20	LED1	RSV	Reserved for LED1 test pin, is only used by probe
21	LED0	RSV	Reserved for LED0 test pin, is only used by probe

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Analog Voltage	V_{DDM_MAX}	-0.4	V_{DDM} + 0.3	V	
I/O Voltage	V_{DDIO_MAX}	-0.4	V_{DDIO} + 0.3	V	
I/O Pin Input High Voltage	V_{DDIO_IN}	-0.4	V_{DDIO} + 0.3	V	All I/O pins
Relative Humidity	RH	0	50	%	Non-condensing, Non-biased
ESD	ESD_{HBM}	-	2	kV	Class 2 on all pins, as per human body model. JESD22-A114E with 15 sec zap interval.

Notes:
1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.
4. Functional operation under absolute maximum-rated conditions is not implied and should be restricted to the Recommended Operating Conditions.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature	T_A	-20	25	60	°C	
Operating Junction Temperature	T_J	-35	-	80	°C	
Power Supply Voltage	V_{DDM}	3.1	3.3	3.6	V	Power regulator input supply. Includes ripples
LED Power Supply Voltage	V_{DDLED}	3.3	-	4.5	V	LED power supply. Includes ripples
Analog Supply Voltage	V_{DDA}	1.7	1.8	1.9	V	Analog power supply. Includes ripples
Digital Supply Voltage	V_{DDD}	1.7	1.8	1.9	V	Digital power supply. Includes ripples
I/O Supply Voltage	V_{DDIO}	1.62	1.8	3.6	V	Includes ripples
Power Regulator Output Voltage	V_{DDAY}	2.52	2.8	3.08	V	Internal regulator output. Includes ripples
Supply Noise	V_{Npp}	-	-	100	mV_{p-p}	Peak to peak within 10K – 80 MHz
Serial Clock Frequency	SCK_SPI	-	-	10	MHz	
	SCK_I^2C	-	400[1]	1000[2]	KHz	1. Max value for Fast mode 2. Max value for Fast mode plus

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

2.3 Thermal Specifications

Table 4. Thermal Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-40	-	125	°C	
Lead-free Solder Temperature	T_P	-	-	245	°C	Refer to Package Handling Information document

2.4 DC Characteristics

Table 5. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Peak Power Supply Current	I_{DDM_MAX}	-	-	10	mA	For V_{DDM}
	I_{DDLED_MAX}	-	-	150	mA	For V_{DDLED}
	I_{DDD_MAX}	-	-	20	mA	For V_{DDD}
	I_{DDA_MAX}	-	-	10	mA	For V_{DDA}
Peak I/O Supply Current	I_{DDIO_MAX}	-	-	30	mA	For V_{DDIO}
Output Supply Current	I_{DDAY_MAX}	-	-	20	mA	For V_{DDAY}
Power Consumption						
Supply Current @ Power Down	I_{DDPD}	-	1	-	µA	For chip only Wakeup by read register
With Two Green LEDs						
Supply Current @ HRD PPG mode	I_{DDHRD}	-	65	-	µA	For chip only, not including LED current, without I^2C interface I/O toggle
LED current	I_{DDLED}	-	25	-	µA	20 report/sec, LED DAC = 12mA, on yellow skin color (ET=11.5us)
With IR Touch Detection						
Supply Current @ Touch Detection mode	$I_{DDtouch}$		9		µA	For chip only, not including LED current, without I^2C interface I/O toggle
LED current at touch	I_{DDLED}	-	6	-	µA	8 report/sec, LED DAC = 50mA, on yellow skin color
I/O						
Input High Voltage	V_{IH}	0.7* V_{DDIO}	-	-	V	
Input Low Voltage	V_{IL}	-	-	0.3* V_{DDIO}	V	
Output High Voltage	V_{OH}	V_{DDIO} - 0.4	-	V_{DDIO} + 0.4	V	@I_{OH} = 2mA
Output Low Voltage	V_{OL}	-0.4	-	0.4	V	@I_{OL} = 2mA
LED						
Sink current	I_{LED}	40	50	60	mA	@ LED DAC = 50mA
LED cathode voltage	V_{LED-}	0.4		3.6	V	

Notes:

1. Electrical Characteristics are defined under recommended operating conditions.
2. All the parameters are tested under operating conditions: V_{DDM} = 3.3V, V_{DDIO} = 1.8 and 3.3V, T_A = 25°C

2.5 AC Characteristics

Table 6. AC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Up from V_{DD} ↑	t_{PU}	-	10	-	ms	From V_{DD} ↑ to valid interface communication
SDI/SDO Read Hold Time	T_{HOLD}	-	3	-	µs	Minimum hold time for valid data.
Address and data delay time	t_{delay}	2.75			µs	Refer to Serial Interface section
Chip Pulse Interrupt Width	t_{INT}	2	-	32	µs	Default 32us, can be changed in INT_Pulse_Width register
Rise and Fall Times: SDI/SDO	t_r , t_f	-	30	-	ns	C_L = 30 pF
HW POWERDN Time	$t_{powerdn}$	300	500	-	µs	POWERDN keep high period

Notes:

1. Electrical Characteristics are defined under recommended operating conditions
2. All the parameters are tested under operating conditions: T_A = 25°C, V_{DDM} = 3.3V, V_{DDIO} = 3.3V for 3.3V IO application and V_{DDIO} = 1.8 V for 1.8V IO application.

3.0 Mechanical Specifications

3.1 Mechanical Dimension

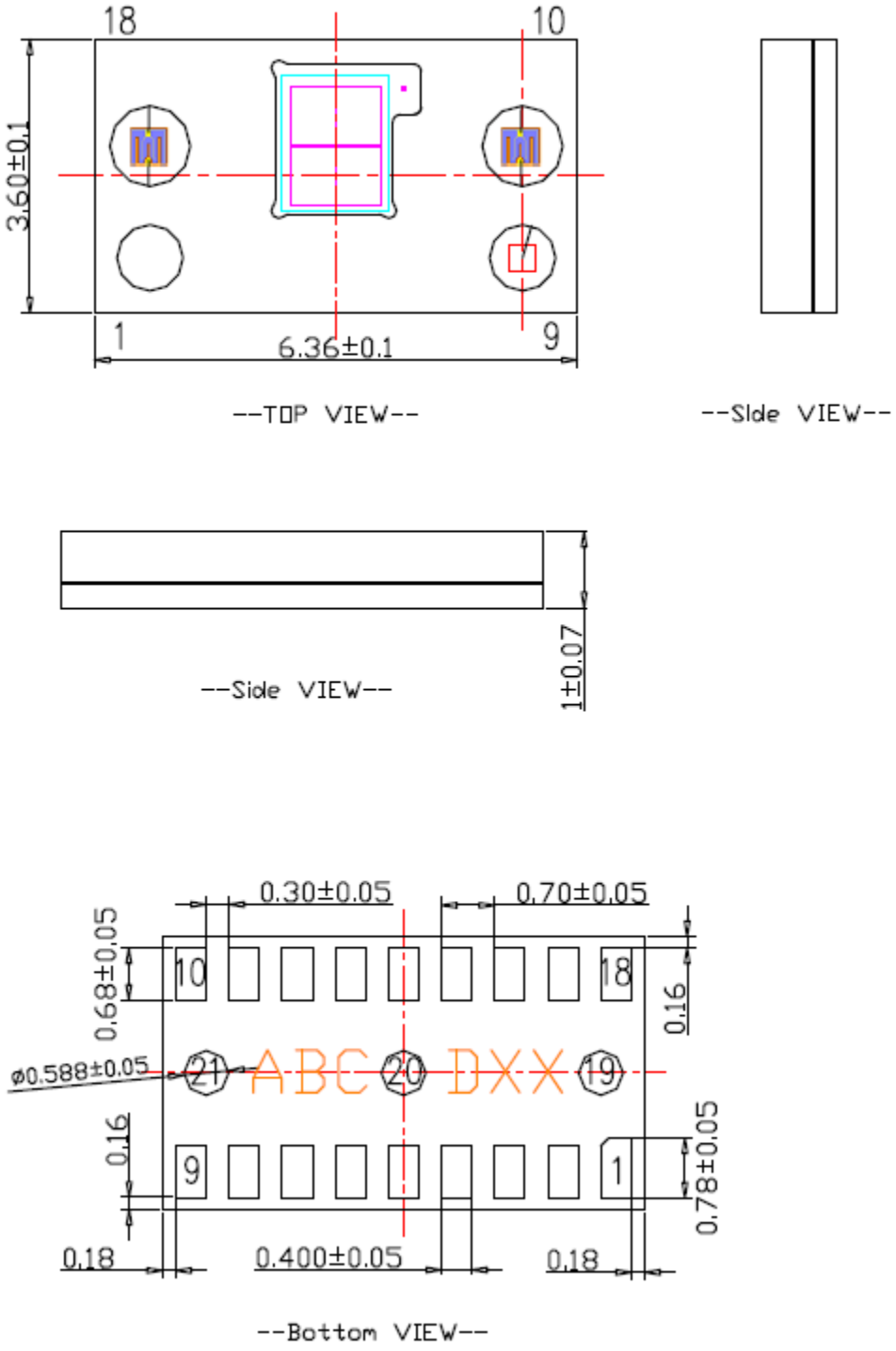
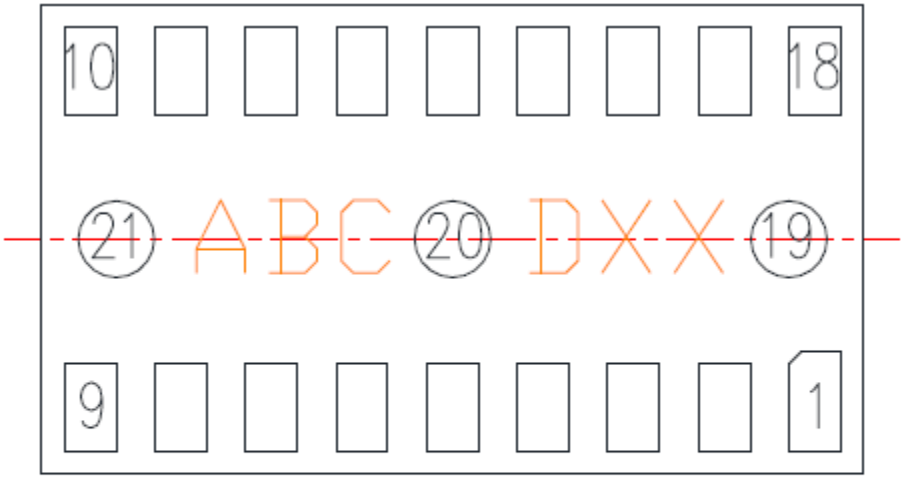


Figure 3. Package Outline Diagram

3.2 Package Marking

Refer to Figure 4. for the code marking location on the device package.



ABCD ➔ Date Code

XX ➔ Ass'y Lot Code (Option)

Figure 4. Package marking

4.0 System Level Description

4.1 System Overview

This section describes on how the chip being used to make up a complete system including the explanation on the 3rd party components and how they work with the chip.

The PAH8011ET is based on CMOS optical technology that is designed to meet the requirements of heart rate monitor accessories and wearables like smart watch or wrist band device. Figure 5 illustrates a system design for App Level diagram. The processor is accessing PPG data from PAH8011ET chip, then pass it to App level. APP level applies PixArt provided algorithm library to determine the heart rate data and waveform. Figure 6. illustrates a system design for Firmware Level diagram. The processor will also access PPG data from PAH8011ET chip, then perform heart rate calculation with PixArt algorithm library and send result to display or end device.

PAH8011ET can be configured to generate different frame rate settings.

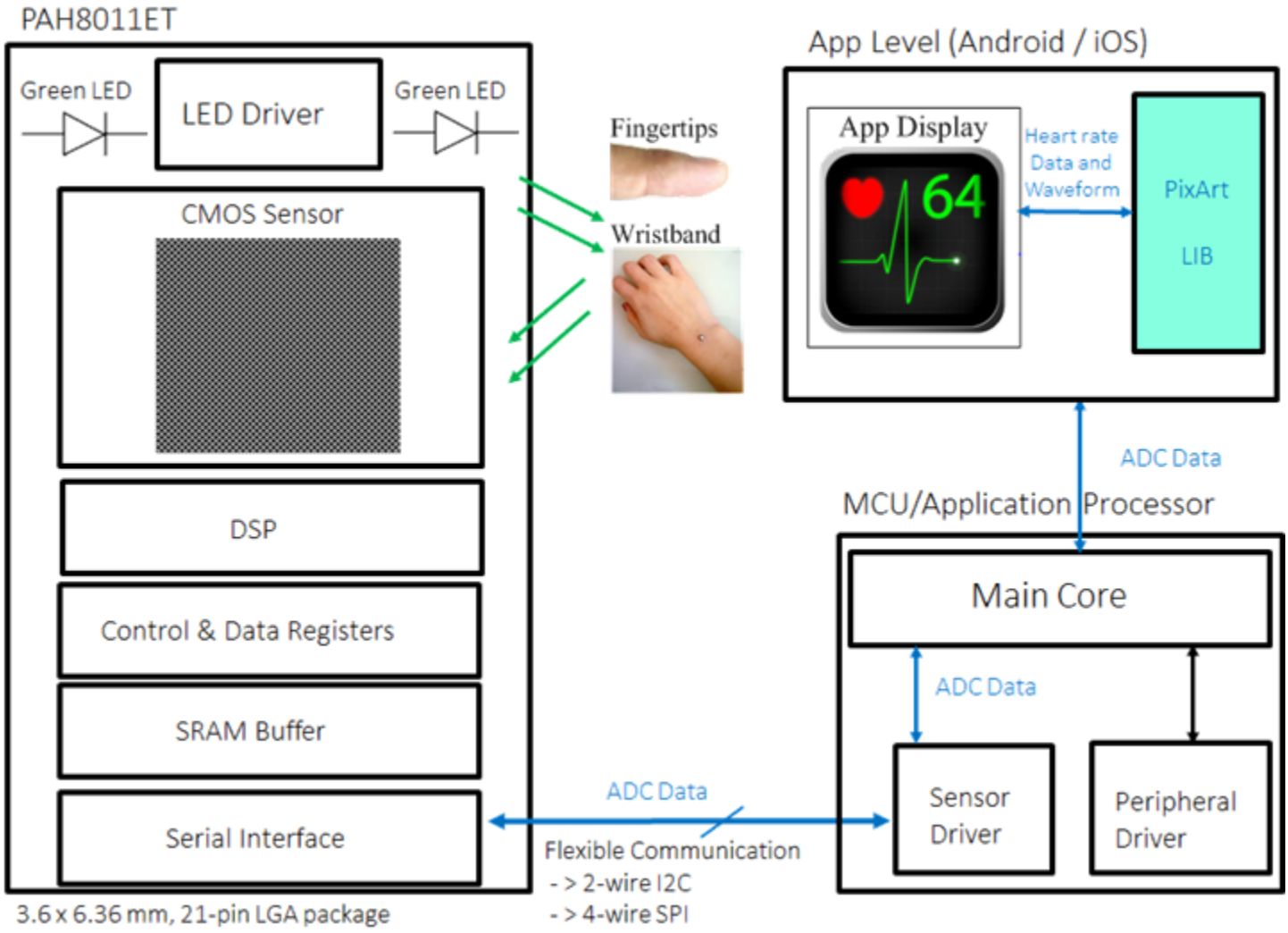


Figure 5. System Design for App Level

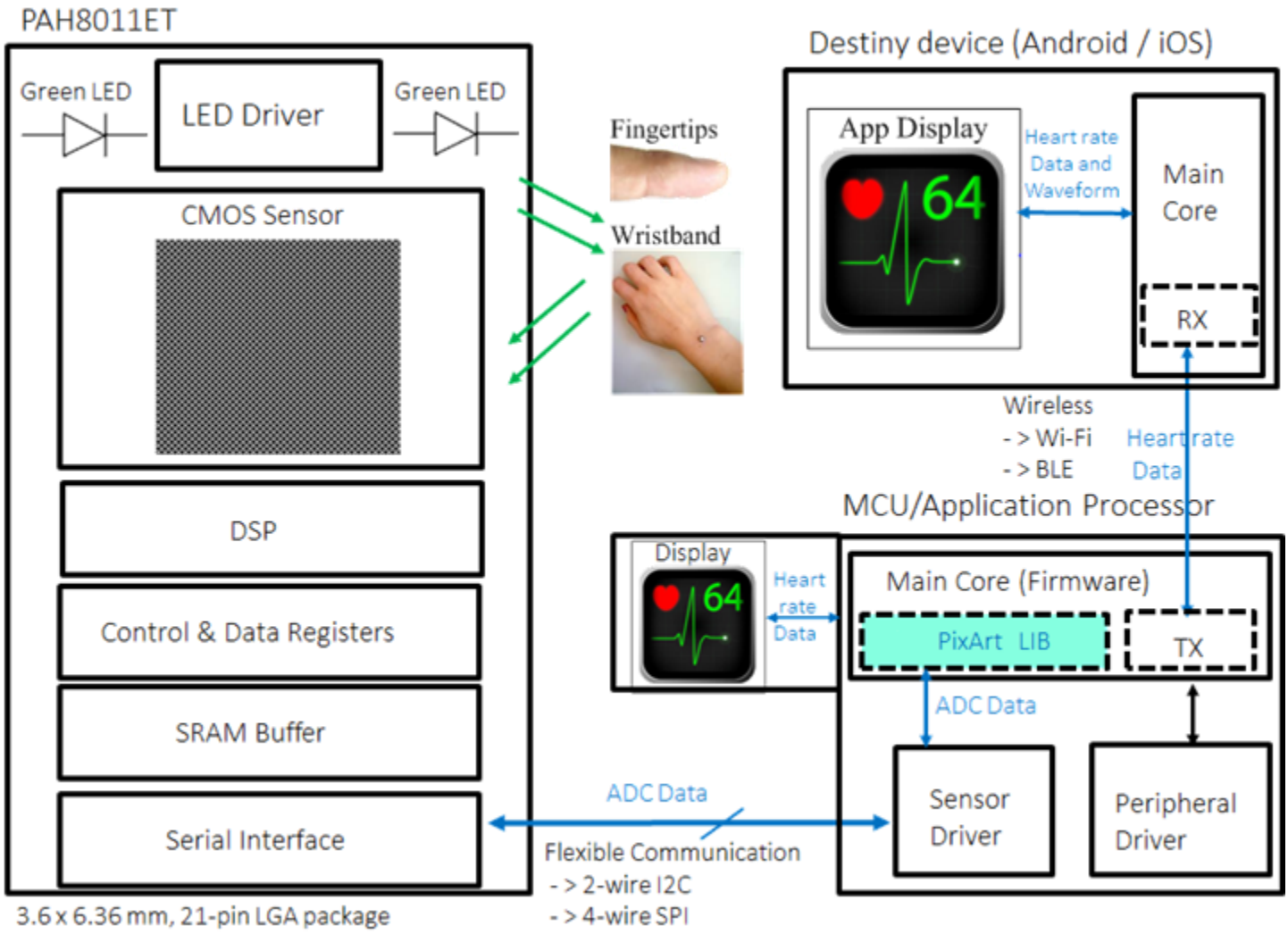


Figure 6. System Design for Firmware Level

4.2 Heart Rate Detection

Heart rate detection is an optical measurement technique that uses a light source and a detector to detect cardiovascular pulse wave that propagates through the body. The detected signal (pulse wave) called photoplethysmography and it is known as PPG/PTG. The PPG signal reflects the blood movement in the vessel, which goes from the heart to the fingertips through the blood vessels in a wave-like motion. Therefore, we can use this PPG signal to calculate heart rate.

This optical based technology could offer significant benefits in healthcare application as it is noninvasive, yet accurate and simple to use.

4.2.1 Applications

- Heart rate detection in general healthcare (Perfusion Index : Typ.1%)
- PPG Waveform

4.2.2 Heart Rate Detection Performance

Parameters	Value	Unit	Conditions
Heart Rate Measurement Range	30 – 240	bpm	
Heart Rate Tolerance of Average Root Mean Square (ARMS)	±3	bpm	@ Room temperature for steady state: 0 km/hr.
	±5	bpm	@ Room temperature for motion state: 0 – 9 km/hr on the treadmill.
Response Time	8 – 10	second	@ Heart Rate = 72/bpm

Notes:

- PAH8011ET can provide heart rate measurement. However, it is not for medical device usage.
- For usage of heart rate detection chip on the wearable device that to be put on the wrist, finger or palm,
  - The chip must be placed securely and in-contact with the skin surface as well as keeping it stable without any motion during measurement in acquiring accurate heart rate measurement.
  - Do not wear the device on the wrist bone. It should be wear on the higher position of, especially for those with a smaller wrist.
- Chip's performance is optimized with good blood flow. It is recommended to have light exercise for a few minutes to increase your blood flow before turning on the heart rate monitor.
- On cold weather condition or user is having poor blood circulation (e.g.: cold hands, fingers and feet), the chip performance (heart rate accuracy) could be effected as the blood flow is slower in the measuring spot position. It is recommended to activate the heart rate monitor in indoor use.
- If the chip is having problem to read heart rate, may try to swap it on the other side of hand wrist to repeat the measurement.
- For continuous heart rate measurement, do minimize hand movement and extreme bending of the wrist.

4.3 Reference Schematic

PAH8011ET-IP GGIR Package

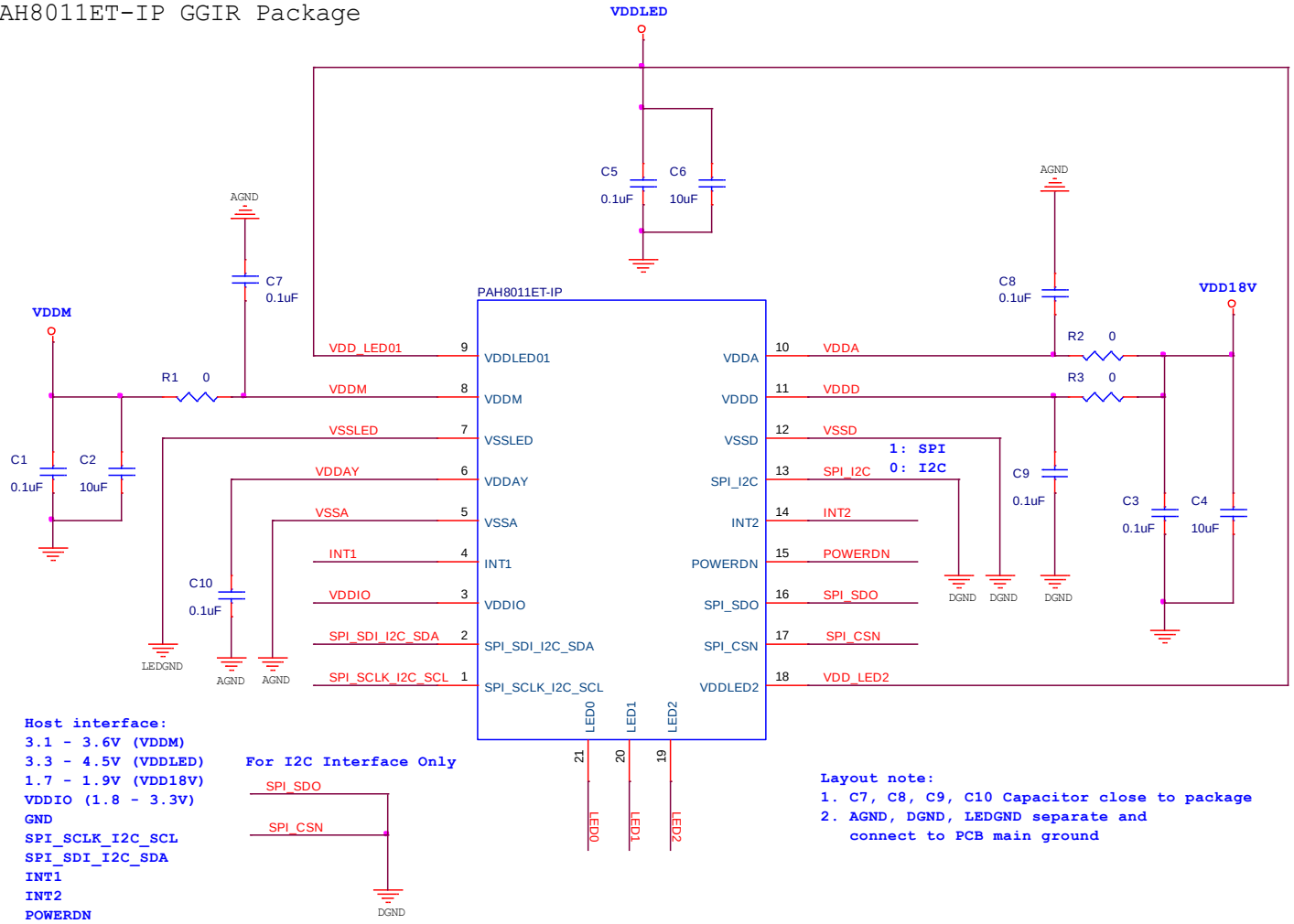


Figure 7. Reference Application Circuit

4.4 Design Guidelines

4.4.1 Schematic Design

1. VDDM & VDDIO & VDDLED: 3.3V, VDD18V: 1.8V (for 3.3V System)
2. VDDM & VDDLED: 3.3V~3.6V, VDDIO & VDD18V: 1.8V (for 1.8V System)
3. VDDM & VDDLED: 3.3V~3.6V, VDD18V: 1.8V, VDDIO: 2.8V (for 2.8V System)
4. It is recommended to separate the power system of VDDM/VDDLED and wireless system to avoid power interference.
5. The maximum load current of LDO (supplying power to VDDM/VDD18V/VDDLED/VDDIO) need to be larger than 250mA. For maximum current of each power rail, refer to IDDM_MAX, IDDLED_MAX, IDDD_MAX, IDDA_MAX, IDDIO_MAX and IDDAY_MAX parameters in Table 6. DC Electrical Specifications.
6. SPI_SDI_I2C_SDA and SPI_SCLK_I2C_SCL pull high to VDDIO with resistor for I^2C Only.
7. SPI_SDO and SPI_CSN pull down to GND for I2C Only.
8. SPI_SDI_I2C_SDA weakly pull high to VDDIO with resistor for SPI only when host is input mode at no IO toggle state.
9. VDDM, VDDD, VDDA, VDDAY must have 0.1µF capacitor connecting to GND and place closely to 8011.
10. The AGND, DGND and LEDGND must be separated and connected to PCB main GND.
11. INT1 pin is recommended to be connected to MCU HW INT as data ready INT for power saving.
12. INT2 pin is recommended to be connected to MCU HW INT for touch function.
13. Ensure that the VDDM, VDDLED, VDD18V's power noise should be under 100mV. (with 0.1µF and 10µF capacitor)
14. Tie SPI_I2C pin to VDDIO for SPI or tie to GND for I^2C.
15. At power on, VDDIO must be powered on equal to or first than VDD18V.
    Note: When VDDIO must be powered on first before VDDM, host should prevent using the I2C interface (connected with chip) to switch the LDO providing VDDM voltage.
16. At power off for 1.8V IO system, VDDM must be powered off first than VDD18V/VDDIO.
17. At power off for 2.8V/3.3V IO system, VDDIO and VDDM must be powered off first than VDD18V.
18. When 8011ET is not in use, entering POWER DOWN Mode.

4.4.2 Recommended PCB Layout

4.4.2.1 Pad Dimension on PCB/FPC

1. Pad size design:
   - If use solder mask defined (SMD), pad size is referred as solder mask opening size.
   - If use non-solder mask defined (non-SMD), pad size is referred as copper metal size.
2. Recommended dimension of pad is shown in Figure 8. The actual pad size design will need to consider components aside. (All dimension are mm)

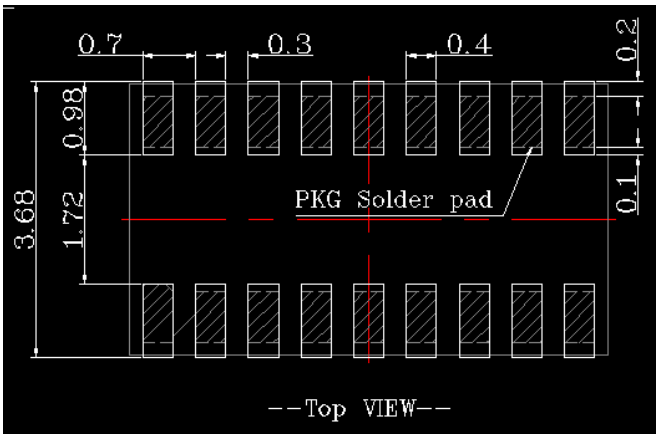


Figure 8. Recommended PCB Layout

4.4.2.2 If using FPC (Flex) board, stiffener is required to be added on the back of FPC (Flex) (at the other side of chip package area) to enhance the flex strength.

- Recommended stiffener type: FR4 or stainless steel.
- Recommended stiffener thickness: minimum 0.4mm for FR4 type, minimum 0.15mm for stainless steel.

4.4.2.3 Recommended use of 0.1~0.12mm thickness stencil for SMT process

- The stencil thickness selection will need to consider passive component size aside package.
- In case of the package is surface mounted on FPCB (Flexible Printed Circuit Boards), the overall thickness of cover layer & adhesive layer is recommenced to be controlled under than 40μm.

4.4.3 PCB Layout Guidelines

The following guidelines can be refer to Figure 9.

1. Trace width of VDDM, VDDIO, VDDLED, VDDA, VDDD, VDDAY traces must be at least 8 mils.
2. Capacitor 0.1μF must be placed close to the chip package.
3. The GND plane of GND of VSSA, VSSD and VSSLED must be layout separately and connected to the PCB's main GND.
4. If use FPC (Flex) board, recommend VSSLED pin separately to output pin, because of high LED current operation.

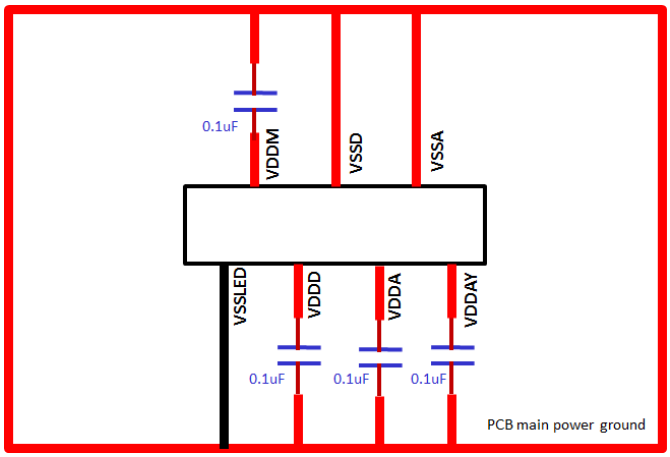


Figure 9. PCB Layout Guide

4.5 Recommend Guideline for PCB Assembly

Recommended Pb-free solder paste vender and type:

- Almit LFM-48W TM-HP
- Senju M705-GRN360-K

IR Reflow Soldering Profile can be referred to Figure 10. Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is:

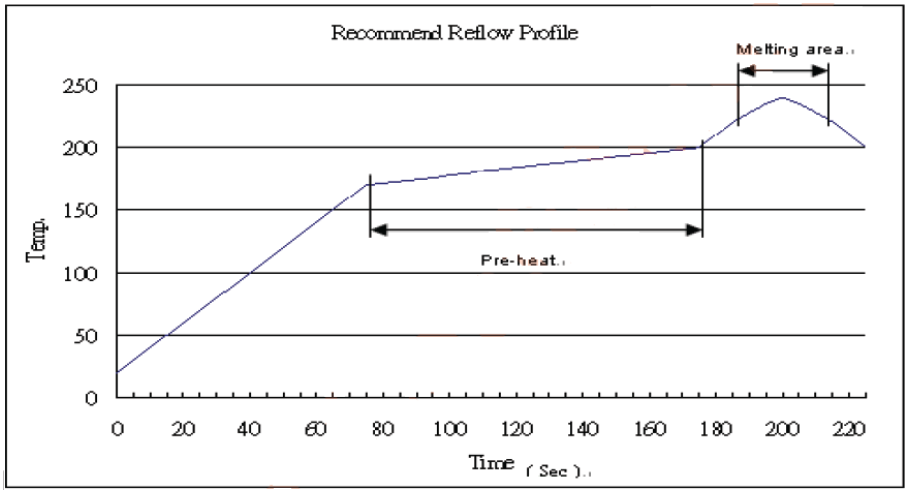


Figure 10. IR Reflow Soldering Profile

Note:

(1) Average Ramp-up Rate (30℃ to preheat zone): 1.5~2.5℃/Sec

(2) Preheat zone:

(2.1) Temperature ramp from 170~200℃

(2.2) Exposure time: 90 +/- 30 sec

(3) Melting zone:

(3.1) Melting area temperature > 220℃ for at least 30~50sec

(3.2) Peak temperature: 245℃

MS Level: MS Level 3

4.6 Packaging Information

4.6.1 Carrier Drawing

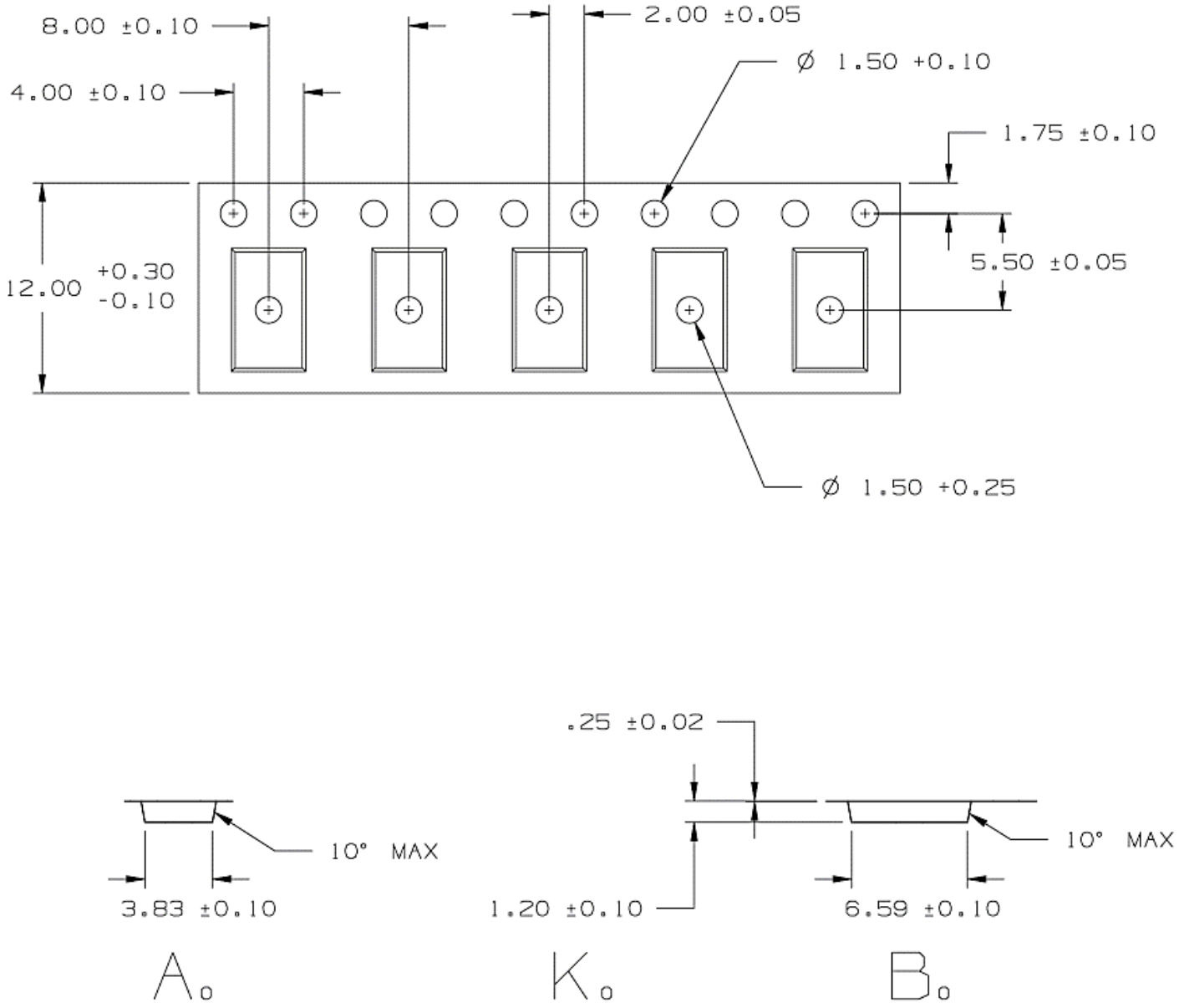


Figure 11. Carrier Drawing

4.6.2 Unit Orientation

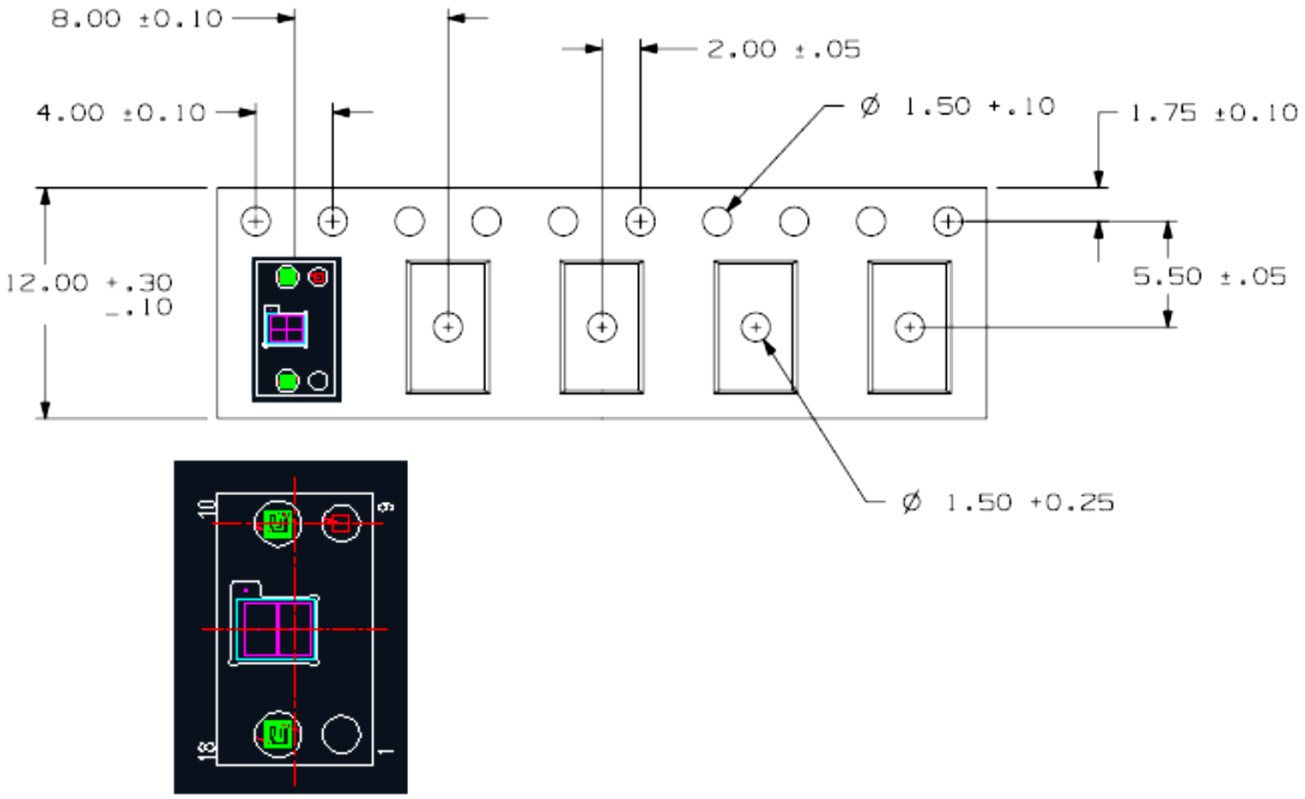


Figure 12. Unit Orientation

The maximum capacity of one packing box: One Inner packing box = 2500 units
Note: The Tape and Reel packing with vacuum pack is 1year storage available @ 25°C, 50%RH

5.0 Registers List

Table 7. Register Bank0

Note: Switch to Register Bank0 by writing 0x00 to Reg-0x7F

Address	Register Name	Access	Default	Address	Register Name	Access	Default
0x00	Product_ID_LB	RO	0x11	0x41	AE_ChB_InnerHiTarget_LB	R/W	0x00
0x01	Product_ID_HB	RO	0x80	0x42	AE_ChB_InnerHiTarget_HB	R/W	0x09
0x02	Version_ID	RO	0xB1	0x43	AE_ChB_InnerLoTarget_LB	R/W	0x00
0x13	AE_ChA_EnH	R/W	0x03	0x44	AE_ChB_InnerLoTarget_HB	R/W	0x07
0x14	AE_ChA_Item	R/W	0x1B	0x49	AE_ChB_LED_DAC_Max	R/W	0x3F
0x16	AE_ChA_ET_Max_LB	R/W	0xA0	0x4A	AE_ChB_LED_DAC_Min	R/W	0x01
0x17	AE_ChA_ET_Max_HB	R/W	0x00	0x51	AE_ChC_EnH	R/W	0x03
0x19	AE_ChA_ET_Min_LB	R/W	0x20	0x52	AE_ChC_Item	R/W	0x1B
0x1A	AE_ChA_ET_Min_HB	R/W	0x00	0x54	AE_ChC_ET_Max_LB	R/W	0xA0
0x1D	AE_ChA_ET_Step	R/W	0x08	0x55	AE_ChC_ET_Max_HB	R/W	0x00
0x1E	AE_ChA_OuterHiBound_LB	R/W	0x00	0x57	AE_ChC_ET_Min_LB	R/W	0x20
0x1F	AE_ChA_OuterHiBound_HB	R/W	0x0A	0x58	AE_ChC_ET_Min_HB	R/W	0x00
0x20	AE_ChA_OuterLoBound_LB	R/W	0x00	0x5B	AE_ChC_ET_Step	R/W	0x08
0x21	AE_ChA_OuterLoBound_HB	R/W	0x06	0x5C	AE_ChC_OuterHiBound_LB	R/W	0x00
0x22	AE_ChA_InnerHiTarget_LB	R/W	0x00	0x5D	AE_ChC_OuterHiBound_HB	R/W	0x0A
0x23	AE_ChA_InnerHiTarget_HB	R/W	0x09	0x5E	AE_ChC_OuterLoBound_LB	R/W	0x00
0x24	AE_ChA_InnerLoTarget_LB	R/W	0x00	0x5F	AE_ChC_OuterLoBound_HB	R/W	0x06
0x25	AE_ChA_InnerLoTarget_HB	R/W	0x07	0x60	AE_ChC_InnerHiTarget_LB	R/W	0x00
0x2A	AE_ChA_LED_DAC_Max	R/W	0x3F	0x61	AE_ChC_InnerHiTarget_HB	R/W	0x09
0x2B	AE_ChA_LED_DAC_Min	R/W	0x01	0x62	AE_ChC_InnerLoTarget_LB	R/W	0x00
0x32	AE_ChB_EnH	R/W	0x03	0x63	AE_ChC_InnerLoTarget_HB	R/W	0x07
0x33	AE_ChB_Item	R/W	0x1B	0x68	AE_ChC_LED_DAC_Max	R/W	0x3F
0x35	AE_ChB_ET_Max_LB	R/W	0xA0	0x69	AE_ChC_LED_DAC_Min	R/W	0x01
0x36	AE_ChB_ET_Max_HB	R/W	0x00	0x70	ChA_LED_Assign	R/W	0x01
0x38	AE_ChB_ET_Min_LB	R/W	0x20	0x71	ChB_LED_Assign	R/W	0x02
0x39	AE_ChB_ET_Min_HB	R/W	0x00	0x72	ChC_LED_Assign	R/W	0x04
0x3C	AE_ChB_ET_Step	R/W	0x08	0x73	ChA_Pixel_Assign	R/W	0x0F
0x3D	AE_ChB_OuterHiBound_LB	R/W	0x00	0x74	ChB_Pixel_Assign	R/W	0x0F
0x3E	AE_ChB_OuterHiBound_HB	R/W	0x0A	0x75	ChC_Pixel_Assign	R/W	0x0F
0x3F	AE_ChB_OuterLoBound_LB	R/W	0x00				
0x40	AE_ChB_OuterLoBound_HB	R/W	0x06				

Table 8. Register Bank1

Note: Switch to Register Bank1 by writing 0x01 to Reg-0x7F

Address	Register Name	Access	Default	Address	Register Name	Access	Default
0x00	ChT_Touch_Function	R/W	0x03	0x2B	ChA_ADC_Samp_Num	R/W	0x02
0x02	ChT_ExpoTime	R/W	0x28	0x2C	ChB_ADC_Samp_Num	R/W	0x02
0x03	ChT_LEDDAC	R/W	0x50	0x2D	ChC_ADC_Samp_Num	R/W	0x02
0x04	Touch_UpperTH_LB	R/W	0x00	0x2E	ADC_Normalized_EnL	R/W	0x00
0x05	Touch_UpperTH_HB	R/W	0x07	0x2F	Wr_Data_Truncate	R/W	0x0A
0x07	Touch_LowerTH_LB	R/W	0x00	0x30	TG_Enable	R/W	0x00
0x08	Touch_LowerTH_HB	R/W	0x06	0x35	INT_Type	R/W	0x3E
0x0A	Touch_Count_TH	R/W	0x01	0x36	INT_Mode_Sel	R/W	0x0E
0x0B	NoTouch_Count_TH	R/W	0x00	0x37	INT_Mask_Select	R/W	0x00
0x0D	ChT_LED_Assign	R/W	0x01	0x38	ChA_Auto_FramePeriod_EnH	R/W	0x01
0x0E	ChT_Pixel_Assign	R/W	0x10	0x3C	ChA_Auto_FP_Max_LB	R/W	0x80
0x11	ChT_Frame_Period	R/W	0x0A	0x3D	ChA_Auto_FP_Max_HB	R/W	0x02
0x12	ChT_Report_Divider_LB	R/W	0x14	0x3E	ChA_Auto_FP_Min _LB	R/W	0x14
0x13	ChT_Report_Divider_HB	R/W	0x00	0x3F	ChA_Auto_FP_Min _HB	R/W	0x00
0x14	ChT_ADC_Samp_Num	R/W	0x03	0x40	ChB_Auto_FramePeriod_EnH	R/W	0x01
0x15	ChA_Frame_Period_LB	R/W	0x28	0x44	ChB_Auto_FP_Max_LB	R/W	0x80
0x16	ChA_Frame_Period_HB	R/W	0x00	0x45	ChB_Auto_FP_Max_HB	R/W	0x02
0x17	ChB_Frame_Period_LB	R/W	0x28	0x46	ChB_Auto_FP_Min _LB	R/W	0x14
0x18	ChB_Frame_Period_HB	R/W	0x00	0x47	ChB_Auto_FP_Min _HB	R/W	0x00
0x19	ChC_Frame_Period_LB	R/W	0x28	0x48	ChC_Auto_FramePeriod_EnH	R/W	0x01
0x1A	ChC_Frame_Period_HB	R/W	0x00	0x4C	ChC_Auto_FP_Max_LB	R/W	0x80
0x1B	ChA_Frame_Samp_Num	R/W	0x04	0x4D	ChC_Auto_FP_Max_HB	R/W	0x02
0x1C	ChB_Frame_Samp_Num	R/W	0x04	0x4E	ChC_Auto_FP_Min _LB	R/W	0x14
0x1D	ChC_Frame_Samp_Num	R/W	0x04	0x4F	ChC_Auto_FP_Min _HB	R/W	0x00
0x21	ChA_Function	R/W	0x68	0x56	FIFO_RptNum_LB	R/W	0x29
0x23	ChB_Function	R/W	0x69	0x57	FIFO_RptNum_HB	R/W	0x00
0x24	Update_Flag	R/W	0x00	0x58	FIFO_AutoClearNum	R/W	0x14
0x25	ChC_Function	R/W	0x69	0x5A	FIFO_Data_Mode	R/W	0x03
0x26	Golden_Report_Divider_LB	R/W	0x40	0x5B	FIFO_Info_Mode	R/W	0x00
0x27	Golden_Report_Divider_HB	R/W	0x06	0x5D	LED0DAC_Man_Code	R/W	0x40
0x28	ChA_Report_Divider	R/W	0x01	0x5E	LED1DAC_Man_Code	R/W	0x40
0x29	ChB_Report_Divider	R/W	0x01	0x5F	LED2DAC_Man_Code	R/W	0x40
0x2A	ChC_Report_Divider	R/W	0x01	0x60	LEDDAC_Test_EnH	R/W	0x00

Table 9. Register Bank2

Note: Switch to Register Bank2 by writing 0x02 to Reg-0x7F

Address	Register Name	Access	Default	Address	Register Name	Access	Default
0x00	Read_Touch_Data_LB	RO	0x00	0x16	Read_ChA_ADC_Data_HB	RO	0x00
0x01	Read_Touch_Data_HB	RO	0x00	0x17	Read_ChB_ADC_Data_LB	RO	0x00
0x03	Read_ChA_ET_LB	RO	0x00	0x18	Read_ChB_ADC_Data_HB	RO	0x00
0x04	Read_ChA_ET_HB	RO	0x00	0x19	Read_ChC_ADC_Data_LB	RO	0x00
0x06	Read_ChB_ET_LB	RO	0x00	0x1A	Read_ChC_ADC_Data_HB	RO	0x00
0x07	Read_ChB_ET_HB	RO	0x00	0x1B	INT_Reg_Array	R/W	0x00
0x09	Read_ChC_ET_LB	RO	0x00	0x1C	Read_FIFO_Checksum_A	RO	0x00
0x0A	Read_ChC_ET_HB	RO	0x00	0x1D	Read_FIFO_Checksum_B	RO	0x00
0x0C	Read_ChA_LEDDAC	RO	0x00	0x1E	Read_FIFO_Checksum_C	RO	0x00
0x0D	Read_ChB_LEDDAC	RO	0x00	0x1F	Read_FIFO_Checksum_D	RO	0x00
0x0E	Read_ChC_LEDDAC	RO	0x00	0x20	Read_FIFO_Checksum_E	RO	0x00
0x0F	Read_ChA_FP_LB	RO	0x00	0x25	FIFO_RPTNUM_SYNC_LB	RO	0x00
0x10	Read_ChA_FP_HB	RO	0x00	0x26	FIFO_RPTNUM_SYNC_HB	RO	0x00
0x11	Read_ChB_FP_LB	RO	0x00	0x4B	TimeStamp_EnH	R/W	0x00
0x12	Read_ChB_FP_HB	RO	0x00	0x4E	TimeStamp_Data_A	RO	0x00
0x13	Read_ChC_FP_LB	RO	0x00	0x4F	TimeStamp_Data_B	RO	0x00
0x14	Read_ChC_FP_HB	RO	0x00	0x50	TimeStamp_Data_C	RO	0x00
0x15	Read_ChA_ADC_Data_LB	RO	0x00				

Register Bank3 are FIFO data, use interface to burst read Address 0x00 for acquiring FIFO data.

Note: Switch to Register Bank3 by writing 0x03 to Reg-0x7F

Table 10. Register Bank4

Note: Switch to Register Bank4 by writing 0x04 to Reg-0x7F

Address	Register Name	Access	Default
0x15	INT_Direction	R/W	0x0F
0x64	Global_Reset_N	R/W	0x01
0x65	TG_Reset_N	R/W	0x01
0x66	Reg_Reset_N	R/W	0x01
0x69	PD_Mode_EnH	R/W	0x00

Document Revision History

Revision Number	Date	Description
1.0	30 Jun 2017	Product Release version
1.1	22 Sep 2017	1. Update Unit Orientation Figure 2. Modify Recommended Layout PCB