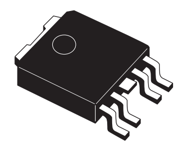
L4987Cxx

Very low drop voltage regulators with inhibit and dropout control flag

Features

- Very low dropout voltage (0.25 V typ.)
- Dropout control flag
- Very low quiescent current
- (Typ. 90 mA in OFF Mode, 500 mA in ON Mode)
- Output current up to 200 mA
- Logic-controlled electronic shutdown
- Output voltages of 3.3 V, 5 V
- Internal current and thermal limit
- Only 2.2 µF for stability
- Available in ± 2% selection at 25°C
- Supply voltage rejection: 70 dB (typ.)



PPAK

Description

The L4987 is a very low drop regulator available in PPAK. The very low drop-voltage (0.5 V Max at 200 mA) and the very low quiescent current make it particularly suitable for low noise, low power applications, and in battery powered systems. The input dump protection up to 40 V makes it ideal for automotive applications, a shutdown Logic Control function is available (pin 2, TTL compatible). This means that when the device is used as a local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. The regulator employs an output pin (open collector) providing a logic signal when the pass transistor is in saturation at low input voltage, this signal can be used to prevent the pop-up phenomenon in the car radio. In battery powered systems (the cellular phone, notebook) it is possible to use the flag to monitor the battery charge status through the dropout of the regulator.

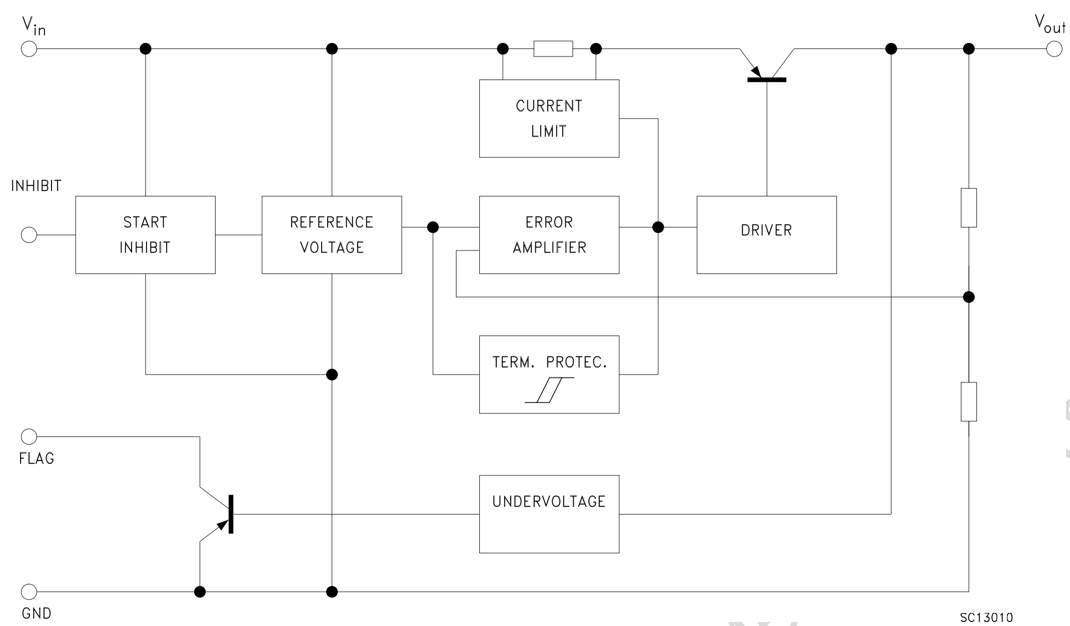
Table 1. Device summary

Part number	Order code	Output voltage
L4987Cxx33	L4987CPT33TR	3.3 V
L4987Cxx50	L4987CPT50TR	5.0 V

Contents

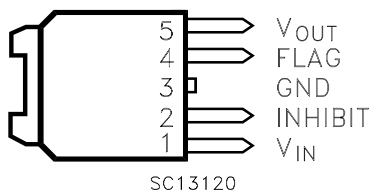
1 Schematic diagram

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin connections (top view)



3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC Input voltage	40	V
I_O	Output current	Internally Limited	
P_{tot}	Power dissipation	Internally Limited	
T_{stg}	Storage temperature range	-40 to 150	°C
T_{op}	Operating junction temperature range	-40 to 125	°C

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

Table 3. Thermal data

Symbol	Parameter	PPAK	Unit
R_{thJC}	Thermal resistance junction-case	8	°C/W
R_{thJA}	Thermal resistance junction-ambient	100	°C/W

4 Electrical characteristics

Table 4. Electrical characteristics of L4987Cxx33 (refer to the test circuits, V_I = 6.3 V, I_O = 5 mA, T_J = 25°C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 200 mA, V_I = 6.3 V	3.234	3.3	3.366	V
		I_O = 200 mA, V_I = 6.3 V, T_J=-40 to 125°C	2.76		3.432	
V_I	Operating input voltage	I_O = 200 mA	4		18	V
I_{out}	Output current limit		250			A
ΔV_O	Line regulation	V_I = 4.6 to 18 V, I_O = 0.5 mA		2.4	14	mV
ΔV_O	Load regulation	V_I = 4.4 V, I_O = 0.5 to 200 mA		3	20	mV
I_d	Quiescent current ON MODE	V_I = 4.6 to 18 V, I_O = 0 mA		0.7	1	mA
		V_I = 4.6 to 18 V, I_O = 200 mA		1.5	6	
	OFF MODE	V_I = 12 V		90	180	µA
SVR	Supply voltage rejection	I_O = 5 mA, V_I = 5.6 ± 1 V, f = 120 Hz		80		dB
		f = 1 KHz		75		
		f = 10 KHz		60		
V_d	Dropout voltage	I_O = 200 mA		0.25	0.5	V
		I_O = 200 mA, T_J=-40 to 125°C			0.7	
V_{IL}	Control input logic low	T_J = -40 to 125°C			0.8	V
V_{IH}	Control input logic high	T_J = -40 to 125°C	2			V
I_I	Control input current			10		µA
C_O	Output bypass capacitance	ESR = 0.5 to 10 Ω, I_O = 0 to 200 mA, T_J= -40 to 125°C	2	10		µF
V_{FL}	Control flag output low	V_I - V_O < V_{CESAT} power, I_{FL} = 6mA, I_O = 200mA			0.5	V
I_{FH}	Control flag output high leakage current	V_I > 4 V, V_{OH} = 15 V			10	µA

Table 5. Electrical characteristics of L4987Cxx50 (refer to the test circuits, V_I = 8 V, I_O = 5 mA, T_J = 25°C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 200 mA, V_I = 8 V	4.9	5	5.1	V
		I_O = 200 mA, V_I = 8 V, T_J = - 40 to 125°C	4.8		5.2	
V_I	Operating input voltage	I_O = 200 mA	5.7		18	V
I_{out}	Output current limit		250			A
ΔV_O	Line regulation	V_I = 6.3 to 18 V, I_O = 0.5 mA		3	20	mV
ΔV_O	Load regulation	V_I = 6.3 V, I_O = 0.5 to 200 mA		3	20	mV
I_d	Quiescent current ON MODE	V_I = 6.3 to 18 V, I_O = 0 mA		0.7	1	mA
		V_I = 6.3 to 18 V, I_O = 200 mA		1.5	6	
	OFF MODE	V_I = 12 V		90	180	µA
SVR	Supply voltage rejection	I_O = 5 mA, V_I = 7.3 ± 1 V; f = 120 Hz		76		dB
		f = 1 KHz		71		
		f = 10 KHz		58		
V_d	Dropout voltage	I_O = 200 mA		0.3	0.5	V
		I_O = 200 mA, T_J = -40 to 125°C			0.7	
V_{IL}	Control input logic low	T_J = -40 to 125°C			0.8	V
V_{IH}	Control input logic high	T_J = -40 to 125°C	2			V
I_I	Control input current			10		µA
C_O	Output bypass capacitance	ESR = 0.5 to 10 Ω, I_O = 0 to 200 mA T_J= -40 to 125°C	2	10		µF
V_{FL}	Control flag output low	V_I - V_O < V_{CESAT} power, I_{FL} = 6 mA I_O = 200 mA			0.5	V
I_{FH}	Control flag output high leakage current	V_I > 5.85 V, V_{OH} = 15 V			10	µA

5 Typical characteristics

(Unless otherwise specified $T_J = 25°C$, $C_I = C_O = 0.1\ \mu F$)

Figure 3. Output and flag voltage vs input voltage

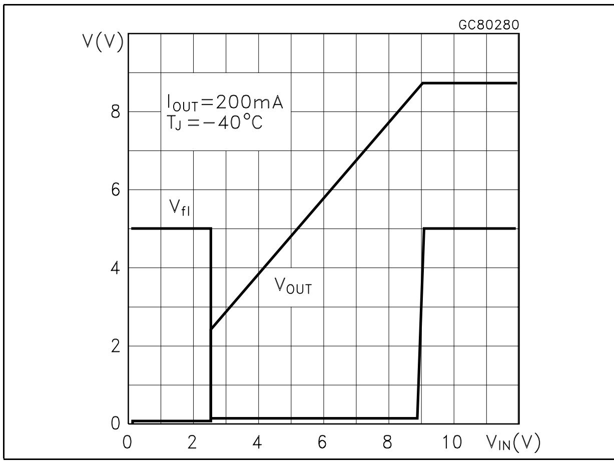


Figure 4. Output voltage vs input voltage

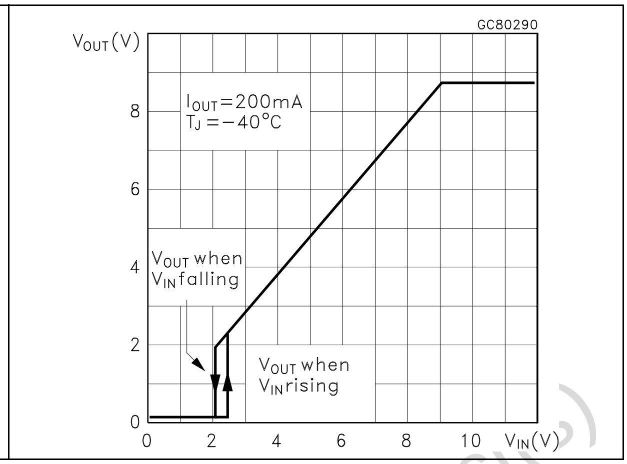


Figure 5. Output and flag voltage vs input voltage

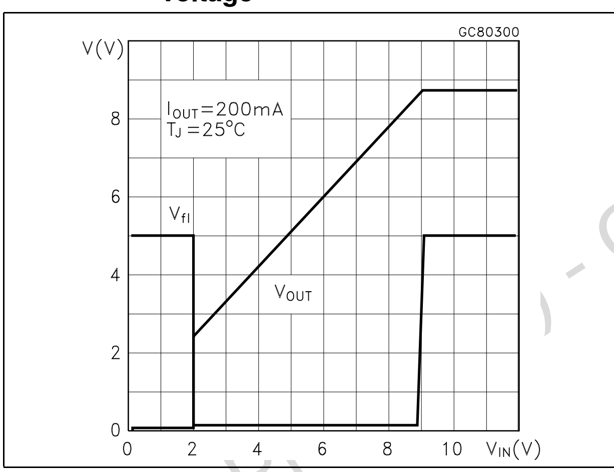


Figure 6. Output voltage vs input voltage

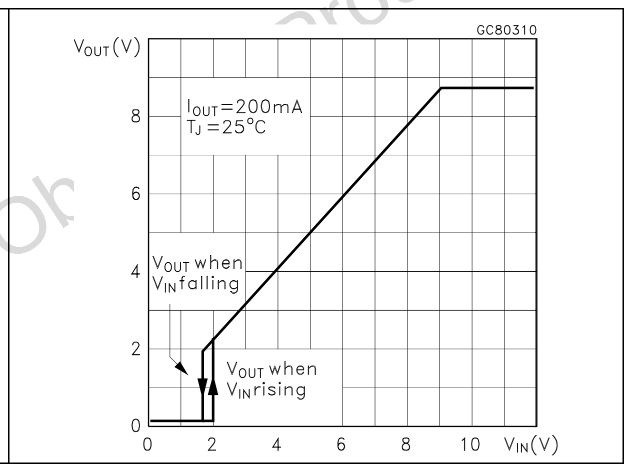


Figure 7. Output and flag voltage vs inp. volt.

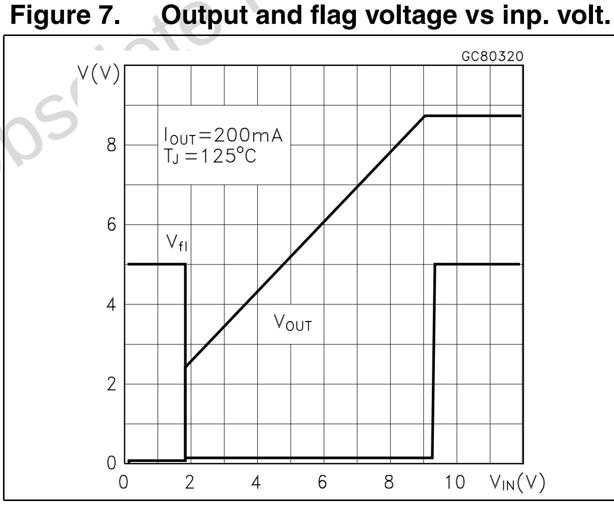
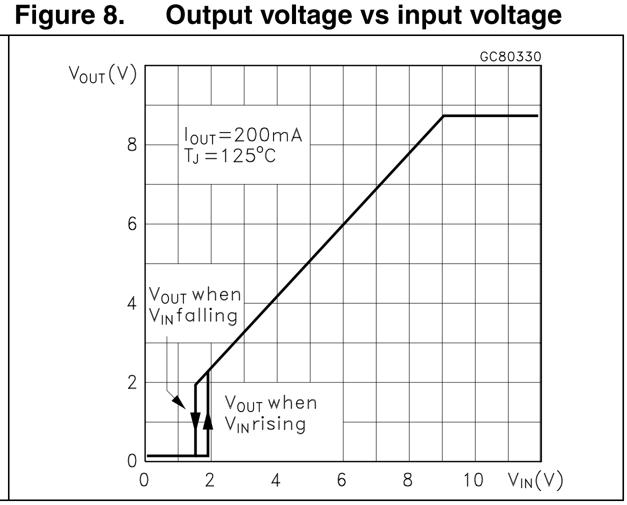


Figure 8. Output voltage vs input voltage



6 Application hint of L4987CPT33

6.1 How to use the control flag

The flag produces a logic "low" whenever the output drops out of regulation. An "out of regulation condition can result from:

1) Low input voltage ($V_{IN} \leq V_{OUT} + V_{DROP}$)

2) Current limiting

3) Thermal limiting

Figure 3. to *Figure 4.* show the typical behavior of the output voltage and the control flag versus the input voltage and the temperature. No hysteresis is implemented; so the response of V_{OUT} and V_{FLAG} are the same either when the V_{IN} ramps up or down.

The control flag is an open collector which requires an external pull-up resistor. This may be connected to the regulator output (*Figure 11.*) or some other supply voltage (*Figure 12.*).

Using the regulator output prevents an invalid "high" on the flag which occurs if it is pulled up to an external voltage while the regulator input voltage is reduced below about 2 V (*Figure 13.*).

Concerning the pull-up resistor its value must be properly chosen as suggested below. When "low" as it is possible to see in *Figure 7.* the control flag voltage is:

$V_{FLAG(LOW)} = V_{CE} = 0.5 = V_{SUPPLY} - R_{PULL} \times I_{FL}$

V_{SUPPLY} is chosen by design and, thus is known, while I_{FL} must be at maximum 10 mA.

Then 0.5 V $\geq V_{SUPPLY} - R_{PULL} \times$ 10 mA

The minimum value of R_{PULL}, is, so, determined by the following equation:

$R_{PULL(min)} \geq V_{SUPPLY}$ - 0.5/10 mA

Regarding the maximum value of R_{PULL} note that its value depends of the type of logic used (CMOS, TTL etc.), the transistor leakage current and the presence or not of a load on V_{FLAG}.

The following example shows how to determine the R_{PULL} max in the case of CMOS logic, no load and 10 µA (for L4987 it is the maximum value of I_{FH}) of control flag leakage current.

Because of CMOS logic:

$V_{FLAG(HIGH)} \geq 2/3\ V_{SUPPLY}$

but:

$V_{FLAG(HIGH)} = V_{SUPPLY} - R_{PULL} \times I_{FH} \geq 2/3\ V_{SUPPLY}$

so, the maximum value is determined by the following equation:

$R_{PULL(MAX)} \leq (1/3\ V_{SUPPLY})/10$ mA

Figure 9. Output and flag voltage vs input

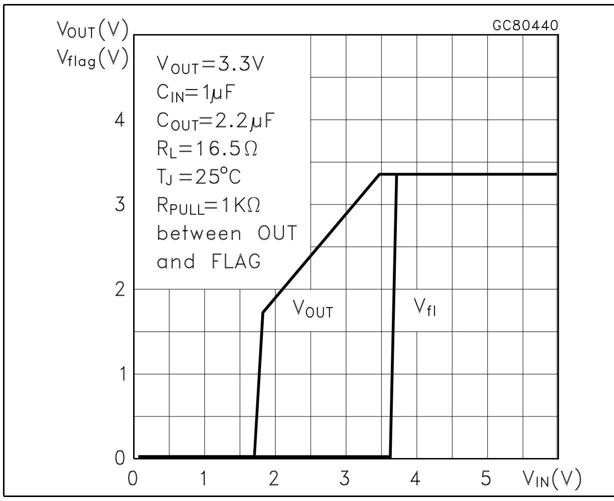
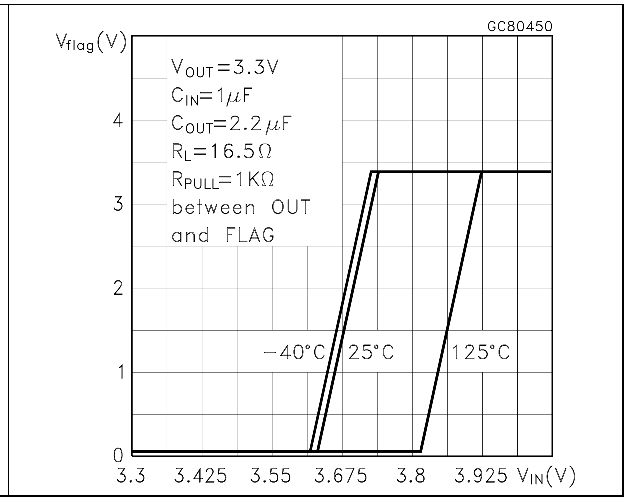


Figure 10. Flag voltage vs input



7 Test circuits

Figure 11. Test circuit

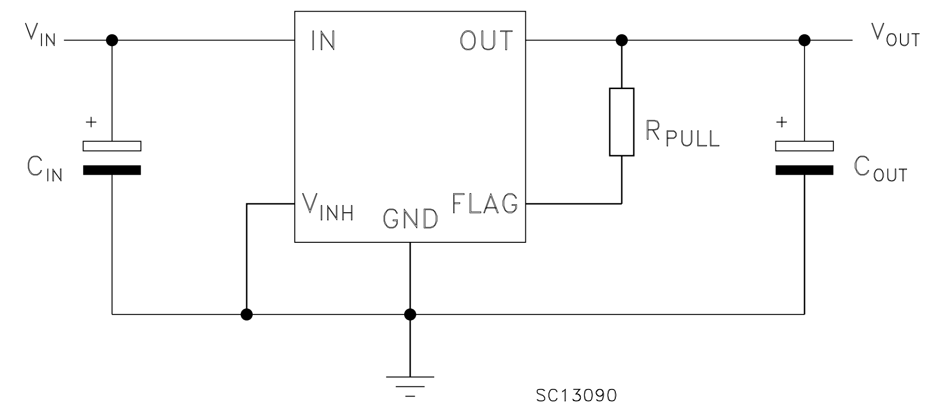


Figure 12. Single antenna receiver with master receiver port

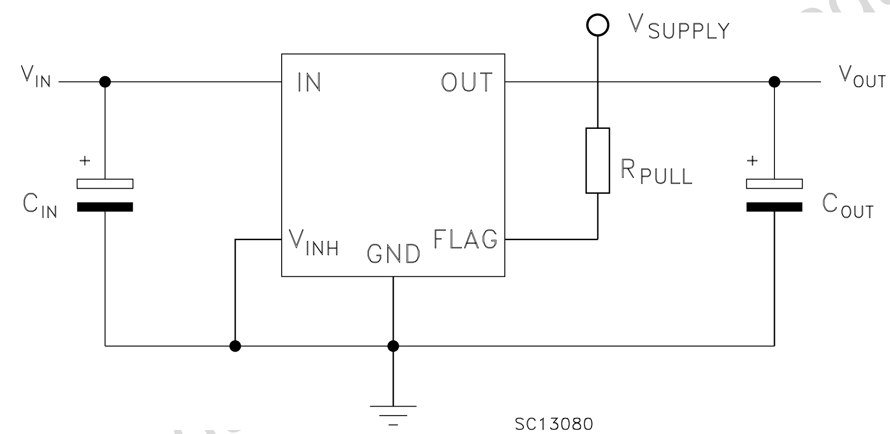


Figure 13. Equivalent output circuit

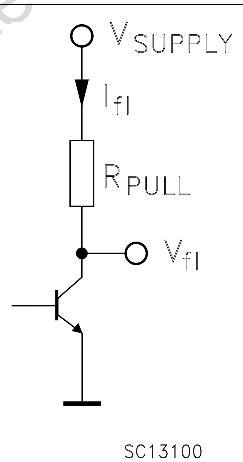
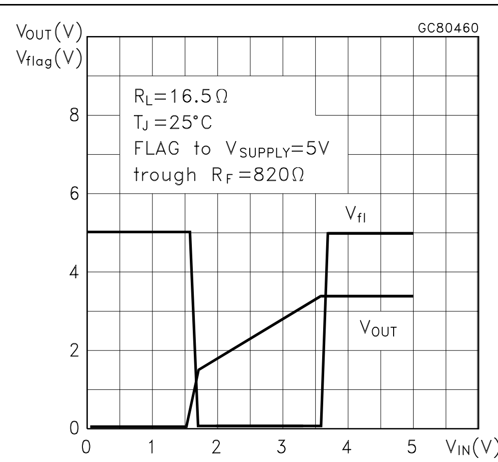


Figure 14. Output and flag voltage vs input

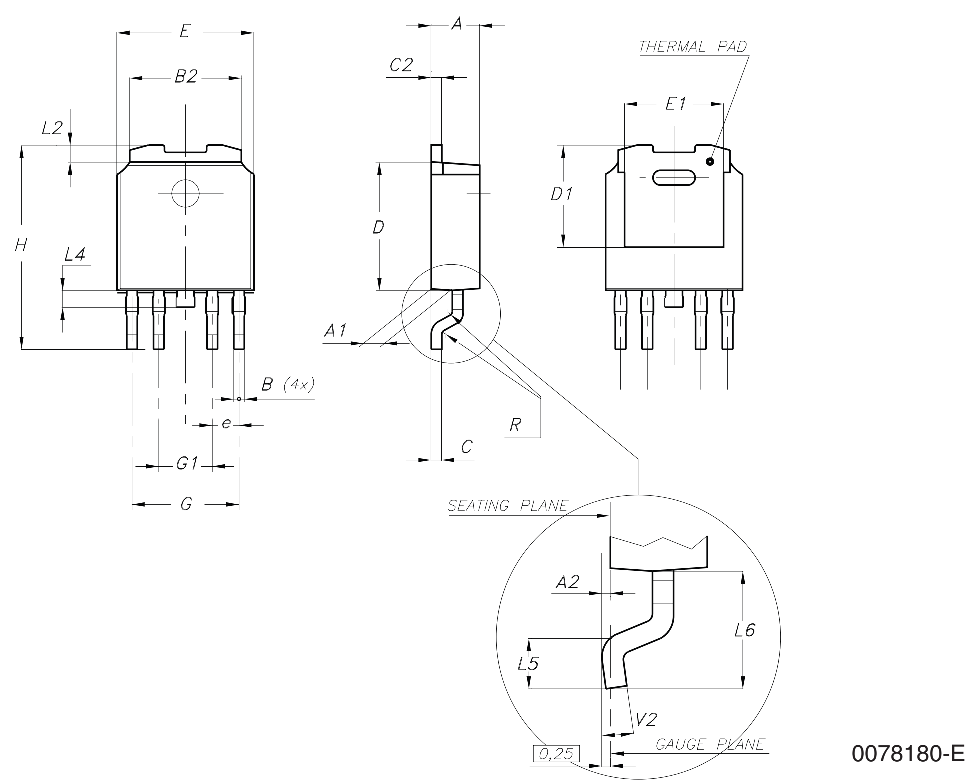


8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

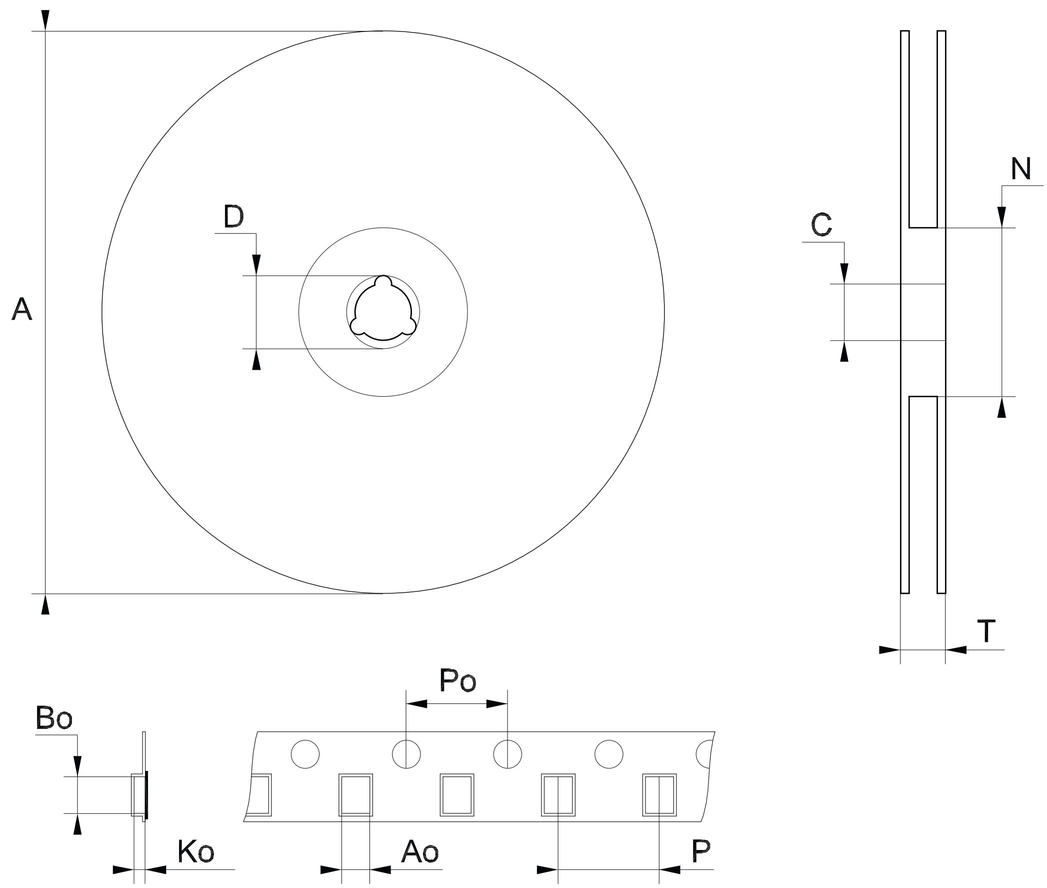
PPAK mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.4		0.6	0.015		0.023
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.201	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		1.27			0.050	
G	4.9		5.25	0.193		0.206
G1	2.38		2.7	0.093		0.106
H	9.35		10.1	0.368		0.397
L2		0.8	1		0.031	0.039
L4	0.6		1	0.023		0.039
L5	1			0.039		
L6		2.8			0.110	



Tape & reel DPAK-PPAK mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.80	6.90	7.00	0.268	0.272	0.2.76
Bo	10.40	10.50	10.60	0.409	0.413	0.417
Ko	2.55	2.65	2.75	0.100	0.104	0.105
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	7.9	8.0	8.1	0.311	0.315	0.319



Note: Drawing not in scale

9 Revision history

Table 6. Document revision history

Date	Revision	Changes
22-Jun-2004	4	V_O min and V_O max values in Table 5, pag. 4 have been corrected.
04-Sep-2006	5	The I_{FH} value on table 7 has been updated and new template.
26-Sep-2007	6	Add *Table 1.* in cover page.