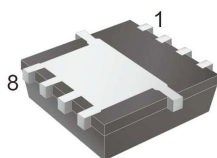


PDFN 5x6



**Pin Definition:**

- |           |          |
|-----------|----------|
| 1. Source | 8. Drain |
| 2. Source | 7. Drain |
| 3. Source | 6. Drain |
| 4. Gate   | 5. Drain |

# TSM35N03PQ56

## 30V N-Channel Power MOSFET

**PRODUCT SUMMARY**

V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (mΩ)	I <sub>D</sub> (A)
30	7 @ V <sub>GS</sub> =10V	12
	9 @ V <sub>GS</sub> =4.5V	10

**Features**

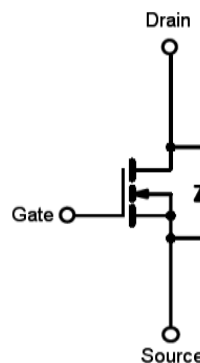
- Advanced Trench Technology
- Low On-Resistance
- Low gate charge typical @ 8.2nC (Typ.)
- Low Crss typical @ 90pF (Typ.)

**Ordering Information**

Part No.	Package	Packing
TSM35N03PQ56 RLG	PDFN56	2.5Kpcs / 13" Reel

**Note:** "G" denote for Halogen Free Product

**Block Diagram**



N-Channel MOSFET

**Absolute Maximum Ratings** (T<sub>a</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	±25	V
Continuous Drain Current	I <sub>D</sub>	T <sub>C</sub> =25°C	35
		T <sub>C</sub> =70°C	35
		T <sub>A</sub> =25°C	22
		T <sub>A</sub> =70°C	18
Drain Current-Pulsed Note 1	I <sub>DM</sub>	60	A
Avalanche Current, L=0.5mH	I <sub>AS</sub> , I <sub>AR</sub>	26	A
Avalanche Energy, L=0.5mH	E <sub>AS</sub> , E <sub>AR</sub>	33	mJ
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> =25°C	35
		T <sub>C</sub> =70°C	23
		T <sub>A</sub> =25°C	4.2
		T <sub>A</sub> =70°C	2.7
Storage Temperature Range	T <sub>STG</sub>	-55 to +150	°C
Operating Junction Temperature Range	T <sub>J</sub>	-55 to +150	°C

\* Limited by maximum junction temperature

**Thermal Performance**

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	Rθ <sub>JC</sub>	3.5	°C/W
Thermal Resistance - Junction to Ambient	Rθ <sub>JA</sub>	30	°C/W

Notes: Surface mounted on FR4 board t ≤ 10sec

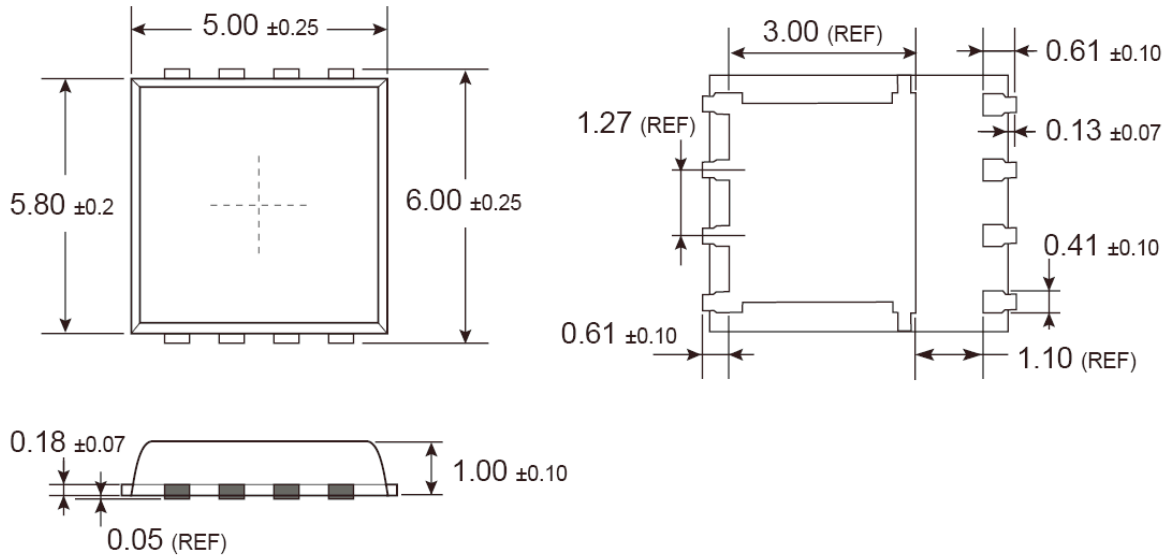
### Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	30	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 12A$	$R_{DS(ON)}$	--	5.5	7	mΩ
	$V_{GS} = 4.5V, I_D = 10A$		--	7.5	9	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	1.3	--	2.5	V
Zero Gate Voltage Drain Current	$V_{DS} = 24V, V_{GS} = 0V$	$I_{DSS}$	--	--	1	μA
Gate Body Leakage	$V_{GS} = \pm 25V, V_{DS} = 0V$	$I_{GSS}$	--	--	±100	nA
<b>Dynamic</b>						
Total Gate Charge	$V_{DS} = 15V, I_D = 16A,$ $V_{GS} = 4.5V$	$Q_g$	--	8.2	--	nC
Gate-Source Charge		$Q_{gs}$	--	2.7	--	
Gate-Drain Charge		$Q_{gd}$	--	2.2	--	
Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ $f = 1.0MHz$	$C_{iss}$	--	1050	--	pF
Output Capacitance		$C_{oss}$	--	210	--	
Reverse Transfer Capacitance		$C_{rss}$	--	90	--	
<b>Switching</b>						
Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 15V,$ $R_G = 1\Omega$	$t_{d(on)}$	--	9	--	ns
Turn-On Rise Time		$t_r$	--	9	--	
Turn-Off Delay Time		$t_{d(off)}$	--	20	--	
Turn-Off Fall Time		$t_f$	--	7	--	
<b>Drain-Source Diode Characteristics and Maximum Rating</b>						
Drain-Source Diode Forward Voltage	$V_{GS}=0V, I_S=2.3A$	$V_{SD}$	--	0.75	1.3	V
Reverse Recovery Time	$I_S = 3.2A, T_J=25^\circ C$ $dI/dt = 100A/\mu s$	$t_{fr}$	--	22	--	ns
Reverse Recovery Charge		$Q_{fr}$	--	14	--	nC

#### Notes:

1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
2.  $R\theta_{JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R\theta_{JC}$  is guaranteed by design while  $R\theta_{CA}$  is determined by the user's board design.  $R\theta_{JA}$  shown below for single device operation on FR-4 in still air
3. The maximum current rating is limited by package.

## PDFN56 Mechanical Drawing



Unit: Millimeters

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