MagnaChip

Datasheet – MSI2206

Dual Channel 6A Load Switch

General Description

The MSI2206 is a dual-channel, low Ron N-channel MOSFET with controlled turn-on.

The input voltage range operates from 0.8V to 5.5VDC and can support a maximum continuous current of 6A per channel. Each channel is independently controlled by an EN1 and EN2.

In device, a 220Ω on-chip load resistor is added for quick output discharge when switch is turned off.

The device is packaged 2mm x 3mm, DFN-14Lead with thermal pad for high power dissipation.

Features

- Integrated Dual-Channel Load Switch
- Wide Input Voltage : 0.8V to 5.5V
- Low $R_{DS(ON)}$: 18 mΩ (Typ.)
- 6A Maximum Continuous Current per Channel
- Low Quiescent Current
  - 80uA (Both Channel)
  - 60uA (Single Channel)
- Controllable Rise Time
- Quick Output Discharge (QOD)
- DFN 14-pin Package with Thermal Pad
- ESD Protected
  - Human Body Model : > 2.0kV
  - Charged Device Model : > 1.0kV

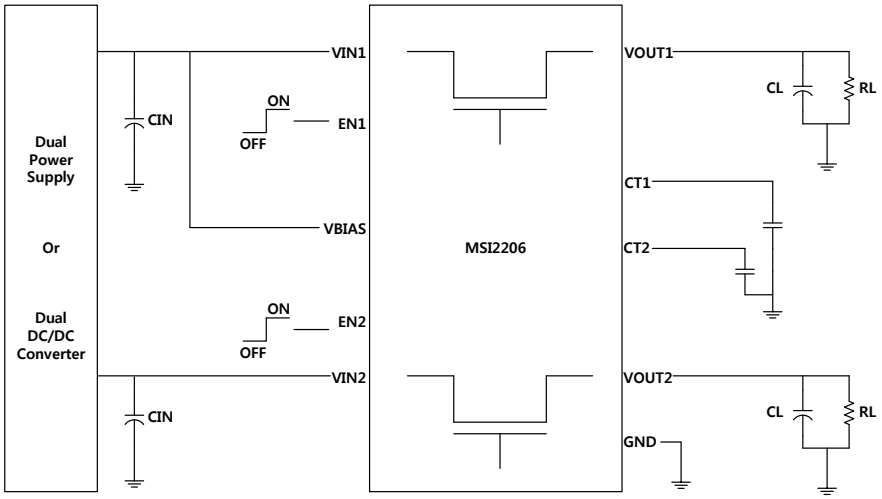
Applications

- Ultrabook™
- Notebooks/Netbooks
- Tablet PC
- Consumer Electronics
- Set-top Boxes / Residential Gateways
- Telecom Systems
- Solid State Drive (SSD)

Ordering Information

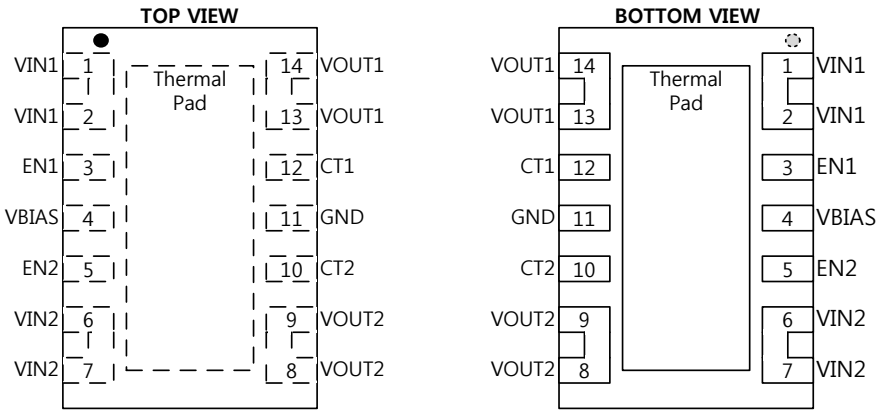
Part Number	Top Marking	Ambient Temperature Range	Package	RoHS Status
MSI2206DFRH	2206 YWLL	-40℃ to +85℃	2 mm X 3 mm DFN-14 Lead	Halogen Free Pb-Free

Typical Application



Pin Configuration

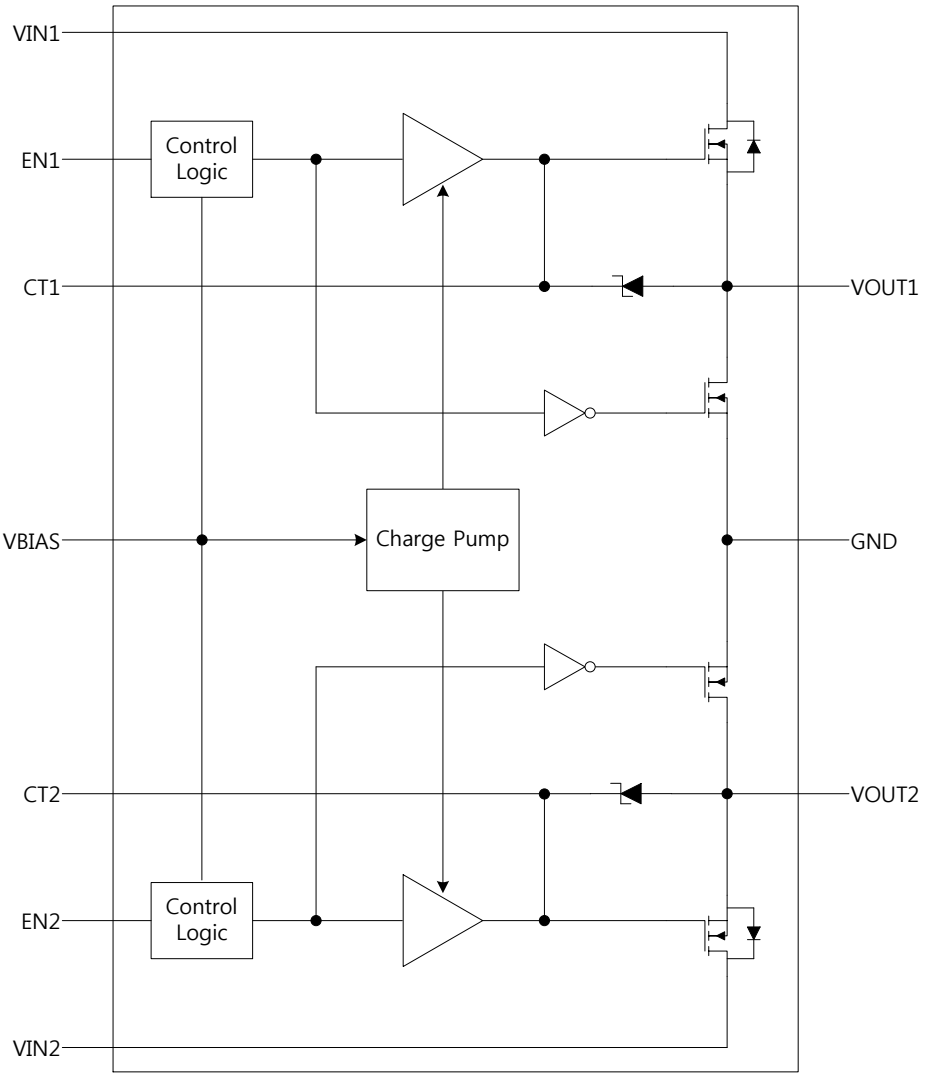
Top View and Bottom View



Pin Description

Name	No.	Description
VIN1	1, 2	Switch #1 Input
VIN2	6, 7	Switch #2 Input
VOUT1	13,14	Switch #1 Output
VOUT2	8, 9	Switch #2 Output
VBIAS	4	Bias Voltage. Power supply to device.
EN1	3	Active high switch #1 control input. Do not leave floating
EN2	5	Active high switch #2 control input. Do not leave floating
CT1	12	Switch #1 Slew rate control. Can be left floating.
CT2	10	Switch #2 Slew rate control. Can be left floating.
GND	11	Ground
Thermal Pad	15	Thermal pad to alleviate thermal stress. Tie to GND.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Min	Max	Unit
V_{IN}	VIN1, VIN2 to GND	-0.3	6.0	V
V_{OUT}	VOUT1, VOUT2 to GND	-0.3	6.0	V
V_{BIAS}	VBIAS to GND	-0.3	6.0	V
V_{EN}	EN1, EN2 to GND	-0.3	6.0	V
V_{CT}	CT1, CT2 to GND	-0.3	20	V
I_{SW}	Maximum Continuous Switch Current		6.0	A
T_{STG}	Storage Junction Temperature	-65	+150	°C
T_A	Operating Temperature Range	-40	+85	°C
ESD	HBM on All Pins (Note 2)	2.0		kV
	CDM on All Pins (Note 3)	1.0		

Note 1: Stresses beyond the above listed maximum ratings may damage the device permanently. Operating above the recommended conditions for extended time may stress the device and affect device reliability. Also the device may not operate normally above the recommended operating conditions. These are stress ratings only.
Note 2: ESD tested per JESD22-A114C.
Note 3: ESD tested per JESD22-C101E

Recommended Operating Conditions (Note 1)

Symbol	Parameter	Min	Max	Unit
$V_{IN1,2}$	Supply Input Voltage	0.8	V_{BIAS}	V
V_{BIAS}	Bias Voltage Range	2.5	5.5	V
$V_{OUT1,2}$	Output Voltage Range		$V_{IN1,2}$	V
EN1,2	Enable Logic High Voltage	1.2	5.5	V
	Enable Logic Low Voltage	0	0.4	V
$C_{IN1,2}$	Input Capacitor	1.0		uF
T_A	Ambient Temperature (Note 2)	-40	85	℃

Note 1: Normal Operation of the device is not guaranteed if operating the device over outside range of recommended conditions.
Note 2: The ambient temperature may have to be derated if used in high power dissipation and poor thermal resistance conditions.

Package Thermal Resistance

Parameter	MIN	MAX	Unit
θ_{JA} , 2.0 mm X 3.0 mm DFN-14 Lead (Note1)	60		℃/W

Note 1: Measured using 2S2P JEDEC std. PCB

Electrical Characteristics

Minimum and maximum limits apply for –40°C ≤ T_A ≤85°C. Typical values are at V_{BIAS} = 5.0V and T_A = 25°C (Unless otherwise noted)

Parameter		Test Condition		Min	Typ.	Max	Unit
SUPPLY OPERATION							
V_{IN1} V_{IN2}	Input voltage range	V_{BIAS}=2.5~5.5V, V_{IN}≤V_{BIAS}		0.8		5.5	V
I_{BIAS_ON} (SINGLE)	V_{BIAS} Quiescent Current (Single Channel)	I_{OUT1}=I_{OUT2}=0mA, V_{EN2}=0V $V_{IN1,2}$=V_{EN1}=V_{BIAS}=5.0V			60		uA
$I_{BIAS\_ON\ (BOTH)}$	V_{BIAS} Quiescent Current (Both Channel)	I_{OUT1}=I_{OUT2}=0mA, $V_{IN1,2}$=$V_{EN1,2}$=V_{BIAS}=5.0V			80	120	uA
I_{BIAS_SHDN}	V_{BIAS} Shutdown Current	$V_{EN1,2}$=0V, $V_{OUT1,2}$=0V				2	uA
I_{IN_OFF}	VIN supply current when off-state	$V_{EN1,2}$=0V, $V_{OUT1,2}$=0V	$V_{IN1,2}$=5.0V		0.5		uA
			$V_{IN1,2}$=3.3V		0.1		
			$V_{IN1,2}$=1.8V		0.07		
			$V_{IN1,2}$=0.8V		0.04		
RESISTANCE CHARACTERISTICS							
R_{ON}	On-Resistance per Channel	I_{OUT}=-200mA, V_{IN}=0.8V - 5.0V	25℃		18	25	mΩ
			Full			27	
R_{PD}	Output Pull-down Resistance	V_{IN}=5.0V, V_{EN}=0V, I_{OUT}=15mA			220	300	Ω
ENABLE INPUT							
V_{IH}	Enable Input Logic-High Voltage	V_{BIAS}=2.5V to 5.5V		1.2			V
V_{IL}	Enable Input Logic-Low Voltage					0.4	V
I_{EN}	EN pin Input Leakage Current	V_{EN}=5.5V				1	uA

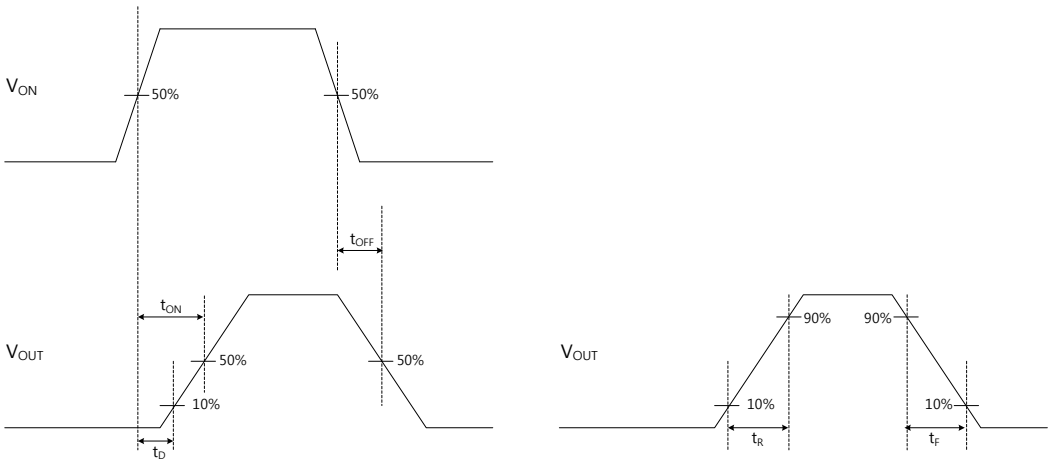
Note 1: All devices under mass production are tested at T_C=+25℃. Specifications over the operating temperature range are not guaranteed.

Switching Characteristics

T_A = 25°C (Unless otherwise noted)

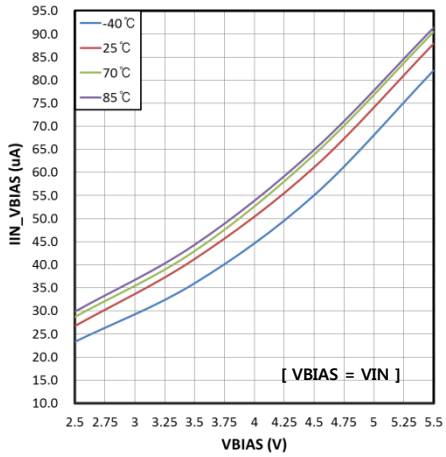
Parameter		Test Condition	Min	Typ.	Max	Unit
V_{IN}=V_{ON}=V_{BIAS}=5V, T_A=25℃						
t_{ON}	Turn-On Time	R_L=10Ω, C_L=0.1uF, C_T=1000pF		1710		us
t_{OFF}	Turn-Off Time	R_L=10Ω, C_L=0.1uF, C_T=1000pF		1.5		
t_R	VOUT rise time	R_L=10Ω, C_L=0.1uF, C_T=1000pF		2210		
t_F	VOUT fall time	R_L=10Ω, C_L=0.1uF, C_T=1000pF		2		
t_D	ON delay time	R_L=10Ω, C_L=0.1uF, C_T=1000pF		610		
V_{IN}=0.8V, V_{ON}=V_{BIAS}=5V, T_A=25℃						
t_{ON}	Turn-On Time	R_L=10Ω, C_L=0.1uF, C_T=1000pF		630		us
t_{OFF}	Turn-Off Time	R_L=10Ω, C_L=0.1uF, C_T=1000pF		1.5		
t_R	VOUT rise time	R_L=10Ω, C_L=0.1uF, C_T=1000pF		410		
t_F	VOUT fall time	R_L=10Ω, C_L=0.1uF, C_T=1000pF		2		
t_D	ON delay time	R_L=10Ω, C_L=0.1uF, C_T=1000pF		520		

Turn-On/Off Switching Waveforms

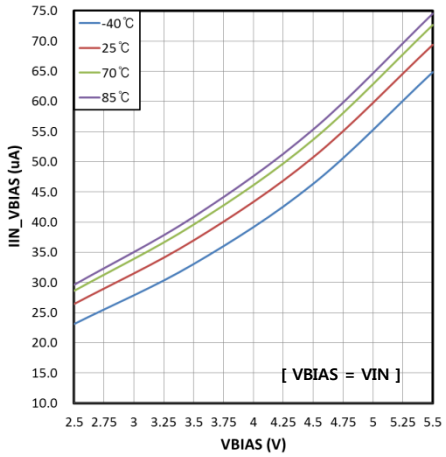


Typical Characteristics

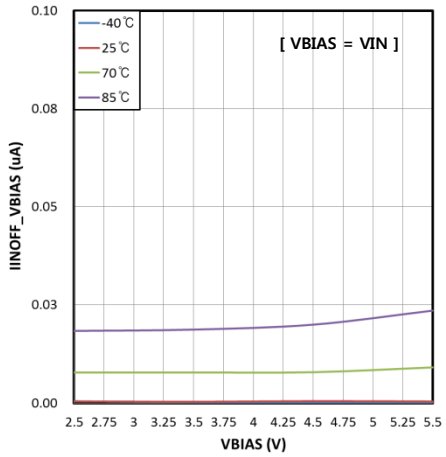
V_{BIAS} vs QUIESCENT CURRENT (SINGLE CHANNEL)



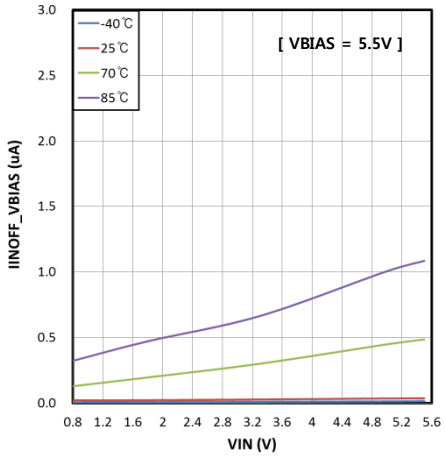
V_{BIAS} vs QUIESCENT CURRENT (BOTH CHANNELS)



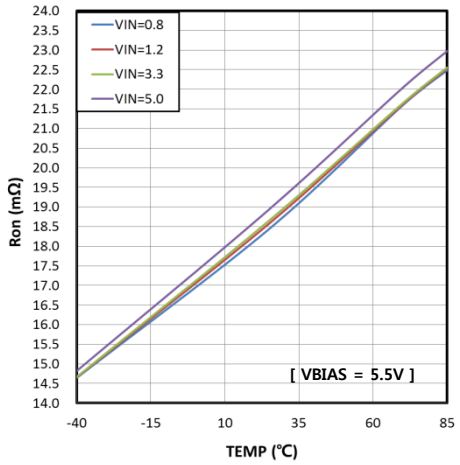
V_{BIAS} vs SHUTDOWN CURRENT (BOTH CHANNELS)



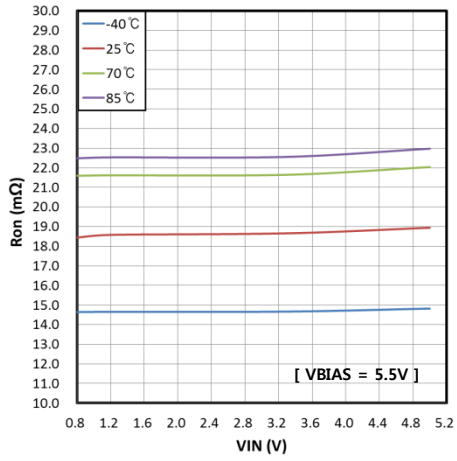
V_{IN} vs OFF-STATE VIN CURRENT (SINGLE CHANNEL)



TEMPERATURE vs R_{ON} (VBIAS = 5.5V, SINGLE CHANNEL)

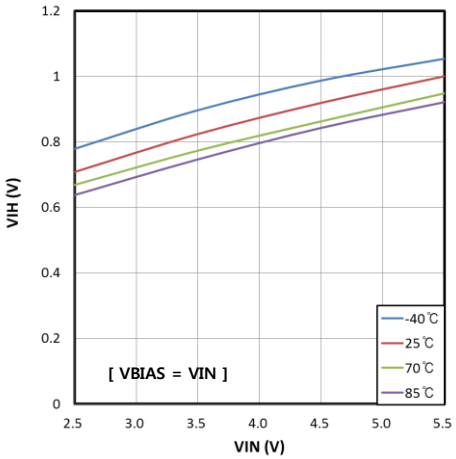


V_{IN} vs R_{ON} (VBIAS = 5.5V, SINGLE CHANNEL)

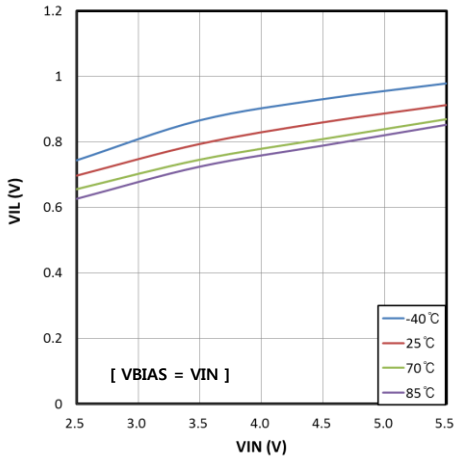


Typical Characteristics (continued...)

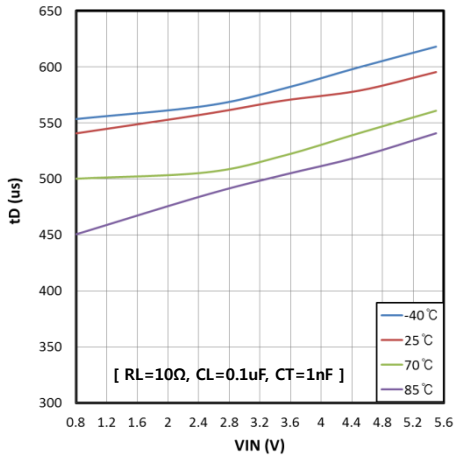
V_{IN} vs VIH



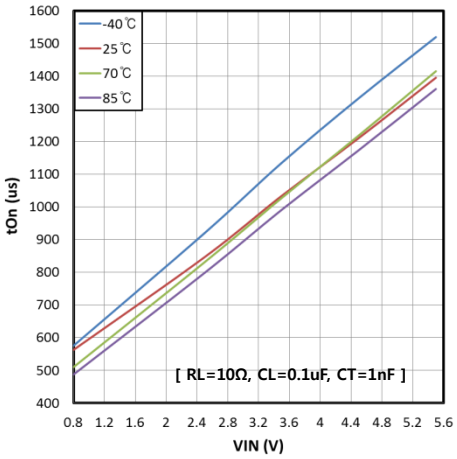
V_{IN} vs VIL



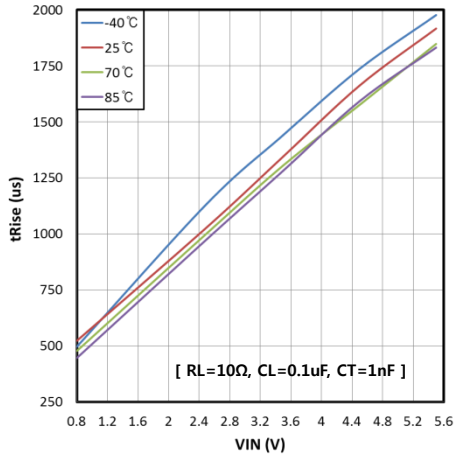
V_{IN} vs t_D
(VBIAS = 5.5V, CT = 1nF)



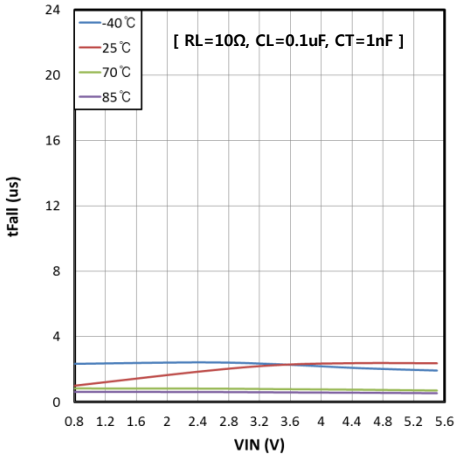
V_{IN} vs t_{ON}
(VBIAS = 5.5V, CT = 1nF)



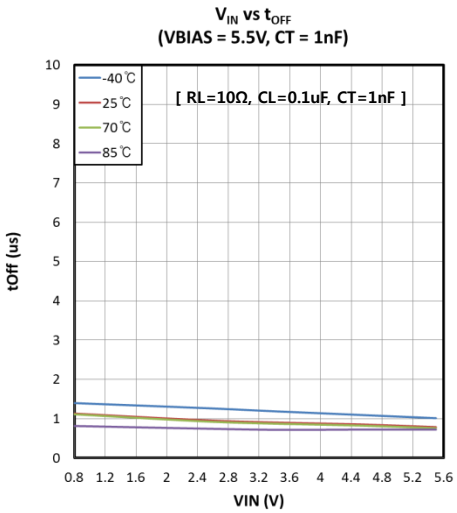
V_{IN} vs t_R
(VBIAS = 5.5V, CT = 1nF)



V_{IN} vs t_F
(VBIAS = 5.5V, CT = 1nF)



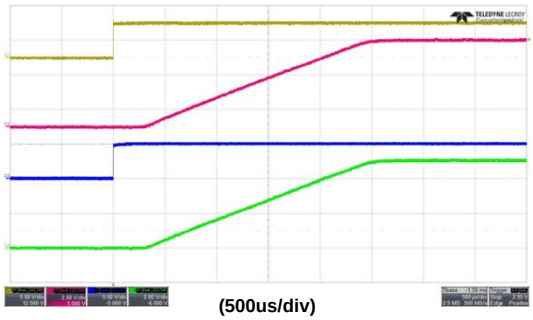
Typical Characteristics (continued...)



Typical Characteristics (continued...)

Turn-on Response

(V_{IN}=5.0V, V_{BIAS}=5.0V, C_{IN}=1uF, C_L=0.1uF, R_L=10Ω)

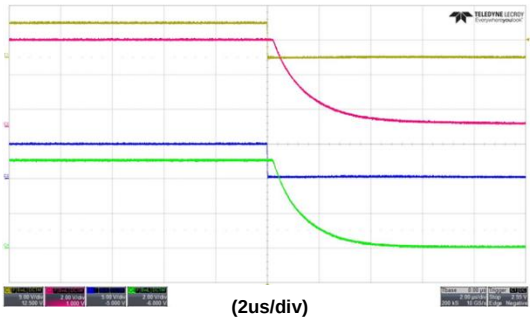


V_{EN1} (5.0V/div)
V_{OUT1} (5.0V/div)
V_{EN2} (5.0V/div)
V_{OUT2} (5.0V/div)

(500us/div)

Turn-off Response

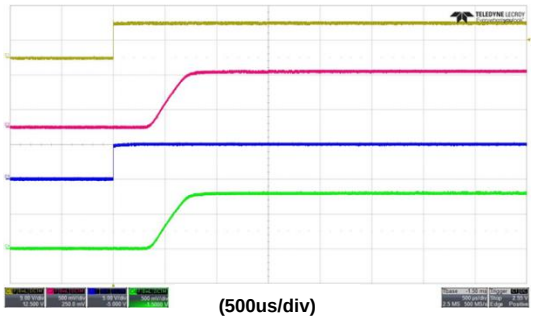
(V_{IN}=5.0V, V_{BIAS}=5.0V, C_{IN}=1uF, C_L=0.1uF, R_L=10Ω)



(2us/div)

Turn-on Response

(V_{IN}=0.8V, V_{BIAS}=5.0V, C_{IN}=1uF, C_L=0.1uF, R_L=10Ω)

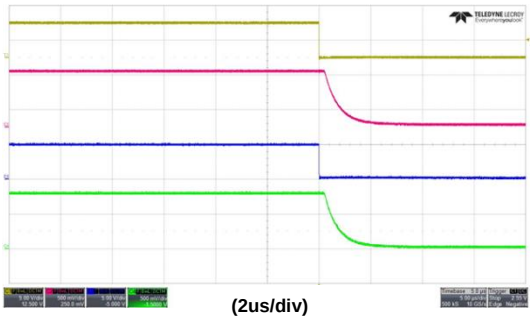


V_{EN1} (5.0V/div)
V_{OUT1} (0.5V/div)
V_{EN2} (5.0V/div)
V_{OUT2} (0.5V/div)

(500us/div)

Turn-off Response

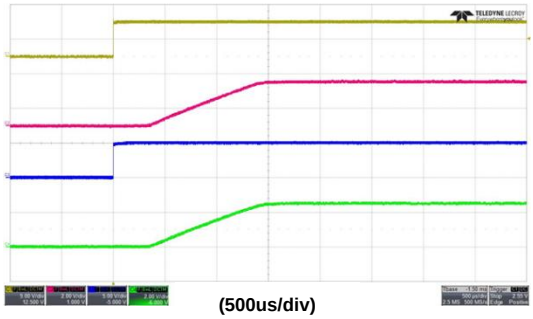
(V_{IN}=0.8V, V_{BIAS}=5.0V, C_{IN}=1uF, C_L=0.1uF, R_L=10Ω)



(2us/div)

Turn-on Response

(V_{IN}=2.5V, V_{BIAS}=2.5V, C_{IN}=1uF, C_L=0.1uF, R_L=10Ω)

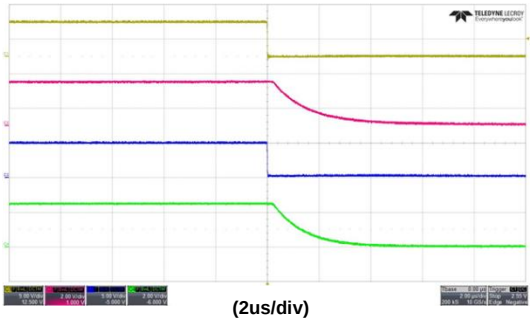


V_{EN1} (5.0V/div)
V_{OUT1} (2.0V/div)
V_{EN2} (5.0V/div)
V_{OUT2} (2.0V/div)

(500us/div)

Turn-off Response

(V_{IN}=2.5V, V_{BIAS}=2.5V, C_{IN}=0.1uF, C_L=0.1uF, R_L=10Ω)

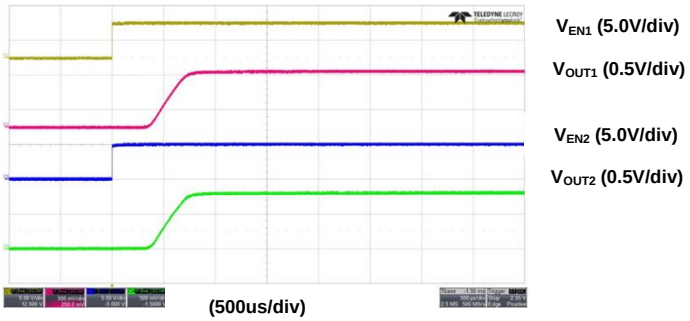


(2us/div)

Typical Characteristics (continued...)

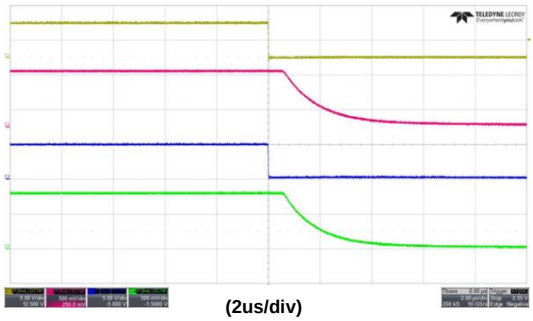
Turn-on Response

(V_{IN}=0.8V, V_{BIAS}=2.5V, C_{IN}=0.1uF, C_L=0.1uF, R_L=10Ω)



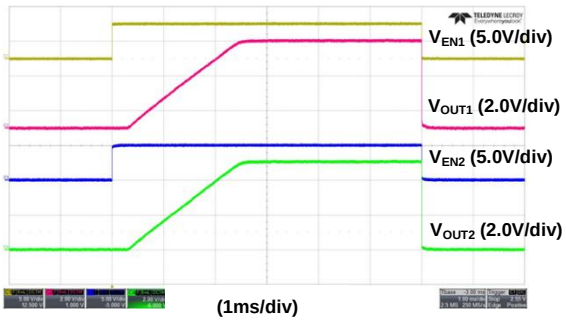
Turn-off Response

(V_{IN}=0.8V, V_{BIAS}=2.5V, C_{IN}=0.1uF, C_L=0.1uF, R_L=10Ω)



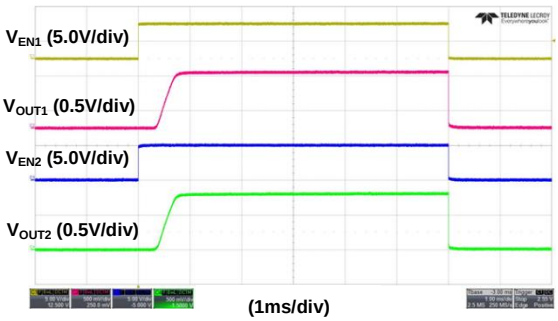
Turn-on/off Response

(V_{IN}=5.0V, V_{BIAS}=5.0V, C_{IN}=0.1uF, C_L=0.1uF, R_L=10Ω)



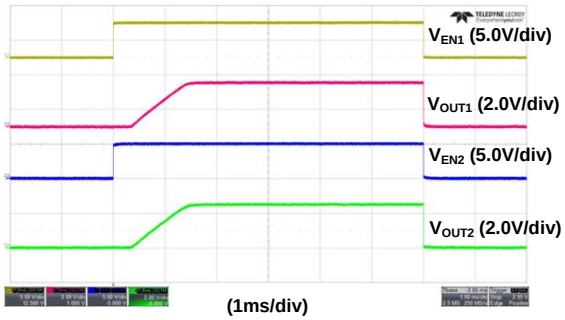
Turn-off Response

(V_{IN}=0.8V, V_{BIAS}=5.0V, C_{IN}=0.1uF, C_L=0.1uF, R_L=10Ω)



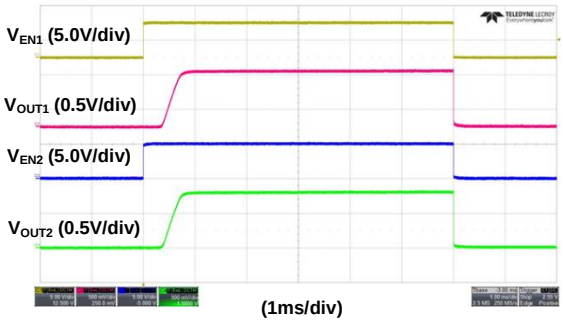
Turn-on Response

(V_{IN}=2.5V, V_{BIAS}=2.5V, C_{IN}=0.1uF, C_L=0.1uF, R_L=10Ω)



Turn-off Response

(V_{IN}=0.8V, V_{BIAS}=2.5V, C_{IN}=0.1uF, C_L=0.1uF, R_L=10Ω)



Detailed Descriptions

Overview

The MSI2206 is a dual channel load switch has low Ron N-channel MOSFET with controllable slew rate.

The MSI2206 is designed to have very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply.

The MSI2206 is controlled by active-high logic input the EN pin. This device has controllable rise time for limiting inrush current.

The input voltage range operates from 0.8V to 5.5VDC to support a wide range for using in many kinds of applications.

This device is packaged 2.0 mm x 3.0 mm, DFN-14 lead package.

Controllable Rise Time

A capacitor to GND on the CT pin sets the slew rate. For optimal performance, CT cap should be minimum 25V voltage rating. A chart for relationship between CT and slew rate when V_{BIAS} is set to 5V is below.

CTx (pF)	RISE TIME (us) 10% - 90%, CL = 0.1uF, CIN = 1uF, RL = 10Ω TYPICAL VALUES at 25℃, VBIAS = 5V, 25V CERAMIC CAP						
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	344	316	289	283	276	274	269
220	668	526	402	377	352	338	321
470	1083	801	551	498	445	419	379
1000	1917	1352	852	751	645	593	511
2200	4137	2729	1635	1348	1139	1036	876
4700	9196	6150	3304	2863	2253	2057	1657
10000	17266	11386	6329	5326	4427	3930	3116

Rise time can be calculated by multiplying the input voltage by the slew rate.

Quick Output Discharge

The MSI2206 has a Quick Output Discharge (QOD). When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 220Ω.

Low Power Consumption

VIN off-state leakage is 0.07uA at 1.8-VIN. So, the load switch allows system standby power consumption to be reduced.

Application and Implementation

EN Input

The MSI 2206's switch position is controlled by an EN active-high logic input. The switch is on when EN is logic high and off when EN is logic low.

The EN pin has a low threshold, making it capable of interfacing with low-voltage signals. The EN pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2V or higher GPIO voltage.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents or short-circuit, a capacitor needs to be placed between V_{IN} and GND.

A 1uF ceramic capacitor of C_{IN} is usually sufficient. Input capacitor is placed close to the pins.

When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

Output Capacitor

Operation of the MSI2206 is recommended C_{IN} greater than C_L. If C_L greater than C_{IN}, V_{OUT} can exceed V_{IN} when system supply is removed. This could result in current flow from V_{OUT} to V_{IN}.

A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

V_{IN} and V_{BIAS} Voltage Range

For optimal operation, make sure $V_{IN} \leq V_{BIAS}$. If setting $V_{IN} > V_{BIAS}$, R_{ON} is increased steeply.

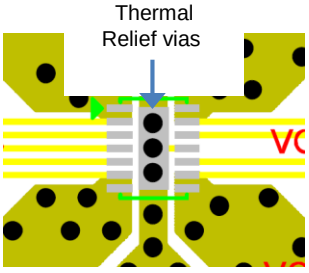
Thermal and Layout Consideration

The MSI2206 maximum power dissipation depends on the differences of the thermal resistance and temperature between junction and ambient air.
The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(MAX)}$ for a given output current and ambient temperature, use the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

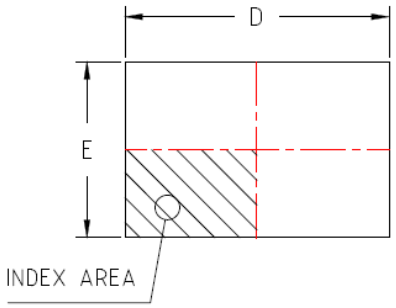
Where:
- $P_{D(MAX)}$ = maximum allowable power dissipation
- $T_{J(MAX)}$ = maximum allowable junction temperature (125°C for the MSI2206)
- T_A = ambient temperature of the device
- Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

The figure below shows an example of a layout. Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

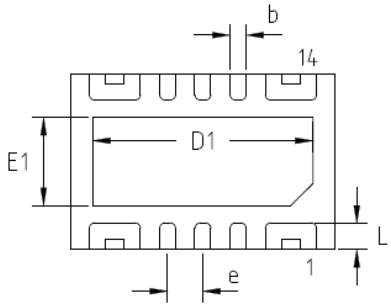


Physical Dimensions

2.0 mm X 3.0 mm DFN-14 Lead

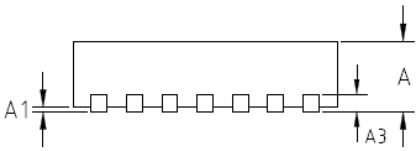


TOP VIEW

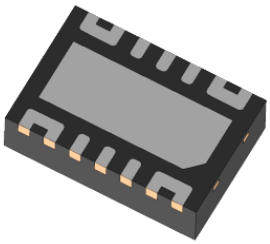


BOTTOM VIEW

Symbol	Dimension [mm]
A	0.75 ± 0.10
A1	0.00~0.05
A3	0.20 REF
D	3.00 ± 0.10
E	2.00 ± 0.10
D1	2.50 ± 0.10
E1	0.9 ± 0.10
b	0.18 ± 0.07
e	0.40 BSC
L	0.30 ± 0.10



SIDE VIEW



MagnaChip is a registered trademark of MagnaChip Semiconductor Ltd.
MagnaChip Semiconductor Ltd.
891, Daechi-Dong, Kangnam-Gu, Seoul, 135-738 Korea
Tel : 82-2-6903-3451 / Fax : 82-2-6903-3668~9
www.magnachip.com