ChipScope OPB IBA (Bus Analyzer) (v. 1.01a)

DS282 June 24, 2009 **Product Specification**

Introduction

The ChipScope™ OPB IBA core is a specialized Bus Analyzer core designed to debug embedded systems containing the IBM CoreConnect On-Chip Peripheral Bus (OPB). The ChipScope OPB IBA core in EDK is based on Tcl script that generates a HDL wrapper to the OPB IBA and calls the ChipScope Core Generator to generate the netlist based on user parameters.

Features

- A Protocol Violation Monitor
- Multiple Trigger Units for Trigger and Data capture
- Each Trigger Unit can be enabled and configured independently
- The Trigger Units for the OPB IBA are:
  - OPB Control signals
  - OPB Address Units
  - OPB Data Unit (combined)
  - OPB Read/Write Data Units
  - OPB Protocol Violation Unit
  - OPB Master Units (based on no. of masters)
  - OPB Slave Units (based on no. of slaves)
- Generic Trigger/Data Unit with selectable width

For more information about the ATC2 core, refer to the *ChipScope Pro Software and Cores User Guide*.

LogiCORE IP Facts				
Core Specifics				
Supported Device Family[1]	Spartan®-3E, Automotive Spartan-3E, Spartan-3, Automotive Spartan-3, Spartan-3A, Automotive Spartan-3A, Spartan-3A DSP, Automotive Spartan-3A DSP, Virtex-4			
Resources Used[2]	I/O	LUTs	FFs	Block RAMs
	8	122	185	0
Special Features	N/A			
Provided with Core				
Documentation	Product Specification			
Design File Formats	VHDL/EDIF			
Constraints File	N/A			
Verification	N/A			
Instantiation Template	N/A			
Reference Designs /Application Notes	None			
Additional Items	Signal Description File (.cdc)			
Design Tool Requirements				
Xilinx® Implementation Tools	ISE® 11.2			
Verification	ChipScope™ Pro 11.2			
Simulation	Not supported in simulation			
Synthesis	Netlist is pre-synthesized by XST			
Support				
Provided by Xilinx, Inc.				

1. Including the variants of these FPGA device families.
2. These estimates assume Virtex-4 device family with one 8-bit wide bank.

Functional Description

The ChipScope OPB IBA core is a specialized Bus Analyzer core designed to debug embedded systems containing the IBM CoreConnect On-Chip Peripheral Bus (OPB). The modules and interconnects are shown in Figure 1.The data path of the ATC2 core consists of:

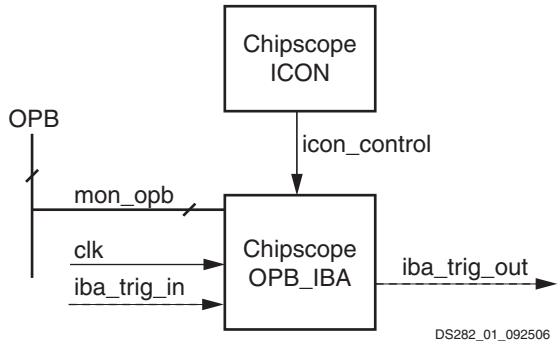

Figure 1: ChipScope OPB IBA Block Diagram

ChipScope OPB IBA I/O Signals

The I/O signals for the ChipScope OPB IBA are listed and described in Table 1.

Table 1: **ChipScope OPB IBA I/O Signals**

Signal Name	Match Unit	Interface	I/O	Description
chipscope_icon_control	N/A	N/A	I[35:0]	ICON Control signals
iba_trig_in	GENERIC	N/A	I	Generic Trigger Inputs
iba_trig_out	GENERIC	N/A	O	IBA Trigger Output
OPB_Clk	CONTROL	N/A	I	OPB Clock
OPB_Rst	CONTROL	MON_OPB	I	OPB Reset
SYS_Rst	CONTROL	N/A	I	System Reset
Debug_SYS_Rst	CONTROL	MON_OPB	I	Debug System Reset
WDT_Rst	CONTROL	MON_OPB	I	Watch Dog Reset
OPB_BE	CONTROL	MON_OPB	I	OPB Byte Enable
OPB_BusLock	CONTROL	MON_OPB	I	OPB Bus Lock
OPB_ErrAck	CONTROL	MON_OPB	I	OPB Error Acknowledge
OPB_MGrant	CONTROL	MON_OPB	I	OPB Master Grant
OPB_PendReq	CONTROL	MON_OPB	I	OPB Pending Request
OPB_Retry	CONTROL	MON_OPB	I	OPB Retry
OPB_RNW	CONTROL	MON_OPB	I	OPB Read / Not Write
OPB_Select	CONTROL	MON_OPB	I	OPB Select
OPB_SeqAddr	CONTROL	MON_OPB	I	OPB Sequential Address
OPB_TimeOut	CONTROL	MON_OPB	I	OPB Timeout

Table 1: **ChipScope OPB IBA I/O Signals *(Cont'd)***

Signal Name	Match Unit	Interface	I/O	Description
OPB_ToutSup	CONTROL	MON_OPB	I	OPB Timeout Suppress
OPB_XferAck	CONTROL	MON_OPB	I	OPB Transfer Acknowledge
OPB_ABus	ADDR	MON_OPB	I	OPB Address Bus
OPB_DBus	DATA	MON_OPB	I	OPB Data Bus
OPB_RdDBus	RDDATA	MON_OPB	I	OPB Read Data Bus
OPB_WrDBus	WRDATA	MON_OPB	I	OPB Write Data Bus
M_BE	MASTER<n>	MON_OPB	I	Master Byte Enable
M_BusLock	MASTER<n>	MON_OPB	I	Master Bus Lock
M_Request	MASTER<n>	MON_OPB	I	Master Request
M_RNW	MASTER<n>	MON_OPB	I	Master Read / Not Write
M_Select	MASTER<n>	MON_OPB	I	Master Select
M_SeqAddr	MASTER<n>	MON_OPB	I	Master Sequential Address
Sl_ErrAck	SLAVE<n>	MON_OPB	I	Master Error Acknowledge
Sl_Retry	SLAVE<n>	MON_OPB	I	Slave Retry
Sl_ToutSup	SLAVE<n>	MON_OPB	I	Slave Timeout Suppress
Sl_XferAck	SLAVE<n>	MON_OPB	I	Slave Transfer Acknowledge

ChipScope OPB IBA Parameters

Table 2 describes the features that can be parameterized to create a ChipScope OPB IBA that is uniquely tailored for a specific system and that will provide optimal performance. For a detailed description of the OPB IBA core, see the *ChipScope Pro Software and Cores User Guide* in the ChipScope installation.

The ChipScope OPB IBA peripheral supports multiple trigger units that connect to the OPB Control bus, Address bus, Data bus, individual Slave or Master buses, a generic trigger input, and a protocol violation unit. Each trigger units can be enabled and parametrized independently. In the following table, C_<XYZ>_UNIT, refers to any one of these units and the parameters associated wit it. The table also lists all the trigger units and the parameter names used to enable each unit.

Table 2: **ChipScope OPB IBA Parameters**

Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Number of Data Samples captured for every trigger match	C_NUM_DATA_SAMPLES	Integer (512, 1024, 2048, 4096, 8192, 16384)	512	integer
Enable the Trigger out signal iba_trig_out which will be asserted when IBA gets triggered	C_ENABLE_TRIGGER_OUT	Integer 1 = Enable Trigger out 0 = Disable Trigger out	0	integer
Target Family	C_FAMILY	Xilinx FPGA families	virtex2	strings
Disable RPM placement information in netlist	C_DISABLE_RPM	Integer 1 = RPM disable 0 = RPM enabled in netlist	0	integer
Disable SRL16 usage	C_DISABLE_SRL16S	Integer 1 = Disable 0 = Enable	0	Integer
Trigger on Rising or Falling edge of clock	C_RISING_CLOCK_EDGE	Integer 1 = Rising 0 = Falling	1	Integer
Enable Trigger Sequencer in the ILA	C_ENABLE_TRIGGER_ SEQUENCER	Integer 1 = Enable 0 = Disable	1	Integer
Maximum number of Sequencer levels	C_MAX_SEQUENCER_ LEVELS	Integer (1-16)	16	Integer
Enable Storage Qualification for ILA	C_ENABLE_STORAGE_ QUALIFICATION	Integer (1 = Enable 0 = Disable	1	Integer
Number of Match Units enabled for <XYZ> Unit Ex: OPB Control Signals	C_<XYZ>_UNITS Ex: C_CONTROL_UNITS	Integer (0-16) 0 = Disable Unit 1-16 = Number of Match Units	0	integer
Counter Width for Match Unit <XYZ> Ex: OPB Control signals Match Unit	C_<XYZ>_UNIT_ COUNTER_WIDTH Ex: C_CONTROL_UNIT_ COUNTER_WIDTH	Integer (0-32) 0 - Disable Match Counter 1-32 - Match Counter Width (Refer to the ChipScope User Guide)	0	integer
Match Tyoe for Match Unit <XYZ> Ex: OPB Control signals Match Unit	C_<XYZ>_UNIT_MATCH_ TYPE Ex: C_CONTROL_UNIT_ MATCH_TYPE	"basic", "basic with edges", "extended", "extended with edges", "range", "range with edges" (Refer to the ChipScope User Guide)	"basic"	string
OPB Control Unit	C_CONTROL_UNITS	Integer (0-16)	1	integer
OPB Address Unit	C_ADDR_UNITS	Integer (0-16)	1	integer

Table 2: **ChipScope OPB IBA Parameters *(Cont'd)***

Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
OPB Data Unit (combined)	C_DATA_UNITS	Integer (0-16)	1	integer
OPB Protocol Violation Unit	C_PV_UNITS	Integer (0-16)	0	integer
Generic Trigger Unit	C_GENERIC_ TRIGGER_UNITS	Integer (0-16)	0	integer
Generic Trigger Input Width	C_GENERIC_TRIGGER_ IN_WIDTH	Integer	0	integer
OPB Write Data Unit	C_WRDATA_UNITS	Integer (0-16)	0	integer
OPB Read Data Unit	C_RDDATA_UNITS	Integer (0-16)	0	integer
OPB Master (0-16) Unit	C_MASTER<n>_UNITS	Integer (0-16)	0	integer
OPB Slave (0-16) Unit	C_SLAVE<n>_UNITS	Integer (0-16)	0	integer

Allowable Parameter Combinations

The parameter C_GENERIC_TRIGGER_IN_WIDTH is valid only when the generic trigger input signal (not OPB-bus related) is enabled on the ChipScope OPB IBA by specifying the C_GENERIC_TRGGER_UNITS to be 1 or higher.

Parameters C_<XYZ>_UNIT_COUNTER_WIDTH and C_<XYZ>_UNIT_MATCH_TYPE are valid only when the corresponding trigger unit is enabled by setting C_<XYZ>_UNITS to be 1 or higher.

The Master and Slave trigger units that can be enabled using C_MASTER<n>_UNITS and C_SLAVE<n>_UNITS is determined by the number of master or slave OPB peripherals in the user's processor design. <n> refers to the position of a peripheral on the OPB bus (this is usually the same as the order in the user's MHS design).

For more information, refer the *ChipScope Pro Software and Cores User Guide*, in the ChipScope installation.

Parameter - Port Dependencies

Table 3: **ChipScope OPB IBA Parameter - Port dependencies**

Port Name	Parameter dependency	Description
iba_trig_in	C_GENERIC_TRIGGER_UNITS C_GENERIC_TRIGGER_IN_WIDTH	The generic trigger input port and its width is determined by these two
iba_trig_out	C_ENABLE_TRIGGER_OUT	The trig_out port is enabled when this parameter is set to 1

Design Implementation

Design Tools

The ChipScope OPB IBA design consists mainly of a Tcl script. When the EDK platgen tool is run, this Tcl script gets called and the script internally calls the ChipScope Pro Core Generator tool in command line mode and provides it an arguments file (.arg) to generate the ChipScope OPB IBA netlist. The Tcl script also generates a HDL wrapper to match the IBA ports based on the core parameters.

XST is the synthesis tool used for synthesizing the wrapper HDL generated for the ChipScope OPB IBA. The EDIF netlist outputs from XST and ChipScope Core Generator are then input to the Xilinx Foundation tool suite for actual device implementation.

Target Technology

The intended target technology is all Xilinx FPGAs.

Device Utilization and Performance Benchmarks

The device utilization varies widely based on the parameter combinations set by the user.

Restrictions

Maximum number of signals that can be monitored with a single IBA is 256 signals.

References

[1] More information on the ChipScope Pro software and cores is available in the *Software and Cores User Guide*, located at
http://www.xilinx.com/support/documentation/sw_manuals/chipscope_pro_sw_cores_10_1_ug029.pdf.

[2] Information about hardware debugging using ChipScope Pro in EDK is available in the Platform Studio 11.1 online help, located at
http://www.xilinx.com/itp/xilinx11/help/platform_studio/platform_studio_start.htm.

[3] Information about hardware debugging using ChipScope Pro in System Generator for DSP is available in the *Xilinx System Generator for DSP User Guide*, located at
http://www.xilinx.com/support/sw_manuals/sysgen_ug.pdf.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The OPB IBA core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator system 11.2 or higher. The CORE Generator system is shipped with Xilinx ISE Foundation Series Development software.

Revision History

Date	Version	Revision
01/16/2004	1.0	Release 6.1i (Initial Xilinx release).
08/30/2004	1.1	Release 6.3i.
04/02/2005	2.0	Release 7.1i, Service Pack 1 changes.
10/31/2005	3.0	Release 8.1i.
09/25/2006	4.0	Release 9.1i.
04/21/2008	5.0	Release 10.1.
04/07/2009	6.0	Release 11.1.
06/24/2009	6.1	Release 11.2.

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