

Description

The 9DML04 devices are 3.3V members of IDT's Full-Featured PCIe family. The 9DML04 supports PCIe Gen1-4 Common Clocked (CC), Separate Reference no Spread (SRnS), and Separate Reference Independent Spread (SRIS) architectures. The part provides a choice of asynchronous and glitch-free switching modes, and offers a choice of integrated output terminations providing direct connection to 85Ω or 100Ω transmission lines. The 9DML04P1 can be factory programmed with a user-defined power up default SMBus configuration.

Recommended Application

Servers, ATCA, ATE, Master/Slave applications

Output Features

- 4 – 1~200 MHz Low-Power HCSL (LP-HCSL) DIF pairs
 - 9DML0441 default Z_{OUT} = 100Ω
 - 9DML0451 default Z_{OUT} = 85Ω
 - 9DML04P1 factory programmable defaults

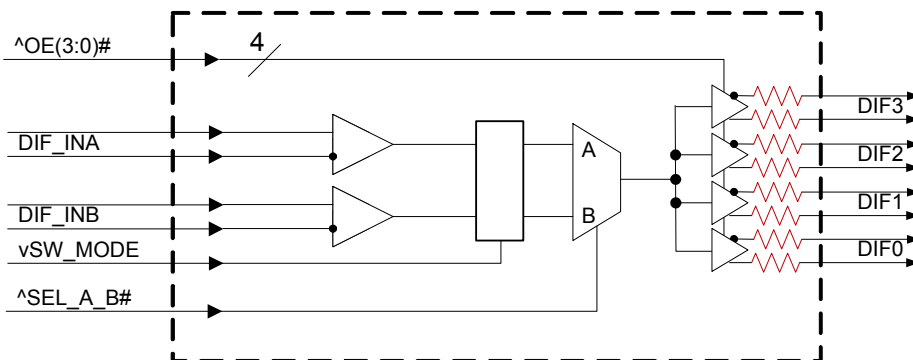
Key Specifications

- PCIe Gen1-2-3-4 CC compliant
- PCIe Gen2-3 SRIS compliant
- DIF additive cycle-to-cycle jitter <1ps
- DIF output-to-output skew <50ps
- Additive phase jitter is <0.1ps rms for PCIe
- Additive phase jitter 160fs rms typ. @156.25M (1.5M to 10M)

Features/Benefits

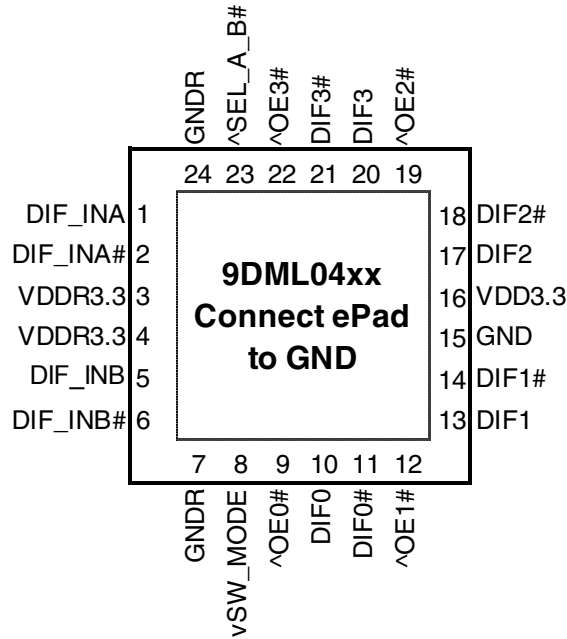
- Direct connection to 100Ω (xx41) or 85Ω (xx51) transmission lines; saves 16 resistors compared to standard PCIe devices
- 76mW typical power consumption; eliminates thermal concerns
- Spread Spectrum (SS) compatible; allows SS for EMI reduction
- Customer defined power up default can be factory programmed into P1 device; allows exact optimization to customer requirements:
 - control input polarity
 - control input pull up/downs
 - slew rate for each output
 - differential output amplitude
 - output impedance for each output
- OE# pins; support DIF power management
- HCSL-compatible differential inputs; can be driven by common clock source
- Selectable asynchronous or glitch-free switching; allows the mux to be selected at power up even if both inputs are not running, then transition to glitch-free switching mode
- Space saving 24-pin 4x4mm VFQFPN; minimal board space

Block Diagram



Note: Resistors default to internal on 41/51 devices. P1 devices have programmable default impedances on an output-by-output basis.

Pin Configuration



24 VQFPN, 4x4 mm, 0.5mm pitch

^ prefix indicates internal 120KOhm pull up resistor
 v prefix indicates internal 120KOhm pull down resistor

Power Management Table

| OEx# Pin | DIF_IN | DIFx | |
|----------|---------|----------|-----------|
| | | True O/P | Comp. O/P |
| 0 | Running | Running | Running |
| 1 | Running | Low | Low |

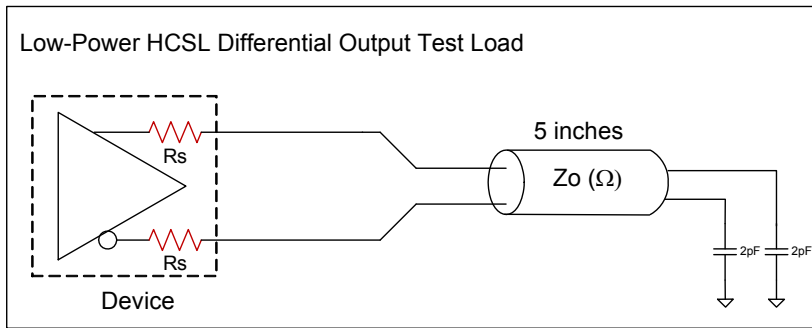
Power Connections

| Pin Number | | Description |
|------------|-----|-------------------------|
| VDD | GND | |
| 3 | 24 | Input A receiver analog |
| 4 | 7 | Input B receiver analog |
| 16 | 15 | DIF outputs |

Pin Descriptions

| Pin# | Pin Name | Type | Pin Description |
|------|-----------|------|--|
| 1 | DIF_INA | IN | HCSL Differential True input |
| 2 | DIF_INA# | IN | HCSL Differential Complement Input |
| 3 | VDDR3.3 | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. |
| 4 | VDDR3.3 | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. |
| 5 | DIF_INB | IN | HCSL Differential True input |
| 6 | DIF_INB# | IN | HCSL Differential Complement Input |
| 7 | GNDR | GND | Analog Ground pin for the differential input (receiver) |
| 8 | vSW_MODE | IN | Switch Mode. This pin selects either asynchronous or glitch-free switching of the mux. Use asynchronous mode if 0 or 1 of the input clocks is running. Use glitch-free mode if both input clocks are running. This pin has an internal pull down resistor of ~120kohms. 0 = asynchronous mode 1 = glitch-free mode |
| 9 | ^OE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 10 | DIF0 | OUT | Differential true clock output |
| 11 | DIF0# | OUT | Differential Complementary clock output |
| 12 | ^OE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 13 | DIF1 | OUT | Differential true clock output |
| 14 | DIF1# | OUT | Differential Complementary clock output |
| 15 | GND | GND | Ground pin. |
| 16 | VDD3.3 | PWR | Power supply, nominal 3.3V |
| 17 | DIF2 | OUT | Differential true clock output |
| 18 | DIF2# | OUT | Differential Complementary clock output |
| 19 | ^OE2# | IN | Active low input for enabling DIF pair 2. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 20 | DIF3 | OUT | Differential true clock output |
| 21 | DIF3# | OUT | Differential Complementary clock output |
| 22 | ^OE3# | IN | Active low input for enabling DIF pair 3. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 23 | ^SEL_A_B# | IN | Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected. |
| 24 | GNDR | GND | Analog Ground pin for the differential input (receiver) |
| 25 | EPAD | GND | Connect to Ground. |

Test Loads



Terminations

| Device | $Z_o (\Omega)$ | $R_s (\Omega)$ |
|----------|----------------|----------------|
| 9DML0441 | 100 | None needed |
| 9DML0451 | 100 | 7.5 |
| 9DML04P1 | 100 | Prog. |
| 9DML0441 | 85 | N/A |
| 9DML0451 | 85 | None needed |
| 9DML04P1 | 85 | Prog. |

Alternate Terminations

The 9DML family can easily drive LVPECL, LVDS, and CML logic. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs”](#) for details.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DML04. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|---------------------------|------|-----|----------------------|-------|-------|
| Supply Voltage | VDDx | | | | 4.6 | V | 1,2 |
| Input Voltage | V _{IN} | | -0.5 | | V _{DD} +0.5 | V | 1,3 |
| Input High Voltage, SMBus | V _{IHSMB} | SMBus clock and data pins | | | 3.9 | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2500 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

³Not to exceed 4.6V.

Electrical Characteristics–Clock Input Parameters

T_A = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------------|--------------------|---|-----|-----|-----|-------|-------|
| Input Common Mode Voltage - DIF_IN | V _{COM} | Common Mode Input Voltage | 150 | | 900 | mV | 1 |
| Input Swing - DIF_IN | V _{SWING} | Differential value | 300 | | | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | |
| Input Duty Cycle | d _{tin} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFIn} | Differential Measurement | 0 | | 125 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Current Consumption

T_A = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-------------------|---------------------------------|-----|-----|-----|-------|-------|
| Operating Supply Current | I _{DD} | VDD, All outputs active @100MHz | | 23 | 30 | mA | |
| Powerdown Current | I _{DDPD} | VDD, all outputs disabled | | 1.6 | 2.5 | mA | 1 |

¹Input clock stopped.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

$T_A = T_{AMB}$, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--|-----------------|--|---------------|------|----------------|--------|-------|
| Supply Voltage | VDDx | Supply voltage for core and analog | 3.135 | 3.3 | 3.465 | V | |
| Ambient Operating Temperature | T_{AMB} | Industrial range | -40 | 25 | 85 | °C | |
| Input High Voltage | V_{IH} | Single-ended inputs, except SMBus | $0.75 V_{DD}$ | | $V_{DD} + 0.3$ | V | |
| Input Low Voltage | V_{IL} | Single-ended inputs, except SMBus | -0.3 | | $0.25 V_{DD}$ | V | |
| Input Current | I_{IN} | Single-ended inputs, $V_{IN} = GND$, $V_{IN} = V_{DD}$ | -5 | | 5 | uA | |
| | I_{INP} | Single-ended inputs $V_{IN} = 0 V$; Inputs with internal pull-up resistors $V_{IN} = V_{DD}$; Inputs with internal pull-down resistors | -50 | | 50 | uA | |
| Input Frequency | F_{ibvp} | | 1 | | 200 | MHz | 2 |
| Pin Inductance | L_{pin} | | | | 7 | nH | 1 |
| Capacitance | C_{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C_{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1 |
| | C_{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T_{STAB} | From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.7 | 1 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable Frequency for PCIe Applications (Triangular Modulation) | 30 | 31.5 | 33 | kHz | |
| Input SS Modulation Frequency non-PCIe | f_{MODIN} | Allowable Frequency for non-PCIe Applications (Triangular Modulation) | 0 | | 66 | kHz | |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | 2 | 3 | clocks | 1,3 |
| Tdrive_PD# | t_{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | t_F | Fall time of single-ended control inputs | | | 5 | ns | 2 |
| Trise | t_R | Rise time of single-ended control inputs | | | 5 | ns | 2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------------------|---|------|-----|------|-------|-------|
| Slew rate | dV/dt | Scope averaging on, default settings | 1.5 | 2.6 | 4 | V/ns | 1,2,3 |
| Slew rate matching | $\Delta dV/dt$ | Slew rate matching | | 8.6 | 20 | % | 1,2,4 |
| Voltage High | V _{HIGH} | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 780 | 850 | mV | 7 |
| Voltage Low | V _{LOW} | | -150 | -32 | 150 | | 7 |
| Max Voltage | V _{max} | Measurement on single ended signal using absolute value. (Scope averaging off) | | 835 | 1150 | mV | 7 |
| Min Voltage | V _{min} | | -300 | -90 | | | 7 |
| Crossing Voltage (abs) | V _{cross_abs} | Scope averaging off | 250 | 406 | 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ -V _{cross} | Scope averaging off | | 20 | 140 | mV | 1,6 |

¹Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V. These are defaults for the 41/51 devices, alternate settings are available in the P1 device.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min/max} (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting Δ -V_{cross} to be smaller than V_{cross} absolute.

⁷ These are defaults for the 41/51 devices. They are factory adjustable in the P1 device.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|----------------------|----------------------------------|------|------|------|-------|-------|
| Duty Cycle Distortion | t _{DCD} | Measured differentially, @100MHz | -0.5 | 0.3 | 1.2 | % | 1,3 |
| Skew, Input to Output | t _{pd} | V _T = 50% | 2600 | 3428 | 4500 | ps | 1 |
| Skew, Output to Output | t _{sk3} | V _T = 50% | | 23 | 50 | ps | 1 |
| Jitter, Cycle to cycle | t _{cyc-cyc} | Additive Jitter in Bypass Mode | | 0.1 | 1 | ps | 1,2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Duty cycle distortion is the difference in duty cycle between the output and the input clock.

Electrical Characteristics—Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|-----------------------|--------------------|---|-----|-----|------|----------------|----------|---------|
| Additive Phase Jitter | $t_{jphPCIeG1-CC}$ | PCIe Gen 1 | | 0.0 | 0.01 | n/a | ps (p-p) | 1,2,3,5 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz) | | 0.0 | 0.01 | | ps (rms) | 1,2,4,5 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz) | | 0.0 | 0.01 | | ps (rms) | 1,2,4,5 |
| | $t_{jphPCIeG3-CC}$ | PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz) | | 0.0 | 0.01 | | ps (rms) | 1,2,4,5 |
| | $t_{jphPCIeG4-CC}$ | PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz) | | 0.0 | 0.01 | | ps (rms) | 1,2,4,5 |

¹ Applies to all outputs.

² Based on PCIe Base Specification Rev4.0 version 0.7draft. See <http://www.pcisig.com> for latest specifications.

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ For RMS values additive jitter is calculated by solving the following equation for b [$a^2+b^2=c^2$] where a is rms input jitter and c is rms total

⁵ Driven by 9FGL0841 or equivalent

Electrical Characteristics—Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures⁵

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|-----------------------|----------------------|---|-----|-----|------|----------------|----------|-------|
| Additive Phase Jitter | $t_{jphPCIeG2-SRIS}$ | PCIe Gen 2 (PLL BW of 16MHz, CDR = 5MHz) | | 0.0 | 0.01 | n/a | ps (rms) | 1,2,4 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz) | | 0.0 | 0.01 | | ps (rms) | 1,2,4 |

¹ Applies to all outputs.

² Based on PCIe Base Specification Rev3.1a. These filters are different than Common Clock filters. See <http://www.pcisig.com> for latest

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ For RMS values, additive jitter is calculated by solving the following equation for b [$a^2+b^2=c^2$] where a is rms input jitter and c is rms total

⁵ As of PCIe Base Specification Rev4.0 draft 0.7, SRIS is not currently defined for Gen1 or Gen4.

Electrical Characteristics— Unfiltered Phase Jitter Parameters

$T_A = T_{AMB}$, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

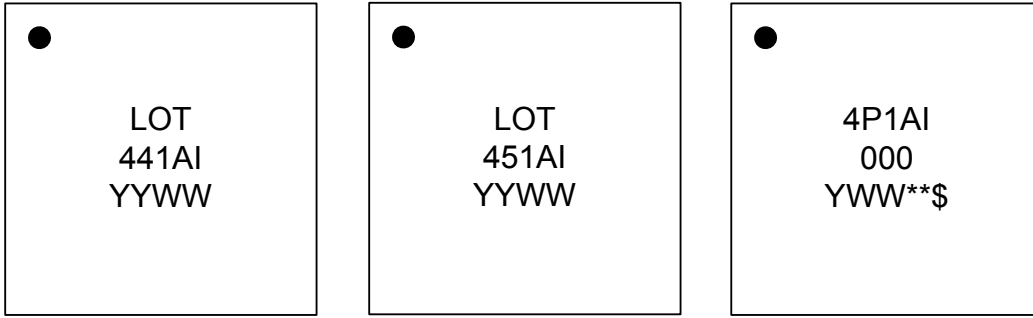
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|------------------------------------|---------------------|--|-----|-----|-----|----------------|----------|-------|
| Additive Phase Jitter, Fanout Mode | $t_{jph156M}$ | 156.25MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 159 | | N/A | fs (rms) | 1,2,3 |
| | $t_{jph156M12k-20}$ | 156.25MHz, 12kHz to 20MHz, -20dB/decade rollover <12kHz, -40db/decade rolloff > 20MHz | | 363 | | N/A | fs (rms) | 1,2,3 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Driven by Rohde&Schartz SMA100

³ For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)² - (input jitter)²]

Marking Diagrams



Notes:

1. "LOT" is the lot sequence number.
2. "YYWW" or "YWW" is the digits of the year and week that the part was assembled.
3. "I" denotes industrial temperature range device.
4. "P" denotes factory programmable defaults.
5. "***" denotes the lot sequence.
6. "\$" denotes the mark code.

Thermal Characteristics

| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP VALUE | UNITS | NOTES |
|--------------------|----------------|---------------------------------|-------|-----------|-------|-------|
| Thermal Resistance | θ_{JC} | Junction to Case | NLG24 | 42 | °C/W | 1 |
| | θ_{Jb} | Junction to Base | | 2.4 | °C/W | 1 |
| | θ_{JA0} | Junction to Air, still air | | 39 | °C/W | 1 |
| | θ_{JA1} | Junction to Air, 1 m/s air flow | | 33 | °C/W | 1 |
| | θ_{JA3} | Junction to Air, 3 m/s air flow | | 28 | °C/W | 1 |
| | θ_{JA5} | Junction to Air, 5 m/s air flow | | 27 | °C/W | 1 |

¹ePad soldered to board

Package Outline and Package Dimensions (NLG24). Use EPAD Option P1

| REVISIONS | | | |
|-----------|-------------------------|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/15/08 | RAC |
| 01 | ADD LAND PATTERN | 11/19/10 | JG |
| 03 | ADD EPAD OPTION | 05/20/15 | CM |
| 04 | ADD NOTE 13 ON PIN 1 ID | 07/09/15 | J-HUA |
| 05 | CORRECT TITLE BLOCK | 9/15/15 | J-HUA |

NOTES :

- DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M - 1994.
- ALL DIMENSIONS ARE IN MILLIMETERS, 9° IS IN DEGREES.
- TERMINAL BUSHING SHALL BE USED FOR ALL TERMINALS.
- TERMINAL DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS METALLIZATION ON THE OTHER END OF THE TERMINAL, THE DIMENSIONAL BASIS ON THE METALLIZED END SHALL BE USED AND NO REFERENCE TO THE NUMBER OF TERMINALS ON EACH D AND E SIZE RESPECTIVELY.
- MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
- PIN #1 ID ON TOP WILL BE LASER MARKED.
- BILATERAL COPPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- THIS DRAWING CONFORMS TO JEDEC REGISTERED OUTLINE MO-220
- DEPENDENT ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULLBACK (C) MAY BE PRESENT FOR 0.50mm NOMINAL LENGTH ONLY.
- TERMINAL NOTCH SHALL BE 0.125mm NOMINAL LENGTH ONLY.
- PIN 1 INDICATION CAN BE A CHAMFER, NOTCH, OR MOUSE BITE.

| EPAD OPTION: | | | | | |
|--------------|------|------|------|------|------|
| SYMBOL | MIN | NOM | MAX | MIN | MAX |
| P1 | 2.30 | 2.45 | 2.60 | 2.70 | 2.80 |
| P2 | 2.30 | 2.45 | 2.60 | 2.70 | 2.80 |
| P3 | 2.30 | 2.45 | 2.60 | 2.70 | 2.80 |

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR ± XXXX

APPROVALS DATE 10/15/08

DRAWN BY: CM

CHECKED

IDT. 6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
WWW.IDT.COM FAX: (408) 284-8591

TITLE: NLG24 PACKAGE OUTLINE
4.0 x 4.0 mm BODY
0.5 mm PITCH VQFPFN

SIZE: DRAWING No. C
DRAWING No. PSC-4192

REV: 05

DO NOT SCALE DRAWING

SHEET 1 OF 2

NOTE 13: PIN 1 IDENTIFIER

DIMENSIONS

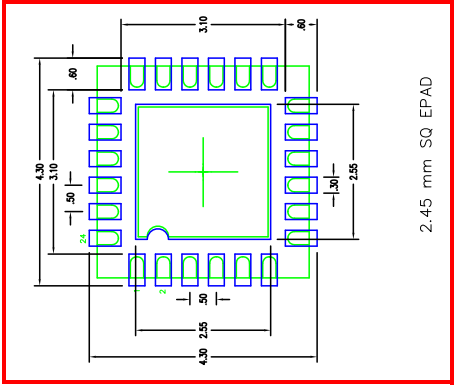
| MIN. | NOM. | MAX. |
|-----------|---------|------|
| 0.50 BSC. | 0.50 | 0.50 |
| 24 | 24 | 24 |
| 6 | 6 | 6 |
| L | 0.30 | 0.40 |
| b | 0.18 | 0.25 |
| L1 | 0.15 mm | MAX |

DIMENSIONS

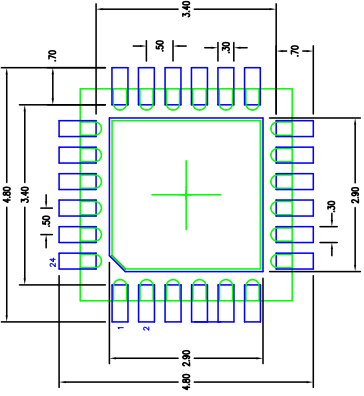
| MIN. | NOM. | MAX. |
|------|-----------|------|
| 0.00 | 0.90 | 1.0 |
| 0.00 | 0.02 | 0.05 |
| 0 | 0.20 REF. | 12 |
| K | 0.20 MIN. | |
| D | 4.0 BSC. | |
| E | 4.0 BSC. | |
| L1 | 0.15 mm | MAX |

Package Outline and Package Dimensions (NLG24), cont. Use 2.45mm SQ EPAD

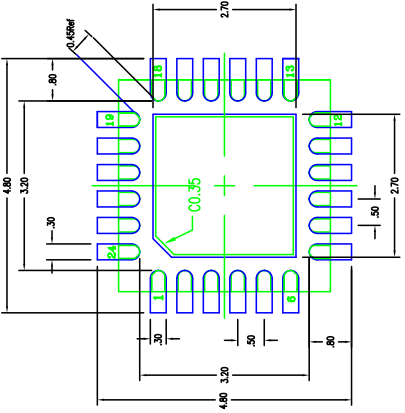
| REVISIONS | | | |
|-----------|-------------------------|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/15/08 | RAC |
| 01 | ADD LAND PATTERN | 11/19/10 | JG |
| 02 | ADD EPAD OPTION | 06/20/13 | KS |
| 03 | ADD EPAD OPTION | 05/20/15 | CM |
| 04 | ADD NOTE 13 ON PIN 1 ID | 07/09/15 | J.HUA |
| 05 | CORRECT TITLE BLOCK | 9/15/15 | J.HUA |



2.45 mm SQ EPAD



2.80 mm SQ EPAD



2.60 mm SQ EPAD

RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | |
|------------------------------|--------------------------|
| TOLERANCES UNLESS SPECIFIED: | INTEGRATION |
| SIZE FINISH | NSMD |
| APPROVALS | DATE |
| DESIGNED BY | 10/15/08 |
| CHECKED BY | 05/20/15 |
| DATE | 07/09/15 |
| TITLE | NL/NLG24 PACKAGE OUTLINE |
| SIZE | 4.0 x 4.0 mm BODY |
| FINISH | 0.3 mm PLTCH VDFPN |
| DESIGNER | PSC-4192 |
| DATE | 05 |
| BY | 05 |

DO NOT SCALE DRAWING SHEET 2 OF 2

Ordering Information

| Part / Order Number | Notes | ShippingPackaging | Package | Temperature |
|---------------------|---|-------------------|---------------|---------------|
| 9DML0441AKILF | 100Ω | Trays | 24-pin VFQFPN | -40 to +85° C |
| 9DML0441AKILFT | | Tape and Reel | 24-pin VFQFPN | -40 to +85° C |
| 9DML0451AKILF | 85Ω | Trays | 24-pin VFQFPN | -40 to +85° C |
| 9DML0451AKILFT | | Tape and Reel | 24-pin VFQFPN | -40 to +85° C |
| 9DML04P1AxxxKILF | Factory configurable. Contact IDT for additional information. | Trays | 24-pin VFQFPN | -40 to +85° C |
| 9DML04P1AxxxKILFT | | Tape and Reel | 24-pin VFQFPN | -40 to +85° C |

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

“xxx” is a unique factory assigned number to identify a particular default configuration.

Revision History

| Rev. | Initiator | Issue Date | Description | Page # |
|------|-----------|------------|--|---------|
| A | RDW | 6/6/2016 | <ol style="list-style-type: none"> 1. Updated leakage current spec for inputs with pull/up/down to +/-50uA. 2. Updated electrical tables with char data 3. Update Front page text 4. Updated ordering information 5. Move to Final. | Various |



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