

Power Management IC for Automotive Microcontroller

Buck-Boost Switching Regulator + LDO + Reset + Watch Dog Timer

BD39002EFV-C

General Description

BD39002EFV-C is a power management IC with buck-boost switching regulator controller (DC / DC1), LDO, reset and WDT.

The BD39002EFV-C includes protection circuits, such as Under voltage, Over voltage, Over current and TSD.

Features

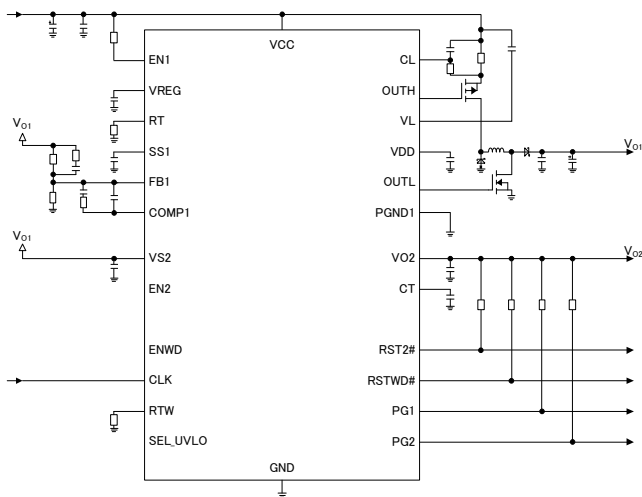
- Automatically controlled buck-boost switching regulator with 40 V rated V_{CC}, DC / DC and LDO input
- 5 V fixed output secondary LDO
- Configurable Sequence control
- Over Current protection
- DC / DC1: Adjustable voltage with external resistors
- LDO: Integrated
- Over voltage / Under voltage detection
- Reset for LDO and WDT
- Window Watchdog Timer
- HTSSOP-B30 package

Applications

- Microcontroller for Automotive

Typical Application Circuit

Simplified Circuit1



Buck-Boost Switching Regulator + Secondary LDO

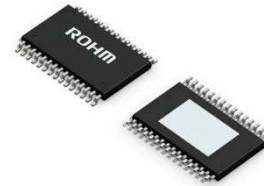
Key Specifications

- Input voltage range 4.0 V to 30 V
(Startup voltage needs to be above 4.5V.)
- Output voltage
Buck-Boost DC / DC1 FB Voltage 0.8 V
Secondary LDO 5.0 V
- Reference voltage accuracy
Buck-Boost DC / DC1 FB Voltage ±2 %
Secondary LDO ±2 %
- Oscillation frequency 200 to 550 kHz
- Max output current
Secondary LDO 600 mA
- Stand-by Current 0 μA (Typ)
- Operating temperature range -40 °C to 125 °C
- AEC-Q100 Qualified

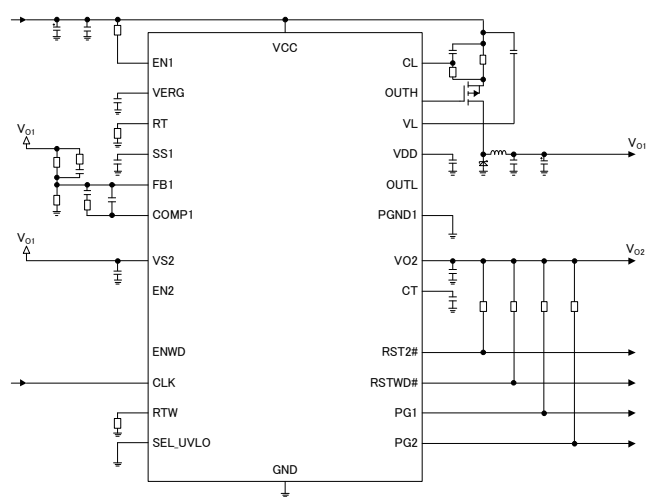
Package

HTSSOP-B30

W (Typ) × D (Typ) × H (Max)
10.00 mm × 7.60 mm × 1.00 mm

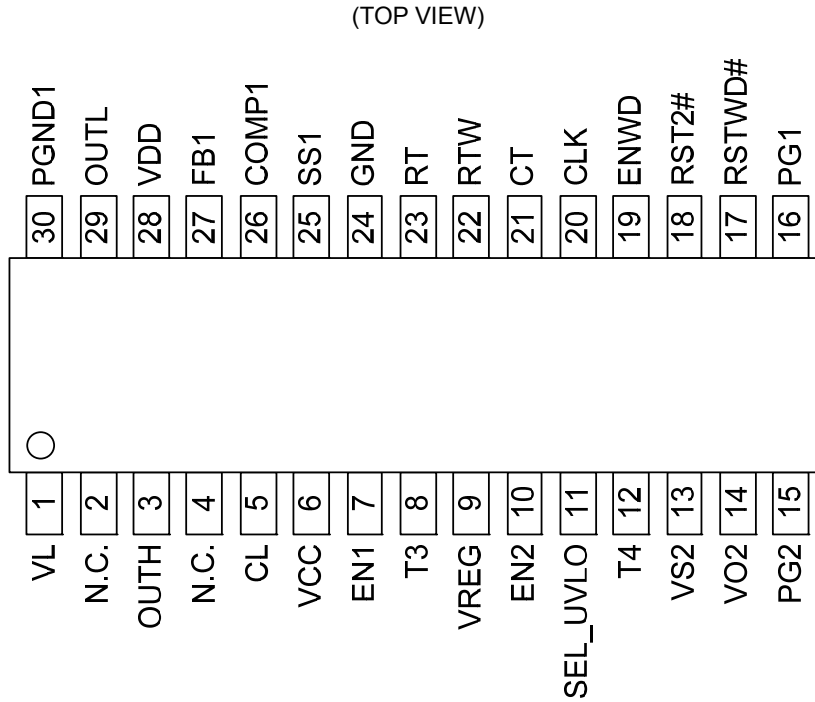


Simplified Cir



Buck Switching Regulator + Secondary LDO

Pin Configuration

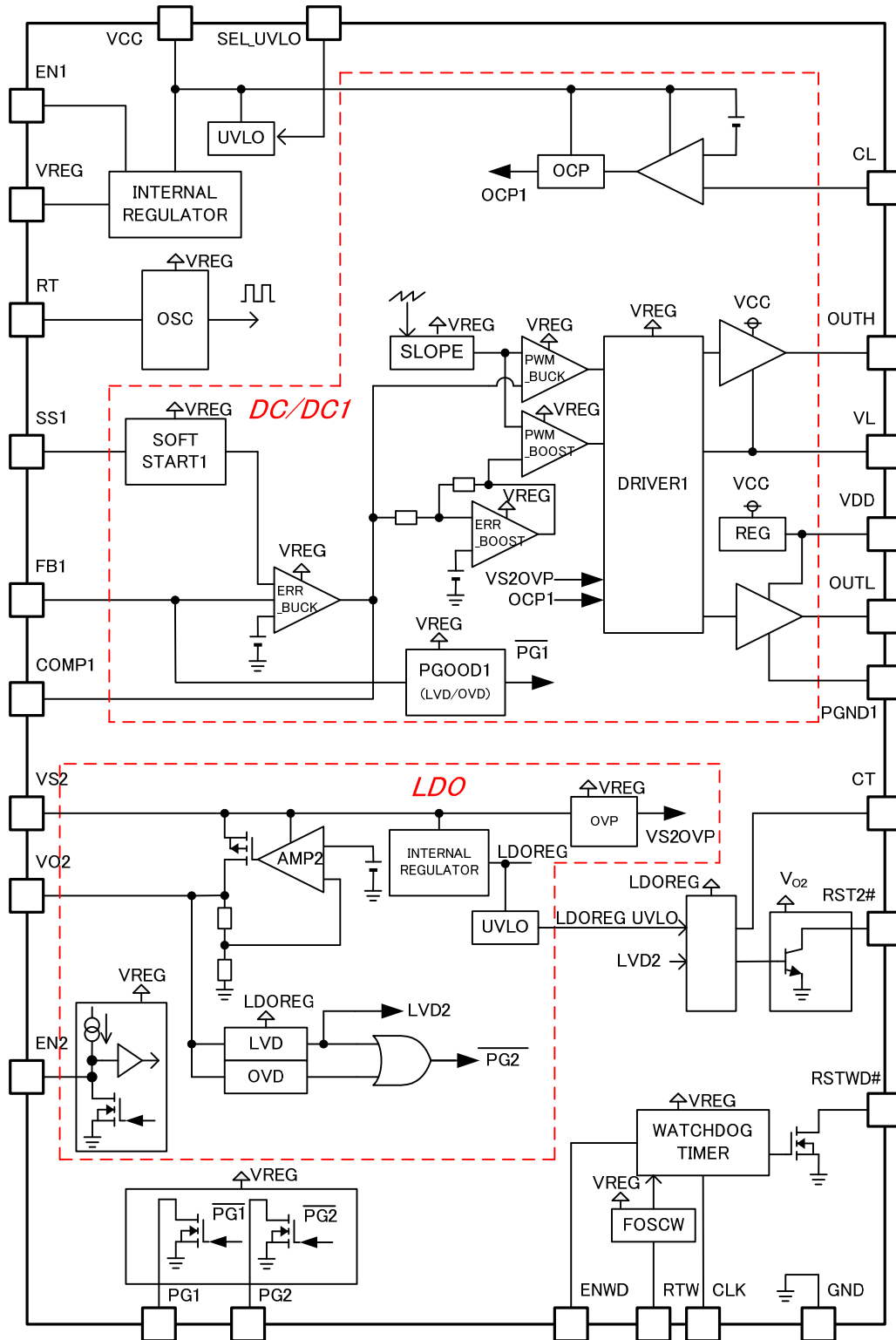


Pin Description

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	VL	Pch FET gate clamp	16	PG1	Power good output for DC / DC1
2	N.C.	Not connected	17	RSTWD#	Reset Output for WDT
3	OUTH	Pch MOSFET drive	18	RST2#	Reset Output for LDO
4	N.C.	Not connected	19	ENWD	WDT enable pin
5	CL	Overcurrent detection setting	20	CLK	Clock input
6	VCC	Supply voltage input	21	CT	Reset Delay
7	EN1	Output ON / OFF for DC / DC1	22	RTW	Frequency setting for WDT
8	T3	Test pin ^(Note 1)	23	RT	Frequency setting
9	VREG	Internal power supply	24	GND	Ground pin
10	EN2	Output ON / OFF for LDO	25	SS1	Soft start time setting for DC / DC1
11	SEL_UVLO	Select Pin for VCC UVLO	26	COMP1	Error-amp output for DC / DC1
12	T4	Test pin ^(Note 1)	27	FB1	Feedback for DC / DC1
13	VS2	Supply Voltage Input for LDO	28	VDD	Nch MOSFET drive supply
14	VO2	5 V Output	29	OUTL	Nch MOSFET drive
15	PG2	Power good output for LDO	30	PGND1	Power Ground

(Note 1) Short with GND

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
VCC Voltage (Note 1)	V _{CC}	40	V
VS2 Voltage (Note 1)	V _{S2}	40	V
CL Voltage	V _{CL}	VCC	V
EN1 Voltage	V _{EN1}	VCC	V
VREG Voltage	V _{REG}	7	V
VDD Voltage	V _{DD}	7	V
SS1 Voltage	V _{SS1}	VREG	V
RST2#, RSTWD#	V _{RST2#} , V _{RSTWD#}	7	V
CLK, RTW, CT, ENWD	V _{CLK} , V _{RTW} , V _{CT} , V _{ENWD}	7	V
PG1, PG2	V _{PG1} , V _{PG2}	7	V
EN2	V _{EN2}	VREG	V
Power Dissipation (Note 2)	P _d	4.69	W
Storage Temperature Range	T _{stg}	-55 to +150	°C
Junction Temperature	T _{jmax}	150	°C

(Note 1) P_d should not be exceeded.

(Note 2) If mounted on a standard ROHM 4 layer PCB (copper foil area: 70 mm × 70 mm) (Standard ROHM PCB size: 70mm × 70 mm × 1.6mm)
Reduce by 37.52 mW / °C (T_a ≥ 25 °C)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Rating

Parameter	Symbol	Min	Max	Unit
Voltage Power Supply	V _{CC} (Buck Boost mode)	4 (Note 1)	30	V
	V _{CC} (Buck mode)	6	30	V
	V _{S2}	5	10	V
Oscillation Frequency	F _{OSC}	200	550	kHz
WDT Oscillation Frequency	F _{OSCW}	50	250	kHz
OUTH Current Ability	I _{OUTH}	-	1.5	A
OUTL Current Ability	I _{OUTL}	-	1.5	A
V _{O2} Current Ability	I _{VO2}	-	600 (Note 2)	mA
Operating Temperature Range	T _{opr}	-40	+125	°C

(Note 1) Initial startup is over 4.5 V

(Note 2) P_d should not be exceeded.

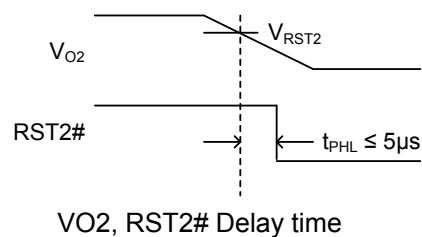
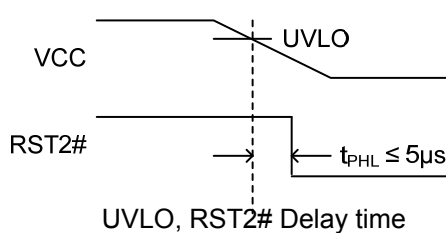
Electrical Characteristic(Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_a \leq +125\text{ }^{\circ}\text{C}$, $4\text{ V} \leq V_{CC} \leq 30\text{ V}$, $5\text{ V} \leq V_{S2} \leq 10\text{ V}$)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
All						
Standby Current 1	I _{ST1}	-	0	10	μA	T _a = 25 °C
Standby Current 2	I _{ST2}	-	-	30	μA	T _a = 125 °C
Circuit Current	I _{VCC}	5	8	12	mA	RT = 33 kΩ, FB1 = 1.0 V
Oscillation Frequency	F _{OSC}	315	350	385	kHz	RT = 33 kΩ
VREG Output Voltage	V _{REG}	3.0	3.5	4.0	V	
VDD Output Voltage	V _{DD}	4.5	5	5.5	V	V _{CC} = 12 V
UVLO_VCC Detection Voltage 1	V _{UVLOVCC1}	3.30	3.60	3.90	V	SEL_UVLO = OPEN
UVLO Hysteresis Voltage 1	V _{UVVCHYS1}	200	400	600	mV	SEL_UVLO = OPEN
UVLO_VCC Detection Voltage 2	V _{UVLOVCC2}	5.27	5.58	5.89	V	SEL_UVLO = GND
UVLO_VCC Release Voltage 2	V _{UVVCCRE2}	5.35	5.67	6.0	V	SEL_UVLO = GND
UVLO Hysteresis Voltage 2	V _{UVVCHYS2}	50	75	-	mV	SEL_UVLO = GND
EN1 L Threshold	V _{EN1L}	-	-	0.5	V	
EN1 H Threshold	V _{EN1H}	2.5	-	-	V	
EN1 Input Resistance	R _{EN1}	180	375	570	kΩ	V _{CC} = 5 V
SEL_UVLO Threshold	V _{SEL_UVLO}	-	V _{REG} / 2	-	V	
SEL_UVLO Output Current	I _{SEL_UVLO}	5	14	23	μA	SEL_UVLO = 0 V
DC / DC1 (Buck - Boost DC / DC Controller)						
FB1 Voltage	V _{REF08}	0.784	0.800	0.816	V	FB1 = COMP1
FB1 Input Bias Current	I _{FB1}	-1	0	+1	μA	FB1 = 0.8 V
Soft Start Quick Charge Current	I _{SS0}	55	110	165	μA	
Soft Start Charge Current	I _{SS1}	5	10	15	μA	
Soft Start selected Voltage	V _{SS0}	0.3	0.7	1.5	V	
Soft Start End Voltage 1	V _{SS1}	-	V _{SS0} + V _{REF08}	-	V	
Soft Start Cramp Voltage	V _{SSCL1}	2.2	2.8	3.3	V	SS1 = open
VCC - VL Voltage	V _L	8	10	12	V	V _{CC} ≥ 12 V VCC - VL
Hi - Side OUTH ON - Resistance	R _{ONHH}	-	1.7	-	Ω	V _{CC} = 12 V OUTH - VCC
Lo - Side OUTH ON - Resistance1	R _{ONHL1}	-	3	-	Ω	V _{CC} = 12 V OUTH - VL
Lo - Side OUTH ON - Resistance2	R _{ONHL2}	-	-	30	Ω	V _{CC} = 4 V OUTH - PGND
Hi - Side OUTL ON - Resistance	R _{ONLH}	-	18	-	Ω	V _{CC} = 12 V
Lo - Side OUTL ON - Resistance	R _{ONLL}	-	22	-	Ω	V _{CC} = 12 V
Over current detection CL voltage (Low)	V _{CL_L}	86	100	114	mV	V _{CC} - CL Voltage, V _{CC} = 12 V
Over current detection CL voltage (High)	V _{CL_H}	172	200	228	mV	V _{CC} - CL Voltage, V _{CC} = 12 V
Maximum ON Duty (OUTL)	T _{ON}	-	92	-	%	F _{osc} = 600 kHz

Electrical Characteristic - Continuance

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
LDO (5.0 V Output LDO)						
Output Voltage 2	V _{O2}	4.90	5.00	5.10	V	6.0 V ≤ VS2 ≤ 10 V, 5 mA ≤ I _{VO2} ≤ 600 mA
Drop Voltage	ΔV _{O2}	-	-	0.6	V	VS3 = 4.65 V, I _{VO2} = 600 mA
Under voltage detection voltage	V _{RST2}	4.50	4.625	4.75	V	
Under voltage hysteresis voltage	V _{RSTH2}	30	-	150	mV	
EN2 Threshold Voltage	V _{EN2}	0.6	0.8	1.0	V	
EN2 Charge Current	I _{EN2}	4	8	12	μA	EN2 = 0.2 V
VS2 Over voltage detection voltage	V _{OVS}	12.5	14	15.5	V	
RST2#, RSTWD#						
Reset Delay Time	t _{RST}	30	56	160	ms	CT = 0.47 μF
Reset L Voltage 1	V _{RSTL1}	-	-	0.25	V	V _{O2} = 1.0 V, I _{RST} = 100 μA
Reset L Voltage 2	V _{RSTL2}	-	-	0.4	V	I _{RST} = 1 mA
Reset Response Time	t _{PHL}	-	-	5	us	RST# Pull up Resistance 4.7 kΩ
WDT Oscillation Frequency	F _{OSCW}	75	100	125	kHz	R _{TW} = 51 kΩ
CLK FAST NG Threshold	t _{WF}	$\frac{507}{F_{OSCW}}$	$\frac{512}{F_{OSCW}}$	$\frac{517}{F_{OSCW}}$	s	
CLK SLOW NG Threshold	t _{WS}	$\frac{6635}{F_{OSCW}}$	$\frac{6655}{F_{OSCW}}$	$\frac{6675}{F_{OSCW}}$	s	
WDT Reset Time	t _{WRES}	$\frac{123}{F_{OSCW}}$	$\frac{128}{F_{OSCW}}$	$\frac{133}{F_{OSCW}}$	s	
CLK L Threshold	V _{CLKL}	-	-	0.8	V	
CLK H Threshold	V _{CLKH}	2.0	-	-	V	
ENWD L Threshold	V _{ENWDL}	-	-	0.8	V	
ENWD H Threshold	V _{ENWDH}	2.0	-	-	V	
RSTWD ON Resistance	R _{RSTWD}	50	100	200	Ω	I _{RSTWD} = 100 μA
PG1, PG2						
PG ON - Resistance	R _{PG1} R _{PG2}	0.5	1.0	2.0	kΩ	
PG1 Under Voltage Detection voltage	V _{LVPG1}	0.62	0.67	0.72	V	FB1 Voltage
PG1 Under Voltage Hysteresis	V _{LVPH1}	20	-	100	mV	FB1 Voltage
PG1 Over Voltage Detection Voltage	V _{OVPG1}	0.88	0.94	1.00	V	FB1 Voltage
PG1 Over Voltage Hysteresis	V _{OVPH1}	20	-	100	mV	FB1 Voltage
PG2 Under Voltage Detection Voltage	V _{LVPG2}	4.50	4.625	4.75	V	V _{O2} Voltage
PG2 Under Voltage Hysteresis	V _{LVPH2}	30	-	150	mV	V _{O2} Voltage
PG2 Over Voltage Detection Voltage	V _{OVPG2}	5.25	5.38	5.50	V	V _{O2} Voltage
PG2 Over Voltage Hysteresis	V _{OVPH2}	30	-	150	mV	V _{O2} Voltage

Reset response time (t_{PHL})



Typical Performance Curves

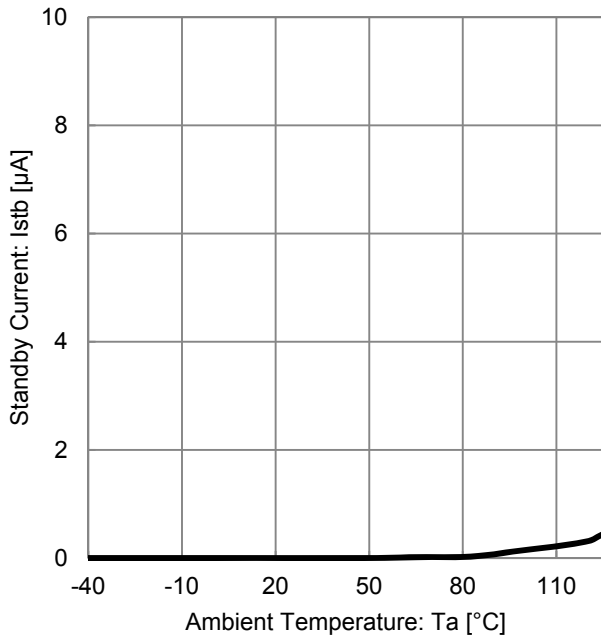


Figure 1. Standby Current vs. Temperature

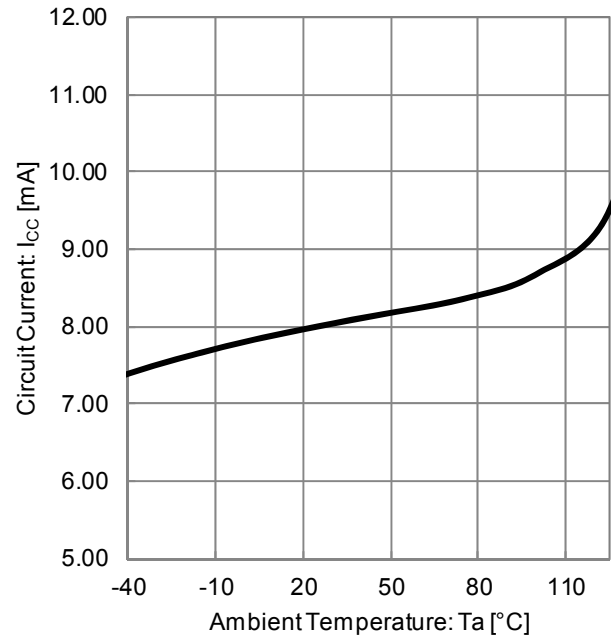


Figure 2. Circuit Current vs. Temperature

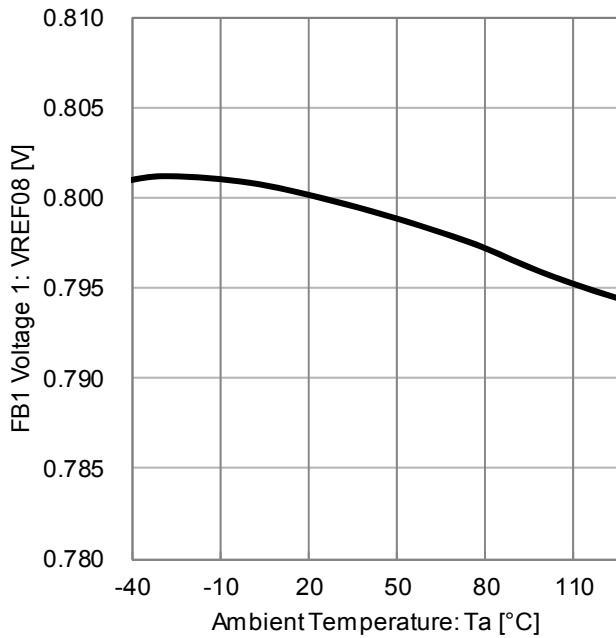


Figure 3. FB1 Voltage vs. Temperature

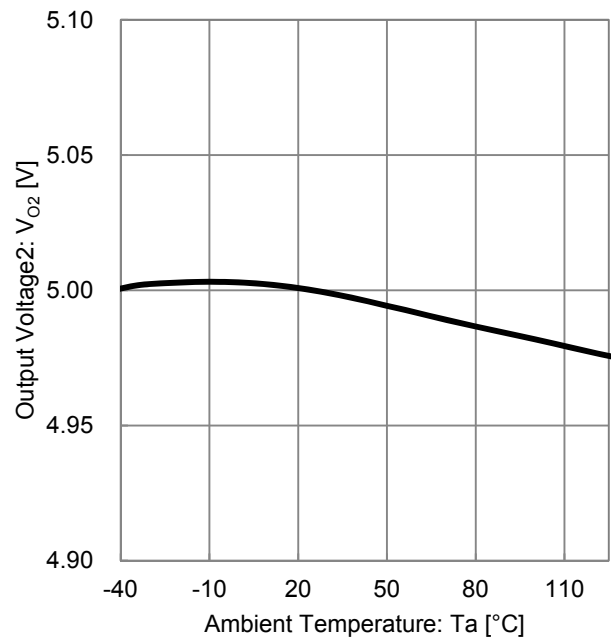


Figure 4. Output Voltage2 vs. Temperature

Typical Performance Curves - Continuance

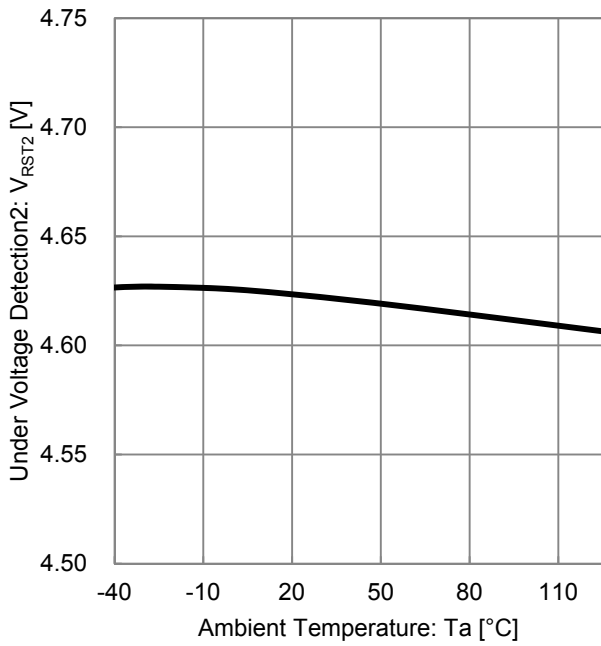


Figure 5. Under Voltage Detection2 vs. Temperature

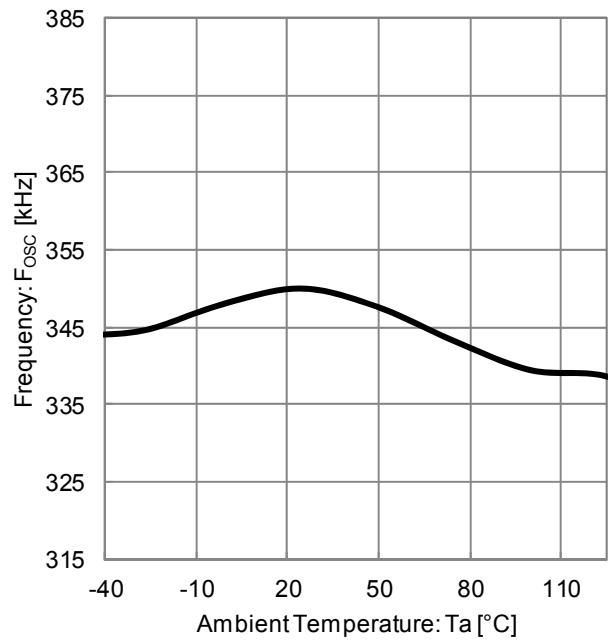


Figure 6. Frequency vs. Temperature

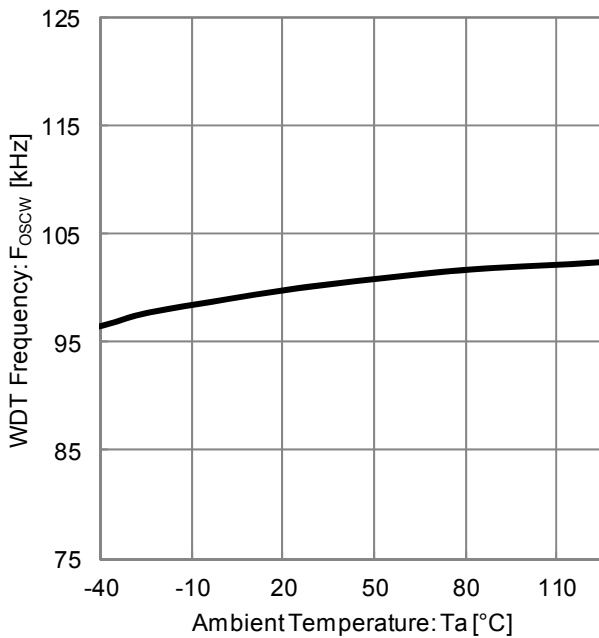


Figure 7. WDT Frequency vs. Temperature

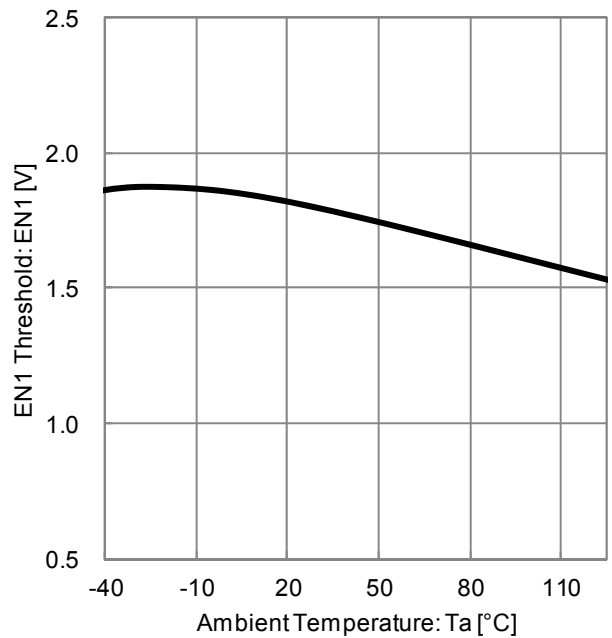


Figure 8. EN1 Threshold vs. Temperature

Typical Performance Curves - Continuance

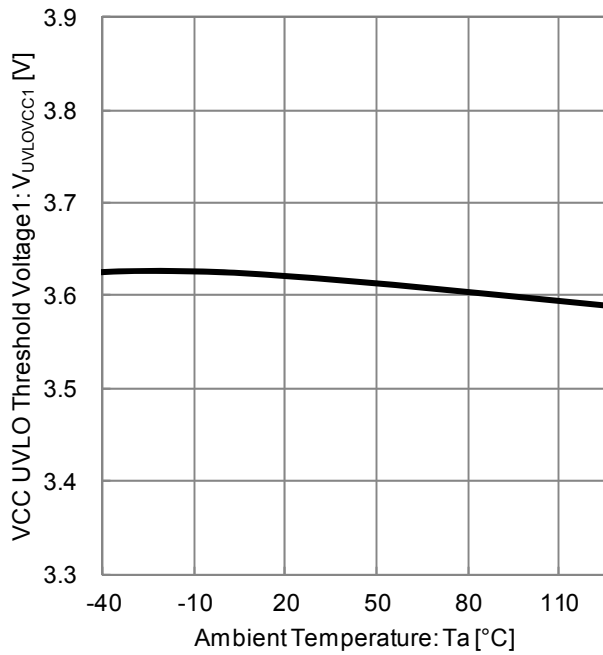


Figure 9. VCC UVLO Threshold Voltage1 vs. Temperature

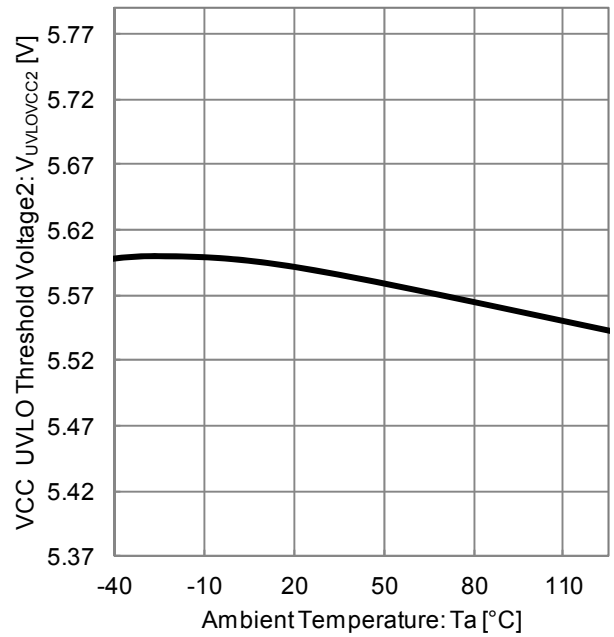


Figure 10. VCC UVLO Threshold Voltage2 vs. Temperature

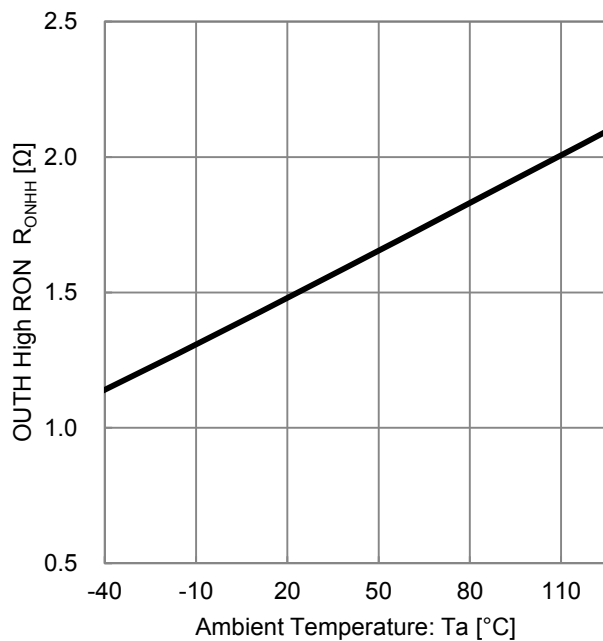


Figure 11. OUTH High RON vs. Temperature

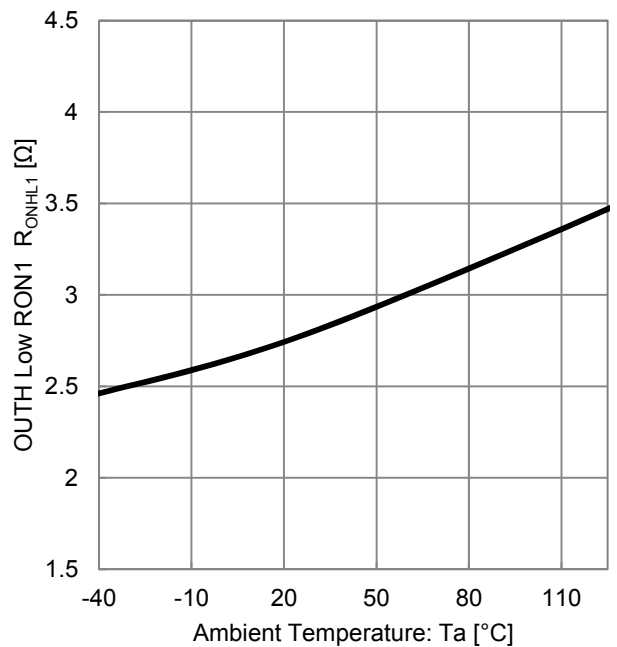


Figure 12. OUTH Low RON1 vs. Temperature

Typical Performance Curves - Continuance

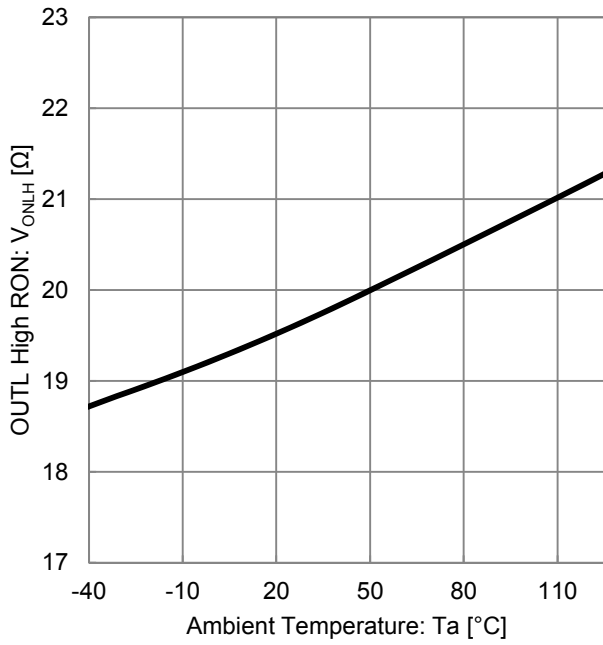


Figure 13. OUTL High RON vs. Temperature

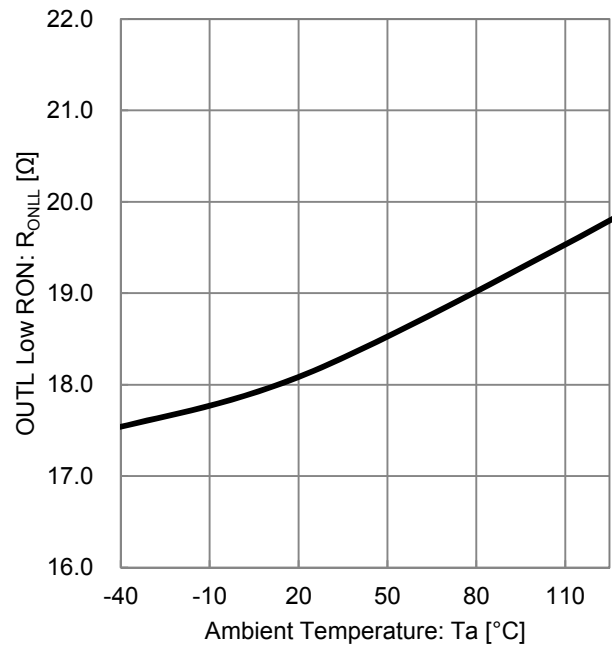


Figure 14. OUTL Low RON vs. Temperature

Description of Blocks

- Under Voltage Lockout circuit (VCC_UVLO)
 This is a Low Voltage Error Prevention Circuit.
 In case of SEL_UVLO = OPEN, if the VCC drops below 3.6 V (Typ), the VCC_UVLO is activated and the output circuit shuts down. In case of SEL_UVLO = GND, if the VCC drops below 5.58 V (Typ), the VCC_UVLO is activated and the output circuit shuts down.
- Thermal Shut Down (TSD)
 The TSD protects the device from overheating.
 If the chip temperature (Tj) reaches 175 °C (Typ), the circuit shuts down
- Over Voltage Detection (OVD)
 If DC / DC1 and LDO output voltage exceeds OVD, each PGOOD Pin turns Low.
 DC / DC1 OVD monitors FB1 voltage and LDO OVD monitors V_{O2} voltage.
 PGOOD pin is an open drain output and a pull up resistor should be connected to PGOOD if this function is being used.
- Low Voltage Detection (LVD)
 If DC / DC1 and LDO output voltage is below LVD, each PGOOD Pin turns Low.
 DC / DC1 LVD monitors FB1 voltage and LDO LVD monitors V_{O2} voltage.
 PGOOD pin is an open drain output, and a pull up resistor should be connected to PGOOD if this function is being used.
- Over Current Protection (OCP)
 DC / DC1 has two levels over current protection with different control system as shown below.

 - 1) OCP1 low level operations (OCP1_L)
 In case the voltage between VCC and CL exceeds 100 mV (Typ), OCP1 (low level operation) is activated and the switching pulse width of OUTH and the switching pulse width of OUTL are limited. Also, if this pulse limited status continues during 256 clock times where the FB1 pin voltage drops below the under voltage detection level, the soft start pin capacitor is discharged and the output is turned OFF during 8192 clock times.
 During the 8192 clock in which the output is turned OFF, the logic of OUTH and OUTL pin changes as follows; OUTH = H and OUTL = H. After the 8192 clock the chip returns to normal operations and the soft start pin is recharged.
 - 2) OCP1 high level operations (OCP1_H)
 In case the inter VCC - CL pin voltage exceeds 200 mV (Typ), the chip goes into OCP1 high level operations, the soft start pin capacitor is discharged and the output is turned OFF for 8192 clk. During the 8192 clock in which the output is turned OFF, the logic of OUTH and OUTL pin changes as follows; OUTH = H and OUTL = H. After the 8192 clock the chip returns to normal operations and the soft start pin is recharged.

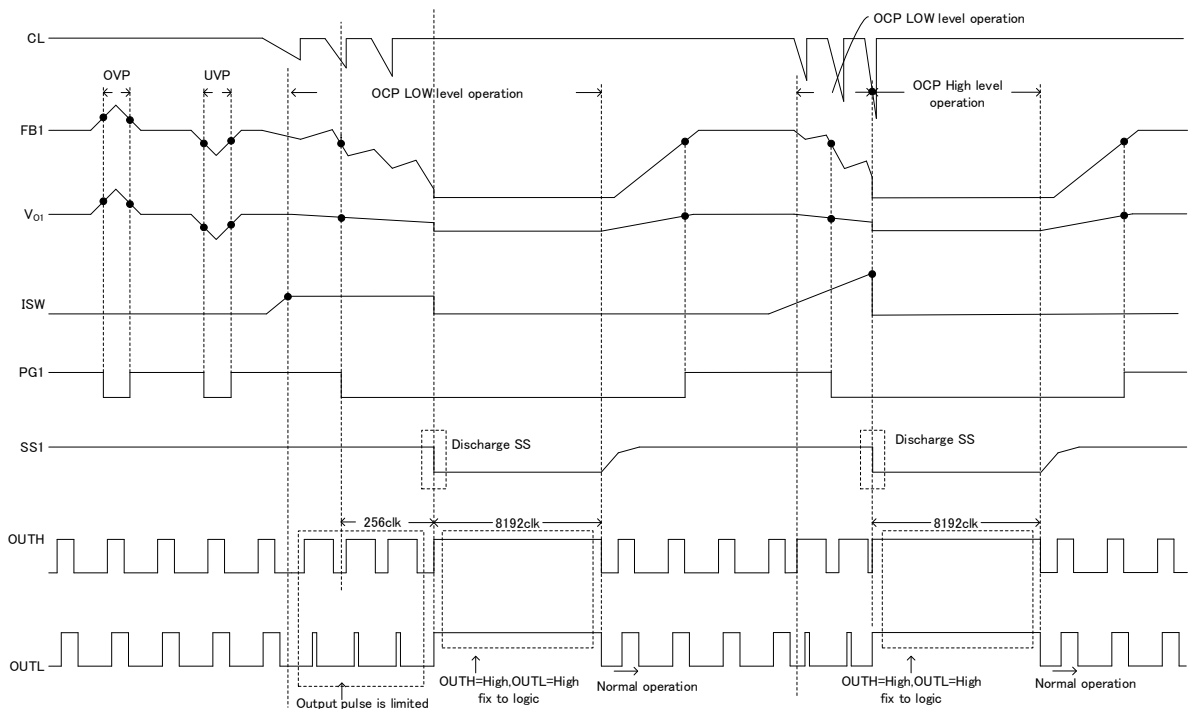
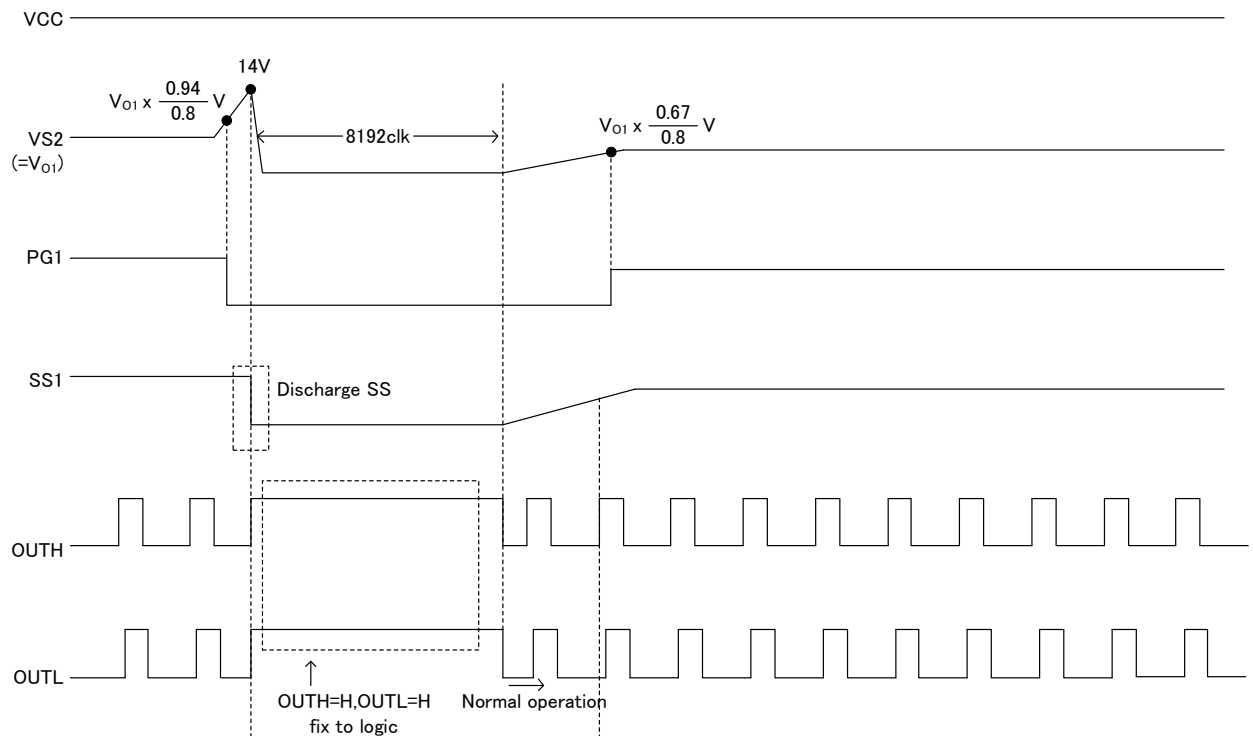


Figure 15. Timing chart for DC / DC1 protection

- If the output current of LDO exceed OCP, the output current is limited and the output voltage is lowered.

■ Over Voltage Protection (VS2)

In case the VS2 voltage exceeds 14 V (Typ), the chip goes into VS2 OVP, the SS1 capacitor is discharged and the DC / DC1 output is turned OFF for 8192 clock. During the 8192 clock in which the output is turned OFF, the logic of OUTH and OUTL changes as follows; OUTH = H and OUTL = H. After the 8192 clock the chip returns to normal operations and the SS1 is recharged.



All numerical values are Typical.

Figure 16. VS2 Over voltage protection

■ RST#, RSTWD# pin

In case of ENWD = L, RSTWD# voltage is pull up voltage.
 In case of ENWD = H, WDT operation starts. If WDT is in abnormal condition, RSTWD# outputs 'L'.
 If V_{O2} voltage is below the LVD, reset voltage (RST#) output is low.
 If V_{O2} exceed the reset release voltage, CT is charged and after tPOR, reset voltage outputs high.

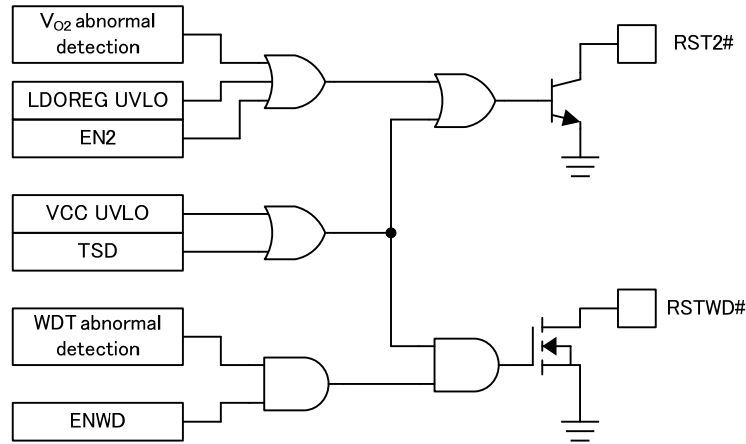


Figure 17. RST#, RSTWD# Logic Circuit

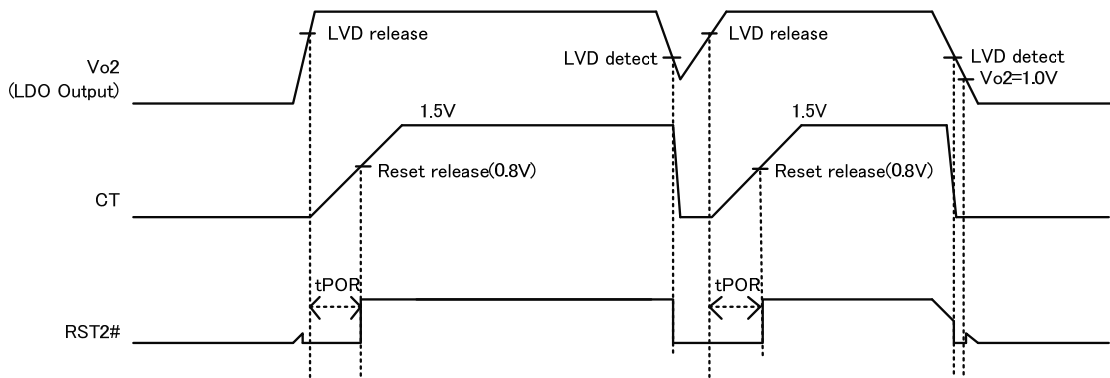


Figure 18. RST2#,Timing Chart

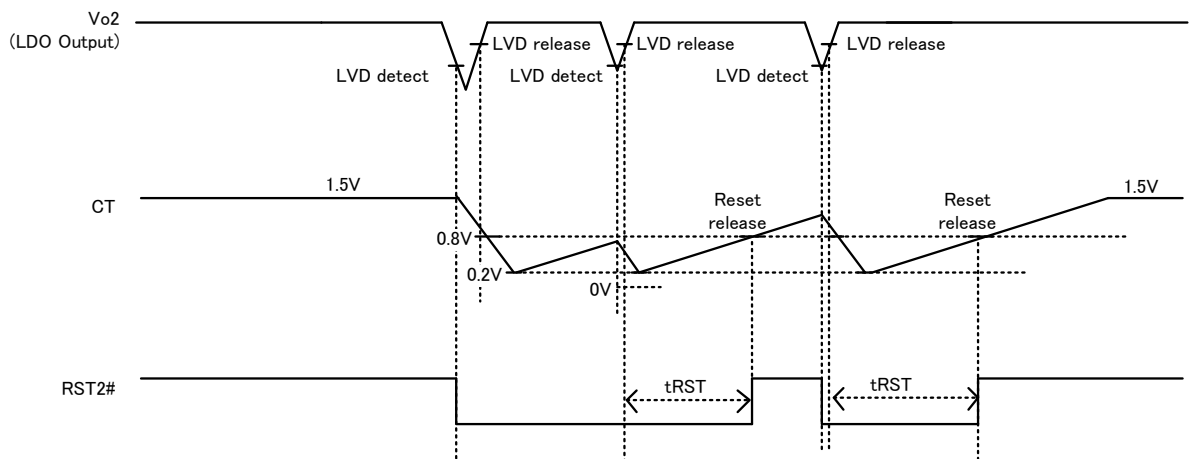


Figure 19. Timing chart (detection of LVD between reset)

- Oscillator for Watch Dog Timer (FOSCW)**
 This block creates a reference frequency of the Watch Dog Timer. The oscillation frequency is determined by the RTW resistance. The oscillation frequency can be set in the range of 50 kHz to 250 kHz.
- WATCH DOG TIMER**
 Microcontroller (μ C) operation is monitored with CLK pin. Window watch dog timer is included to enhance the assurance of the system. WDT starts operating when ENWD becomes high. CLK pin voltage must be Low when ENWD switches to High.
 WDT monitors both edges of CLK pin (rising edge and falling edge). If width of both edges are shorter than Fast NG or longer than Slow NG, RSTWD turns low for a WDT reset time (t_{WRES}). Since the width of Fast NG and Slow NG depends on a number of F_{OSCW} , Fast NG and Slow NG are variable by frequency of F_{OSCW} . If F_{OSCW} is unusual (ex. RTW is short to ground), RSTWD turns low. In case of using RSTWD, pull-up resistor is needed because RSTWD is an open drain.

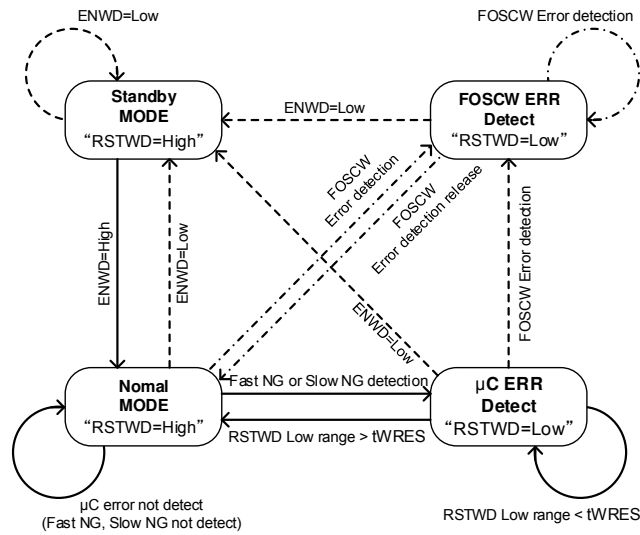
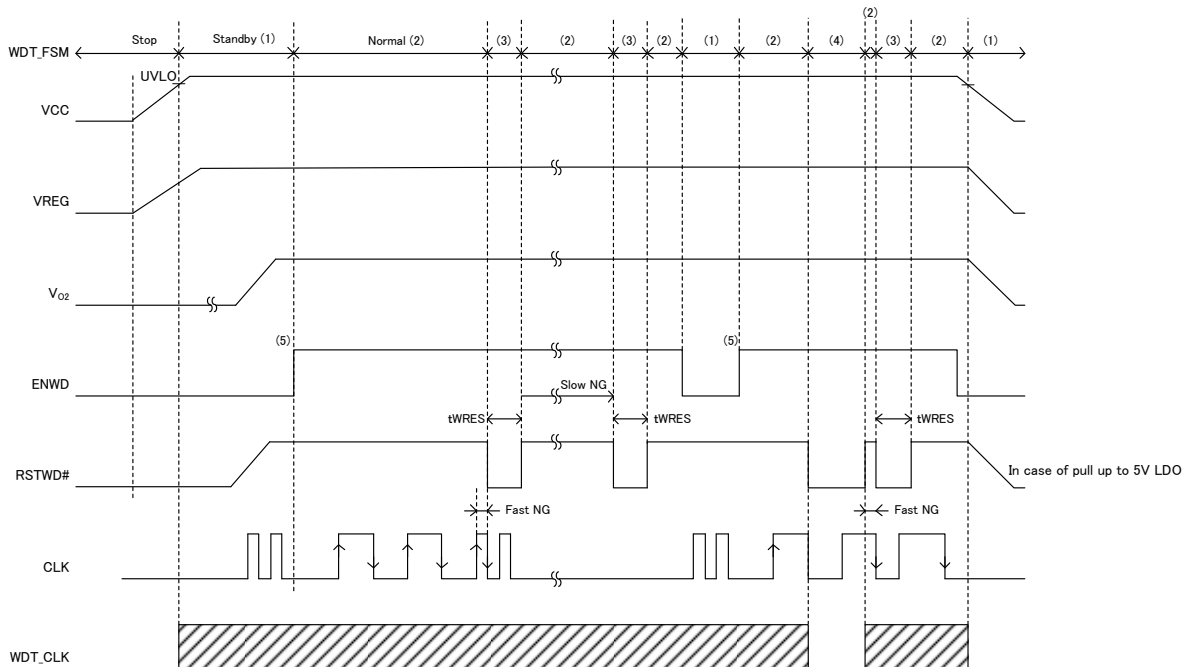


Figure 20. Watch Dog Timer State Change Diagram (WDT FSM)



- (1): Standby Mode, (2): Normal Mode, (3): μ C ERR Detect, (4): OSC_WDT ERR Detect (See Figure 20. WDT FSM)
- (5): When ENWD is changed Low to High, it is necessary that CLK is Low.

Figure 21. WDT Timing Chart

External Components Selection

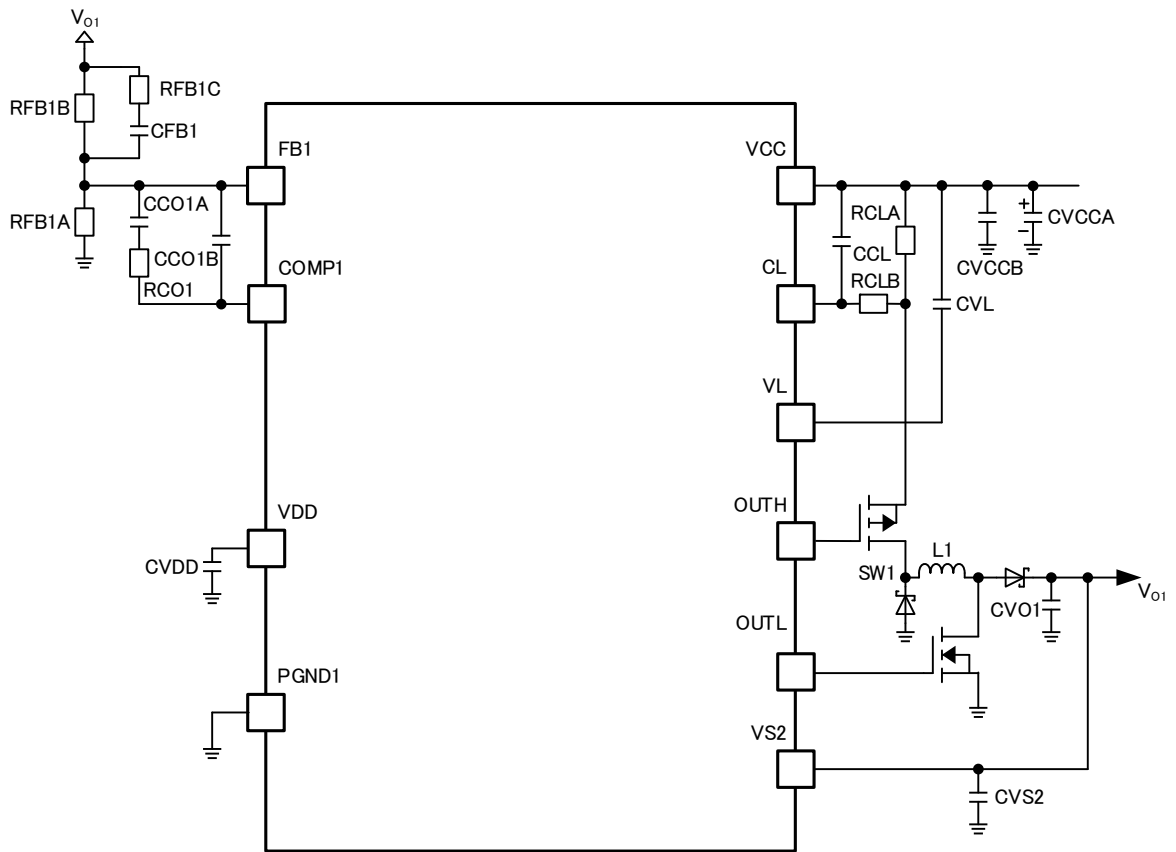


Figure 22. Application Example 1

- (1) Buck mode ($V_{CC} \gg V_{O1}$)
 In case the input voltage is high compared to the output voltage, the chip will go into buck mode, resulting OUTH to repeatedly switch between H and L and that the OUTL will go to L (= OFF). This operation is the same as that of standard step-down switching regulators.
 Shown are the OUTH and OUTL waveforms on the right.
 ON duty of PMOS (D_{pon}), V_{CC} and V_{O1} are shown in the following equation.

$$V_{CC} \times D_{pon} = V_{O1} \quad (\text{eq. 1})$$

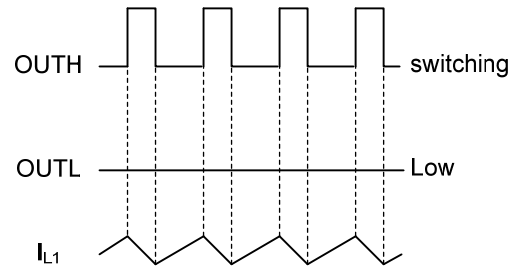


Figure 23

- (2) Buck-Boost mode ($V_{CC} \approx V_{O1}$)
 In case the input voltage is close to the output voltage, the chip will go into buck-boost mode, resulting both the OUTH and OUTL to repeatedly switch between H and L. Concerning the OUTH, OUTL timing, the chip internally controls where the following sequence is upheld; when OUTH: $H \rightarrow L$, OUTL: $H \rightarrow L$.
 Shown below are the OUTH and OUTL waveforms.

① $V_{CC} > V_{O1}$

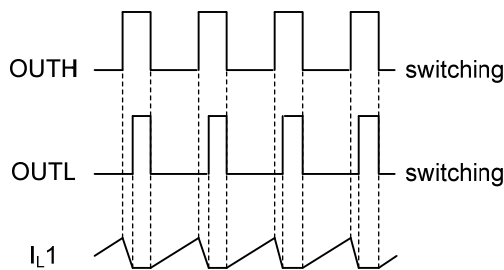


Figure 24

② $V_{CC} < V_{O1}$

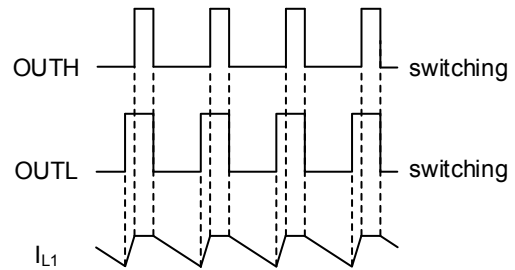


Figure 25

*The timing excludes the SW delay

The relationship between ON duty of PMOS (D_{pon}), ON duty of NMOS (D_{non}), V_{CC} and V_{O1} is shown in the following equation.

$$\frac{V_{CC} \times D_{pon}}{(1 - D_{non})} = V_{O1} \quad (\text{eq. 2})$$

The calculation formula of D_{pon} and D_{non} are shown in Page 17.

- (3) Boost mode ($V_{CC} \ll V_{O1}$)
 In case the input voltage is low compared to the output voltage, the chip will go into boost mode, resulting OUTH to go to L (= ON) and OUTL will repeatedly switch between H and L. This operation is the same as that of standard step-up switching regulators.
 Max duty of OUTL is limited by internal circuit.
 ON duty of NMOS (D_{non}), V_{CC} and V_{O1} are shown in the following equation.

$$V_{O1} \times (1 - D_{non}) = V_{CC} \quad (\text{eq. 3})$$

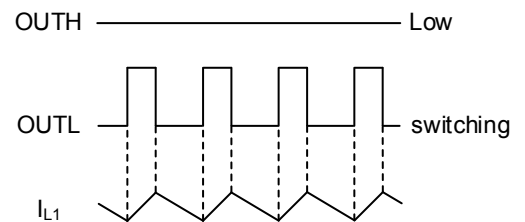


Figure 26

(4) Voltage for Mode Switching and Duty Control

In the event of mode switching from Boost to Buck-Boost or vice versa, mode switching input voltage is dependent on output voltage, the gain of inverting amplifier and the cross duty. The general description is shown below.

The duty of OUTH is controlled by output of error amp (COMP1) and SLOPE voltage.

Also, OUTL duty is controlled by the output voltage of the inverting amplifier in chip (BOOSTCOMP) and SLOPE voltage.

In case $V_{CC} = V_{O1}$, COMP1 voltage becomes equal to BOOSTCOMP voltage, and switching control timing of OUTH and OUTL becomes identical accordingly.

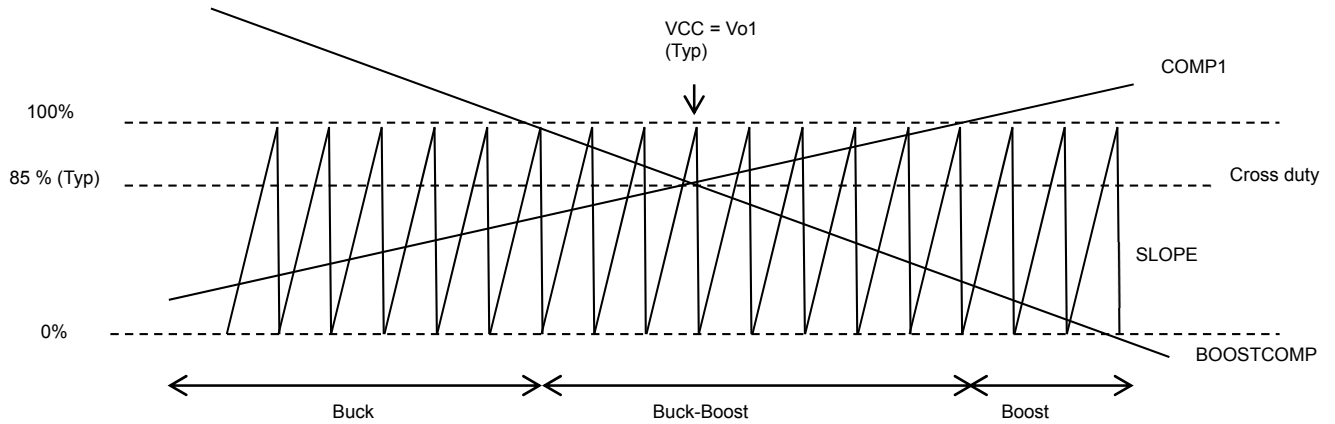


Figure 27. Buck-Boost operation controlled by COMP1, BOOSTCOMP and SLOPE voltage

ON duty of PMOS in this condition is called the cross duty ($D_x = 0.85$, Typ). D_{pon} and D_{non} can be calculated by the following equation, assuming the gain of the inverting amplifier as A (1.5, Typ).

$$\begin{aligned}
 D_{non} &= 1 - D_x + A(D_{pon} - D_x) \\
 &= 1.5D_{pon} - 1.125 \quad (\text{Note 1}) \quad (\text{eq. 4})
 \end{aligned}$$

From eq.3, eq.4 and $D_{pon} = 1$, the input voltage at transition between buck - boost and boost mode is calculated as follows;

$$\begin{aligned}
 V_{CC} &= \{D_x + A(1 - D_x)\}V_{O1} \\
 &= 0.625 \times V_{O1} \quad (\text{Note 1}) \quad (\text{eq. 5})
 \end{aligned}$$

Also, from eq.1, eq.4 and $D_{non} = 0$, the input voltage at transition between buck - boost and buck mode is calculated as follows;

$$V_{CC} = \frac{V_{O1} \times A}{\{(1+A)D_x - 1\}} = 1.333 \times V_{O1} \quad (\text{Note 1})$$

Be sure to confirm D_x and A value under the actual application because these parameters vary depending on conditions of use and external components selected.

D_x varies with oscillating frequency shown in Figure 28.

In addition, 'A' value can be calculated by D_{non} / D_{pon} .

(Note 1) A = 1.5 (Typ), $D_x = 0.85$ (Typ)

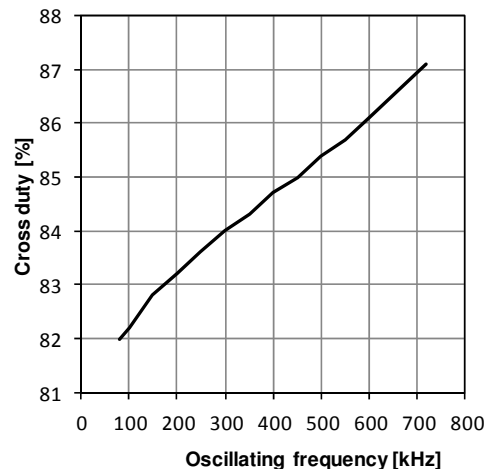


Figure 28. Cross duty vs. frequency characteristics

1. Setting the output L1 value (DC / DC1)

It is necessary to use LC filter. The use of a big inductor helps lower the inductor ripple current and output ripple voltage, even though cost is higher and the size is bigger.

The inductance is shown in the following equation.

The coil value significantly influences the output ripple current. Thus, as seen bellow, the larger coil and the higher switching frequency, the lower ripple current it becomes. The optimal output ripple current setting is 30 % of maximum current.

• DC / DC1 (at Buck - Boost)

Buck mode	Buck-Boost mode		Boost mode
	$V_{CC} > V_{O1}$	$V_{CC} < V_{O1}$	
$\Delta I_{L1} = \frac{(V_{CC} - V_{O1}) \times V_{O1}}{L1 \times V_{CC} \times f}$	$\Delta I_{L1} = \frac{(V_{CC} - V_{O1}) \times D_{pon}}{L1 \times f}$	$\Delta I_{L1} = \frac{(V_{O1} - V_{CC}) \times D_{noff}}{L1 \times f}$	$\Delta I_{L1} = \frac{(V_{O1} - V_{CC}) \times V_{CC}}{L1 \times V_{O1} \times f}$
$\bar{I}_{L1} = I_{O1}$	$\bar{I}_{L1} = \frac{I_{O1}}{D_{noff}}$		

ΔI_L : Ripple current, \bar{I}_L : Average coil current, f: Oscillating frequency

$$D_{pon}: PMOS\ ON\ duty = \frac{V_{O1} \times Dx (1 + A)}{(V_{CC} + A \times V_{O1})} = 2.13 \times V_{O1} / (V_{CC} + 1.5 \times V_{O1}) \quad (Typ)$$

$$D_{noff}: NMOS\ OFF\ duty = (1 + A) \times Dx - A \times D_{pon} = 2.13 - 1.5 \times D_{pon} \quad (Typ)$$

• DC / DC1 (at Buck)

$$\Delta I_{L1} = \frac{(V_{CC(MAX)} - V_{O1}) \times V_{O1}}{V_{CC(MAX)} \times f_{SW} \times L1}$$

($V_{CC(MAX)}$: Maximum input voltage, ΔI_{L1} : Inductor ripple current, V_{O1} : Output voltage 1, f_{sw} : Oscillating frequency)

An output current in excess of the coil current rating will cause magnetic saturation to the coil and decrease efficiency. The following equation shows the peak current I_{LMAX} assuming the efficiency as η .

It is recommended to secure sufficient margin to ensure that the peak current does not exceed the coil current rating.

$$I_{LMAX} = \frac{1}{\eta} \left(\bar{I}_L + \frac{\Delta I_L}{2} \right)$$

Use low resistance (DCR, ACR) coils to minimize coil loss and increase efficiency.

When load current is low, DC / DC1 operates discontinuously so set ΔI_L in a way it operates continuously (I_{L1} keeps continuously flowing).
 The condition of continuous operation is shown in the following equation.

• DC / DC1

$$I_{O1} > \frac{(V_{CC} - V_{O1}) \times V_{O1}}{2 \times V_{CC} \times f_{SW} \times L1}$$

(I_{O1} : Load current)

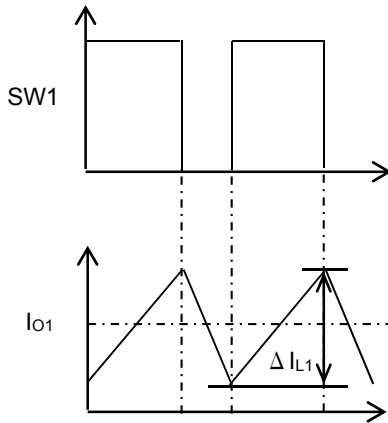


Figure 29. Continuous operation

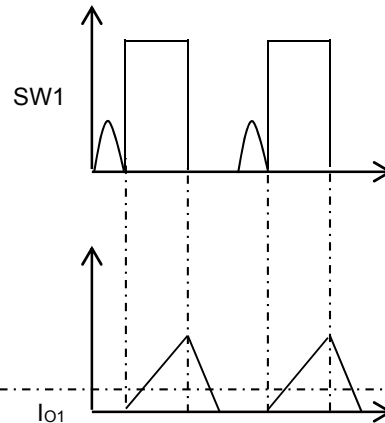


Figure 30. Discontinuous operation

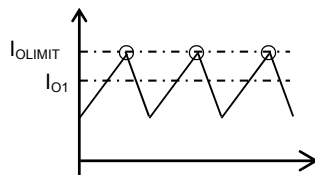


Figure 31. Over current detection

Shielded type inductor (closed magnetic circuit) is recommended. Open magnetic circuit type inductor can be used for low cost applications if noise is not of concern. But in this case, there is magnetic field radiation between the parts and thus keep enough spacing between the parts.

For ferrite core inductor type, please note that magnetic saturation may occur. Saturation needs to be avoided at all times. Precautions must be taken into account on the given provisions of the current rating because it differs according to each manufacturer.

Please confirm the rated current at the maximum ambient temperature of the application to the coil manufacturer.

2. Setting the output capacitor C_{VO1} value (DC / DC1)

The maximum output current is limited by the over current protect operation current as shown in below equation.

$$I_{O(MAX)} = I_{LIMIT(MIN)} - \frac{\Delta I_O}{2}$$

$I_{O(MAX)}$: Maximum output current, $I_{LIMIT(MIN)}$: Minimum over current protect operation level (1ch is external set)
 When the ΔI_L is low, the Inductor core loss (iron loss), the loss due to ESR of the output capacitor and the ΔV_{PP} will become low. ΔV_{PP} is expressed as follows:

Buck mode	Boost mode
$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{8 \times C_{VO} \times f_{SW}}$	$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{I_O}{C_{VO} \times f_{SW}} \times \frac{V_O - V_{CC}}{V_O}$

(ESR : Output capacitor equivalence series resistance, C_O : Output capacitor volume)

By using small ESR capacitor, ΔV_{PP} voltage level can be lowered. The benefit of ceramics capacitor is low ESR and small form factor.

The frequency characteristic of ESR from the datasheet of the manufacturer should be confirmed. Choose the ceramic capacitor which exhibits low ESR in the switching frequency range that is used. On the other hand, DC biasing characteristics of the ceramic capacitor is significant so it needs to be carefully examined. For the voltage rating of the ceramic capacitor, twice or more than the maximum output voltage is usually required. By selecting these high voltages rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristic of X7R or better, is recommended.

Because the voltage rating of ceramic capacitor is low, the selection becomes difficult in the application with high output voltage. In that case, select electrolytic capacitor.

When using electrolytic capacitors, the voltage rating should be 1.2 times or more than the output voltage. Electrolytic capacitors have a high voltage rating, large capacity, small amount of DC biasing characteristic, and are generally inexpensive. Because typical failure mode is OPEN, it is effective to use electrolytic capacitor for applications where high reliability is required such as automotive. On the other hand, disadvantages are relatively high ESR and capacitance value drop at low temperatures. In this case, please take note that ΔV_{PP} may increase at low temperature conditions. Moreover, consider the lifetime characteristic of this capacitor.

The tantalum capacitor and the conductive polymer capacitor have good temperature characteristics, unlike an electrolytic capacitor. These capacitors have small amount of DC biasing characteristic like the electrolytic capacitor. For the voltage rating of the tantalum capacitor, twice or more than the maximum output voltage is usually required. For the voltage rating of the conductive polymer capacitor, 1.5 times or more than the maximum output voltage is usually required. The demerits of tantalum capacitor and conductive polymer capacitor are that a fault mode is "short" and voltages rating is low. Also the conductive polymer capacitor is expensive. For these reason, these capacitors are not used for automotive applications, because of its high reliability requirements.

Output capacitors are rated in ripple current. The RMS values of the ripple electric current obtained in the next expression must not exceed the ratings of ripple electric current.

$$I_{CVO(RMS)} = \frac{\Delta I_O}{\sqrt{12}}$$

($I_{CVO(RMS)}$: Output ripple current RMS value)

When it comes to the capacitance C_o , the value needs to be less than the value calculated by the equations below.

• DC / DC 1

$$C_{O1 (MAX)} = \frac{0.5 \text{ ms} \times (I_{LIMIT (MIN)} - I_{O1 (MAX)})}{V_{O1}}$$

($I_{LIMIT (MIN)}$): Minimum over current protect operation current (1ch is external set).
Soft start Min time DC / DC1: 0.5 ms

Boot failure may occur if the capacitance value exceeds the limits explained above. If the capacitance value is extremely large, over-current protection may be activated by the inrush current at startup, and the output may not start. Please confirm this on the actual circuit.

Capacitance values are critical parameter to determine the LC oscillation frequency. Transient response and loop stability are dependent on the C_{VO} . Please select after confirming the setting of the phase compensation circuit.

3. Setting the input capacitor C_{VCCA} / C_{VCCB} value (VCC)

Input capacitors reduce the power output impedance that is connected to VCC. Two types of capacitors are needed for input capacitor, i.e., decoupling capacitor C_{VCCB} and bulk capacitor C_{VCCA} . The decoupling capacitor of VCC needs to be 1 μF to 10 μF ceramics. The ceramic capacitors are most effective when placed as close to VCC as possible. At VCC, the ceramic capacitors need to be placed between VCC and GND and close to PMOS and the ground of schottky barrier diode. Voltage rating is recommended to be more than 1.2 times the maximum input voltage and twice the normal input voltage.

The bulk capacitor prevents line voltage drop and serves as a backup power supply to maintain the input voltage. The low ESR electrolytic capacitor with large capacitance is suitable for the bulk capacitor. It is necessary to select the capacitance value which best fits to each application. In case impedance of input side is high such as long wiring between the power supply and VCC, input voltage gets unstable when output impedance of the power supply increases resulting in oscillation or degraded ripple rejection characteristics. Large capacitor is needed in this case. It is necessary to verify that the output does not turn off in the event of Vcc drop due to transient in the actual circuit. Make sure not to exceed the rated ripple current of the capacitor in this case. The RMS of the input ripple current can be obtained from the following equation.

• DC / DC 1

$$I_{CVCCB (RMS)} = I_{O1} \times \frac{\sqrt{V_{O1}(V_{CC} - V_{O1})}}{V_{CC}}$$

($I_{CVCCB (RMS)}$): Input ripple current RMS value)

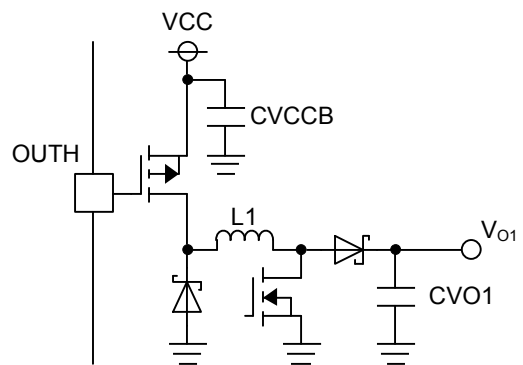


Figure 32. VCC pin

In automotive and other applications requiring high reliability, it is recommended that capacitors are connected in parallel to reduce the risk of electrolytic capacitors drying out. In case of ceramic capacitors, it is recommended make it two in series and two in parallel structures to reduce the risk of destruction due to short circuit event. Currently capacitors containing two in series or two in parallel in one package are available in the market so please contact suppliers.

4. Setting the input capacitor C_{VS2} value
Place a capacitor which is greater than 0.1 μF between VS2 and GND. Select the capacitor considering filter circuit for power supply and VS2. Since the capacitance value is dependent on the board layout and pattern, secure enough margin when selecting the capacitor. Capacitors that have good voltage and temperature characteristics are recommended.
5. Setting the output capacitor C_{VREG} value
Place a capacitor between the VREG pin and GND to avoid oscillation. 0.47 μF or greater capacitance is recommended. C_{VREG} can be electrolytic capacitor or ceramic capacitor. Secure a capacitance of 0.47 μF or greater in the voltage and temperature range in actual operating conditions. The change in capacitance value by temperature may cause oscillation. Select the capacitors which have good temperature characteristics (X7R or better), good DC bias characteristics with high voltage rating. In case significant voltage swing and load transient are expected, make sure to carry out thorough evaluation before making a decision on the capacitance value.
6. Setting the output capacitor C_{VDD} value
Place a capacitor between VDD and GND. The capacitance needs to be 0.01 μF or greater (OUTL = open) and 1 μF or greater (OUTL in use). C_{VDD} can be electrolytic or ceramic. Secure high enough capacitance in the voltage and temperature range in actual operating conditions. The change in capacitance value by temperature may cause oscillation. Select the capacitors which have good temperature characteristics (X7R or better), good DC bias characteristics with high voltage rating. In case significant voltage swing and load transient are expected, make sure to carry out thorough evaluation before making a decision on the capacitance value.
7. Setting the internal drive circuit supply capacitor C_{VL} value
Add a capacitor greater than 0.1 μF between VCC and VL. Select the capacitor considering the filter circuit for power supply and VL. Since the capacitance value is dependent on the board layout and pattern, secure enough margin when selecting the capacitor.
8. Setting output voltage (V_{O1})
 V_{O2} is fixed output while V_{O1} is adjustable.
 V_{O1} output voltage is determined by the following equation.

$$V_{O1} = 0.8 \times \frac{R_{FB1A} + R_{FB1B}}{R_{FB1A}}$$

Please set feedback resistor RFB1B below 30 k Ω to reduce the error margin by the bias current. In addition, since power efficiency is reduced when RFB1A + RFB1B is small, please set the current flowing through the feedback resistor small enough as compared to the output current I_{O1} .

9. Selection of the MOSFET (M1, M2)

In case of Buck-Boost DC / DC, DC / DC1 needs 2 external MOSFET (PMOS = M1 and NMOS = M2). In case of Buck DC / DC, DC / DC1 needs 1 external MOSFET (PMOS). Key parameters in choosing MOSFET are voltage and current rating.

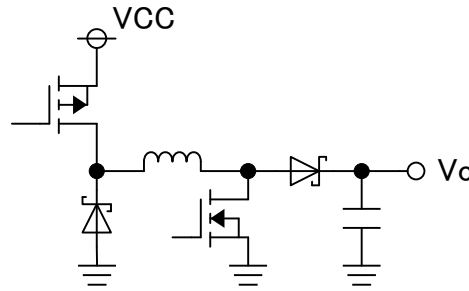


Figure 33. Select MOSFET

(i) PMOS

- V_{ds} maximum rating > VCC
- V_{gs} maximum rating > Lower value of 13 V or VCC
 - * The voltage between VCC - VL is kept at 10 V (Typ), 12 V (Max).
 - VL become 0 V when VCC become less than 10.3 V (Typ)
- Allowable current > coil peak current I_{LMAX}
 - * A value above the over current protection setting is recommended.
 - * Choosing a low ON Resistance FET results in high efficiency.

(ii) NMOS

- V_{ds} maximum rating > V_O
- V_{gs} maximum rating > VDD
- Allowable current > Coil peak current I_{LMAX}
 - * A value above the over current protection setting is recommended.
 - * Choosing a low ON Resistance FET results in high efficiency.

10. Selection of the schottky barrier diode

The diode needs to be low Vf and fast Trr. Key parameters in the diode selection are average rectified current and DC reverse voltage. Average rectified current $I_{F(AVG)}$ can be obtained from the following equation:

$$I_{F(AVG)} = I_{O1(MAX)} \times \frac{V_{CC(MAX)} - V_{O1}}{V_{CC(MAX)}}$$

($I_{F(AVG)}$: Average rectified current)

The absolute maximum rating of the average rectified current needs to be 1.2 times or greater than the $I_{F(AVG)}$.

The absolute maximum rating of the DC reverse voltage needs to be 1.2 times or greater than the maximum input voltage.

The diode power loss can be obtained by the following equation:

$$P_{Di} = I_{O1(MAX)} \times \frac{V_{CC(MAX)} - V_{O1}}{V_{CC(MAX)}} \times VF$$

(VF: Forward voltage of $I_{O1(MAX)}$)

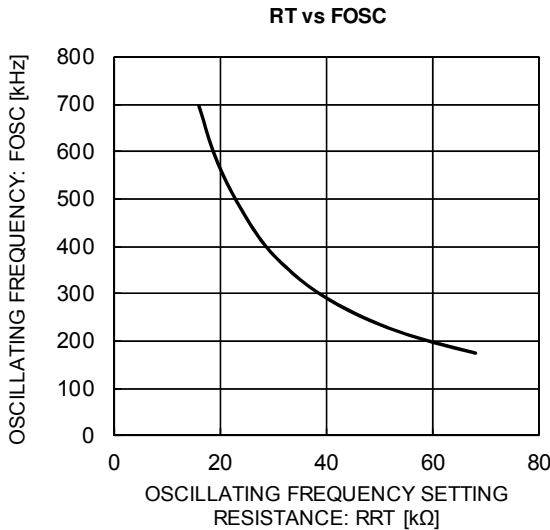
Selecting a diode that has low forward voltage and fast reverse recovery time will help achieve a high efficiency. Select a diode with 0.6 V or lower forward voltage. The use of the diode greater than 0.6 V forward voltage may cause inner element destruction so care has to be taken. The reverse recovery time of the schottky barrier diode is so short and thus its switching loss is ignorable. If the diode needs to withstand the event of output short-circuit, absolute maximum ratings and power dissipation need to be even higher. The maximum rated current needs to be approximately 1.5 times of the over current detection value. The diode power loss at the event of output short-circuit can be obtained by the following equation.

$$P_{Di(SHORT)} = I_{LIMIT(MAX)} \times VF$$

($I_{LIMIT(MAX)}$: V_{O1} Maximum over current protect operation current)

11. Setting the oscillation frequency (DC / DC1)

The internal oscillation frequency can be set by changing the resistance value connected to RT pin. Frequency can be set in the range of 250 kHz to 600 kHz. The following table shows the resistance value and its corresponding oscillation frequency. Switching may stop if the oscillation frequency is set outside of the recommended frequency range and thus normal operation is not guaranteed in such case.



RT [kΩ]	Fosc [kHz]
16	697
20	564
27	424
33	350
39	298
47	250
56	211
68	175

*The oscillation frequency graph is typical. A certain variation exists in actual usage.

Figure 34. RT resistance vs. oscillation frequency

12. Setting the phase compensation circuit (DC / DC1)

Circuit stability and transient response characteristics are determined by phase compensation. In order to get negative feedback stability, set phase lag when gain 1 (0 dB) equal to or less than 135° (greater than 45° phase margin). Good frequency response can be realized by setting higher zero crossing frequency f_c (frequency at 0 dB gain) of the total gain. However, speed and stability are in trade-off relationship. Moreover, DC / DC converter application is sampled by switching frequency and the gain of the switching frequency needs to be suppressed. In order to do so, zero crossing frequency needs to be set equal to or lower than 1 / 10 of the switching frequency.

To improve the responsiveness, switching frequency needs to be raised. It is recommended to draw a Bode plot using the transfer function of control loop in order to get a frequency response necessary. Please confirm the frequency characteristics of the total gain by combining the below three transfer functions.

$$G_{LC} = \frac{1 + \frac{s}{2\pi \times f_{ESR}}}{1 + \frac{s}{Q \times 2\pi \times f_{LC}} + \left(\frac{s}{2\pi \times f_{LC}}\right)^2} \quad \dots (a)$$

$$G_{FB1} = \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{Z2}}\right)}{s \times R_{FB1B} \times C_{CO1A} \times \left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \quad \dots (b)$$

$$G_{PWM} = \frac{V_{CC}}{\Delta V_{RAMP}} \quad \dots (c)$$

(G_{LC} : transfer function of LC resonance, G_{FB} : transfer function of phase compensation, G_{PWM} : transfer function of PWM, ΔV_{RAMP} : 0.4 V, Q : LC quality factor)

Since DC / DC1 is voltage mode, it is possible to add 2-pole and 2-zero compensation as follows. The frequency of zero and pole is determined by the following equations:

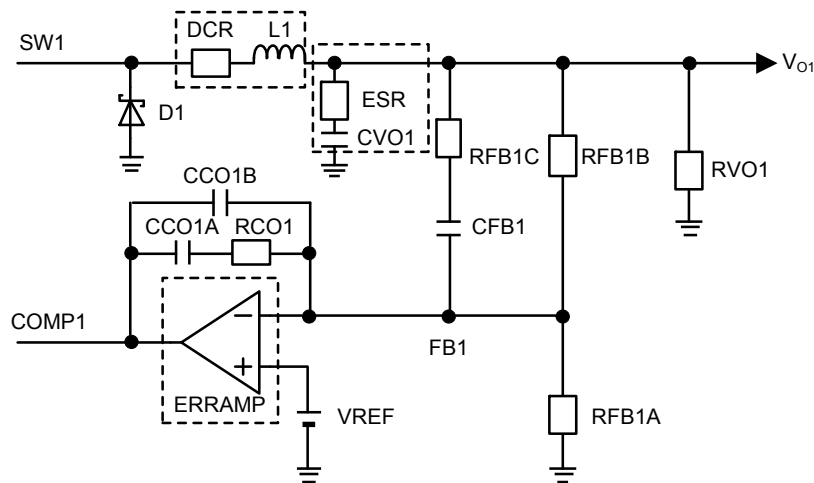


Figure 35. Phase compensation circuit (DC / DC1)

$$f_{LC} = \frac{1}{2\pi} \sqrt{\frac{R_{VO1} + DCR + R_{ON}}{L1 \times C_{VO1} (R_{VO1} + ESR)}} \quad \dots (d)$$

$$f_{ESR} = \frac{1}{2\pi \times ESR \times C_{VO1}} \quad \dots (e)$$

$$f_{Z1} = \frac{1}{2\pi \times R_{CO1} \times C_{CO1A}} \quad \dots (f)$$

$$f_{Z2} = \frac{1}{2\pi \times (R_{FB1B} + R_{FB1C}) \times C_{FB1}} \quad \dots (g)$$

$$f_{P1} = \frac{C_{CO1A} + C_{CO1B}}{2\pi \times R_{CO1} \times C_{CO1A} \times C_{CO1B}} \quad \dots (h)$$

$$f_{P2} = \frac{1}{2\pi \times R_{FB1C} \times C_{FB1}} \quad \dots (i)$$

(DCR: Inductor DC resistance, R_o: Load resistance, R_{ON}: MOS FET ON resistance)

The frequency characteristics are optimized by placing pole and zero at most appropriate frequencies. The estimate is as follows.

$$0.2 \times f_{LC} \leq f_{z1} \leq f_{LC} \quad \dots (j)$$

$$0.5 \times f_{LC} \leq f_{z2} \leq f_{LC} \times 2 \quad \dots (k)$$

$$f_{P1} \approx f_C \times 5 = f_{SW} \times 0.5 \quad \dots (l)$$

$$f_{P2} \approx f_{ESR} \quad \dots (m)$$

The phase compensation set as explained can cancel out the second order lag (-180 °) caused by LC resonance. If f_{ESR} is positioned higher than DC / DC switching frequency such as using low ESR ceramic for output cap, f_{P2} is not necessary.

If LC filter Q (quality factor) is high, the gain has peak and phase rotates too fast resulting in not enough phase margin. In such case, set f_{z1} and f_{z2} as close to f_{LC} as possible. Q (quality factor) is calculated by following equation:

$$Q = \frac{\sqrt{L1 \times C_{VO1} \times R_{VO1} (R_{VO1} + ESR)}}{L1 + C_{VO1} \times R_{VO1} \times ESR} \quad \dots (n)$$

$$\approx R_{VO1} \times \sqrt{\frac{C_{VO1}}{L1}} \quad \dots (o)$$

The way to start designing phase compensation circuit is as explained. Create a Bode plot and check if targeted frequency characteristics are met. The frequency characteristics pretty much fluctuate depending on PCB layout, type of components used and operating conditions. For instance, using electrolytic capacitor for output stability may cause the shift of LC resonance resulting in oscillation due to the capacitance drop at low temp and relevant ESR increase. For phase compensation, temperature compensating type capacitor is recommended. Make sure to check stability and responsiveness in actual product.

Frequency characteristics are checked by gain phase analyzer or FRA. Ask each vendor for measurement method. Even if such measurement equipment is unavailable, phase margin can be estimated from transient load response. Monitor how the output waveform fluctuates when changing from no load to maximum load. If the output fluctuation is significant, response time is slow. If the ringing is frequent, phase margin is not enough. Twice or less ringing is appropriate. The phase margin however cannot be quantified in this check method.

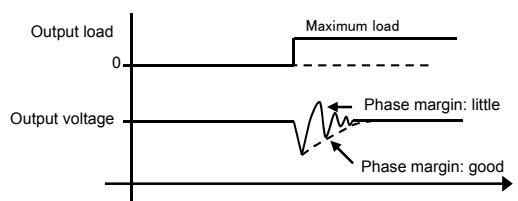
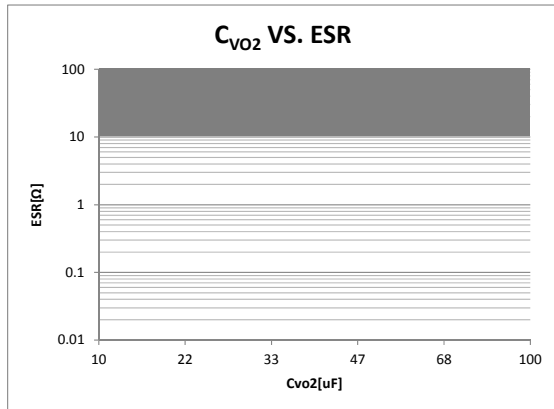


Figure 36. Load response

13. Phase compensation circuit (LDO)

VO2 pin capacitor

The capacitor must be added between VO2 pin and GND in order to prevent it from oscillating and the recommended Capacitance value is more than 10uF. In accordance to the graph shown below, either Electrolytic or Ceramic Capacitor can be used. Please ensure to select a Capacitor higher than 10uF in the range of voltage and temperature to be used at. There is a possibility of oscillation when capacitance value changes due to change of temperature. When selecting a ceramic capacitor, X7R or higher is recommended which is good in temperature characteristic and has excellent DC bias characteristic. In case significant voltage swing and load transient are expected, make sure to carry out a thorough evaluation before making a decision on the capacitance value.



Condition
 $V_{CC} = 12\text{ V}$, $V_{S2} = 6.5\text{ V}$, $0\text{ mA} \leq I_{O2} \leq 600\text{ mA}$,
 $10\text{ }\mu\text{F} \leq C_{VO2} \leq 100\text{ }\mu\text{F}$

Figure 37. Output capacitor value C_{VO2} vs Output capacitor ESR

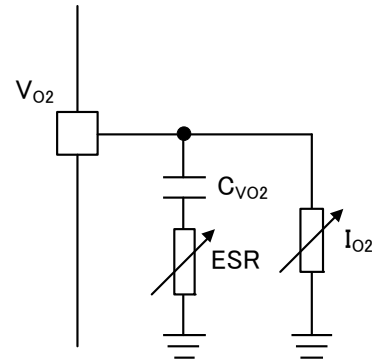


Figure 38. Output capacitor and ESR measurement circuit

14. Provision of Capacitor connected to CL terminal

The capacitor (CCL) and resistor (RCLB) connected to CL pin are the CR noise filter for preventing OCP error detection.

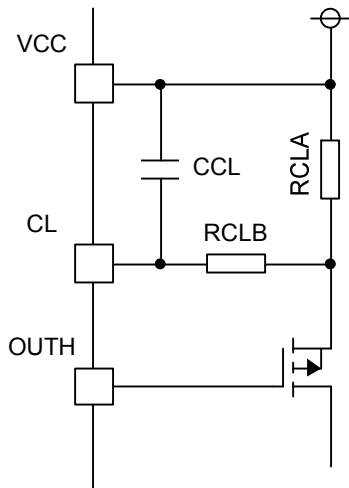


Figure 39. CL pin filter circuit

For the constant setting of filter, since noise depends on circuit and board pattern, there is no fixed rule. But, please try reducing cut-off frequency of CR filter without deteriorating ON pulse waveform that requires detecting current sense.

Pulse width $\approx (VO1 / VCC) \cdot (1 / FOSC)$
 (The rough estimate setting is $RCLB = \text{several tens } \Omega$, $CCL = \text{several thousand pF}$)

15. Soft Start setting

The soft start function is necessary to prevent inrush coil current and output voltage overshoot at start up. Setting of soft start time is shown in the following equation.

• DC / DC1

$$T_{SS1} = \frac{V_{SS0} \times C_{SS1}}{I_{SS0}} + \frac{V_{REF08} \times C_{SS1}}{I_{SS1}}$$

16. Setting the CT power on reset time

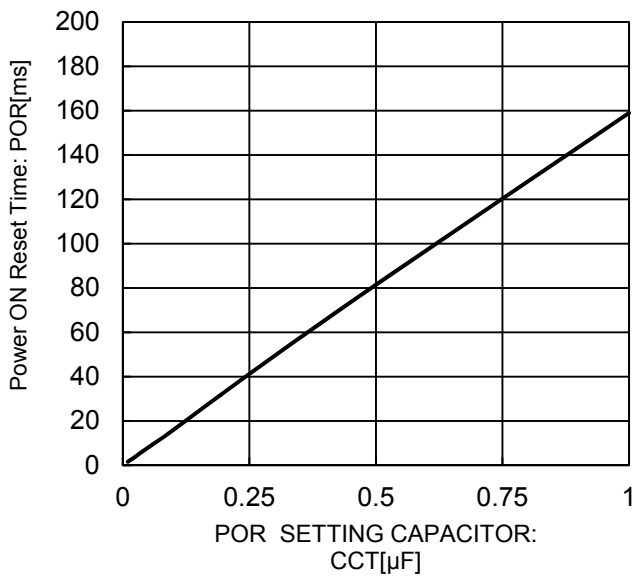
Power reset setting time can be set by the capacitor connected to CT. Capacitance can be chosen from 0.01 μF to 1 μF range or have CT terminal OPEN.

If setting is made out of its range, chattering may occur at Reset output.

CT operation is changed by the time of error detection. See page 13, Figure 19 for detail.

(1) CT pin starts 0 V

CT vs POR

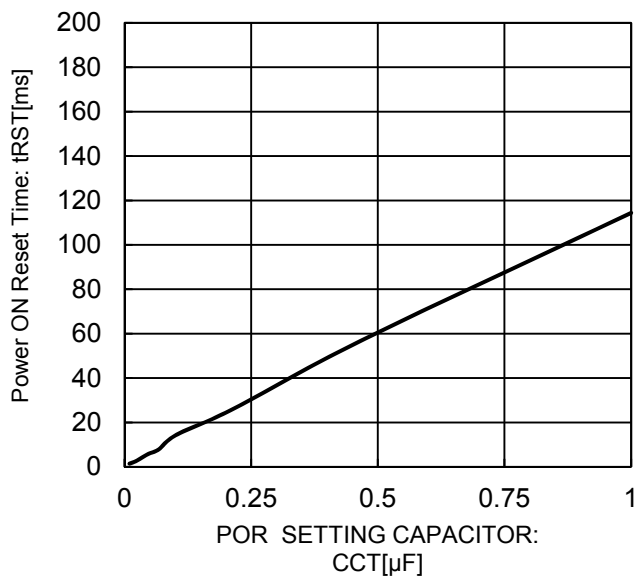


CT [μF]	POR [ms]
0.001	0.167
0.0082	1.09
0.01	1.62
0.022	3.46
0.033	5.24
0.047	7.64
0.068	10.8
0.1	16
0.22	36.2
0.47	76.8
1	159

Figure 40. Power ON Reset time1 (CT = 0 V to 0.8 V(Typ))

(2) CT pin starts 0.2 V

CT vs tRST



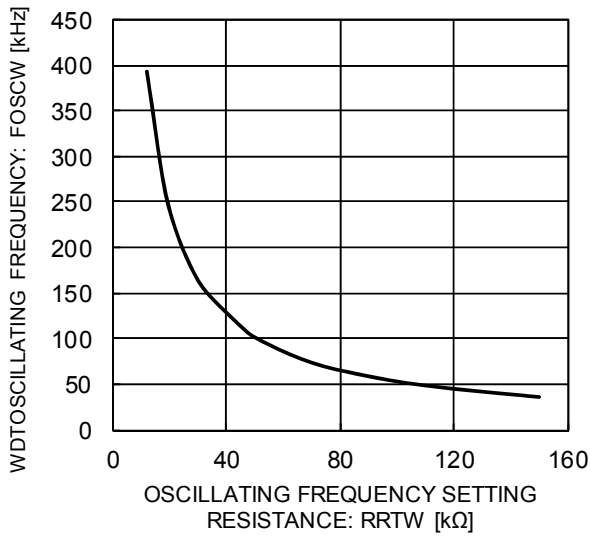
CT [μF]	POR [ms]
0.001	0.16
0.0082	0.826
0.01	1.452
0.022	2.51
0.033	3.93
0.047	5.82
0.068	7.9
0.1	14.12
0.22	26.7
0.47	57.2
1	114.4

Figure 41. Power ON Reset time2 (CT = 0.2 V (Typ) to 0.8 V(Typ))

17. WDT oscillation frequency

WDT oscillation frequency can be set by a resistance value connected to RTW. Possible setting range is 50 kHz to 250 kHz and the relation between resistance value and oscillation frequency is decided as shown below. It is possible that the switching stops at outside these range and its operation is not guaranteed.

RTW vs FOSC

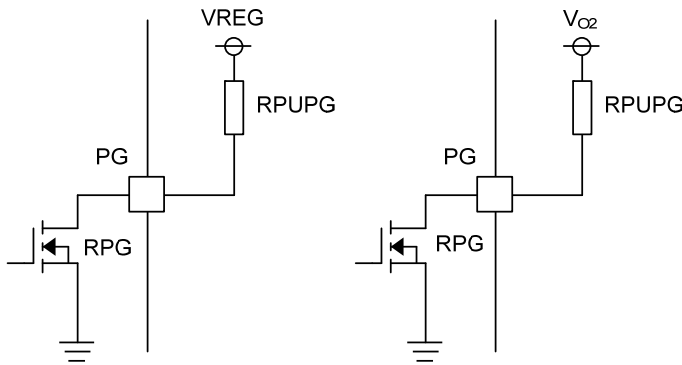


R _{TW} [kΩ]	F _{OSC} [kHz]
18	268
22	221
27	182
33	151
47	108
51	100
62	83
75	69
82	64
100	53
120	45

*This oscillation frequency graph is typical value
Tolerance needs to be put into consideration.

Figure 42. WDT oscillation frequency characteristics

18. Recommend value of external pull - up resistance



PG pin ON resistance (PPUPG)
 Min = 0.5 kΩ, Typ = 1.0 kΩ, Max = 2.0 kΩ

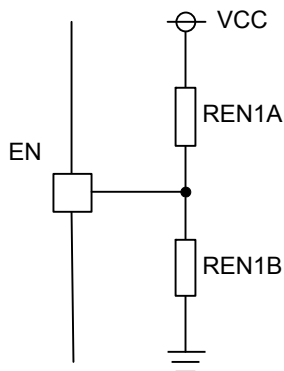
$$\frac{R_{PG}}{R_{PG} + R_{PUPG}} \times V_{O2} > V_{PG} \quad (V)$$

Please set the Resistance value considering H threshold of PG pin.

Figure 43. External pull - up resistance

19. Provision of EN1 pull -up resistance

Because "H" threshold of EN1 is Min 2.5 V, please design as the below equation is able to work.



$$\frac{R_{EN1B}}{R_{EN1B} + R_{EN1A}} \times V_{CC} > 2.5 \quad (V)$$

$$(188 \text{ k}\Omega \leq R_{EN1B} \leq 750 \text{ k}\Omega)$$

Figure 44. EN1 pull -up resistance

Application Examples

- *There are many factors (Board layout, variation of the part, etc.) that can affect the characteristics. Please verify and confirm using practical applications.
- *No connection (N.C) pin should not be connected to any other lines.
- *Be sure to connect the TEST pin to ground.
- * If EN1 pin is connected to VCC pin, please insert resistance between the pins.

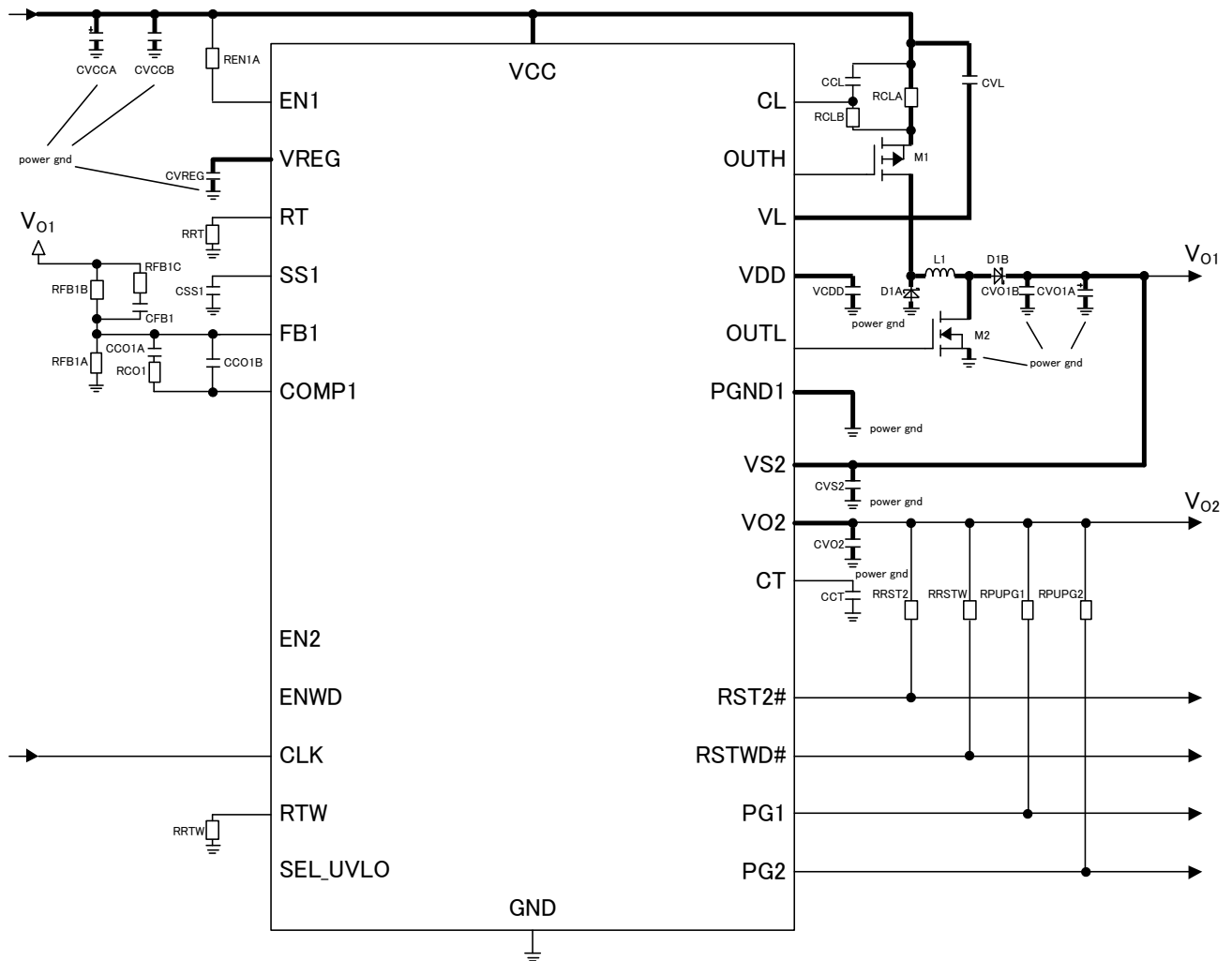


Figure 45. Application Example 2 (Buck - Boost)

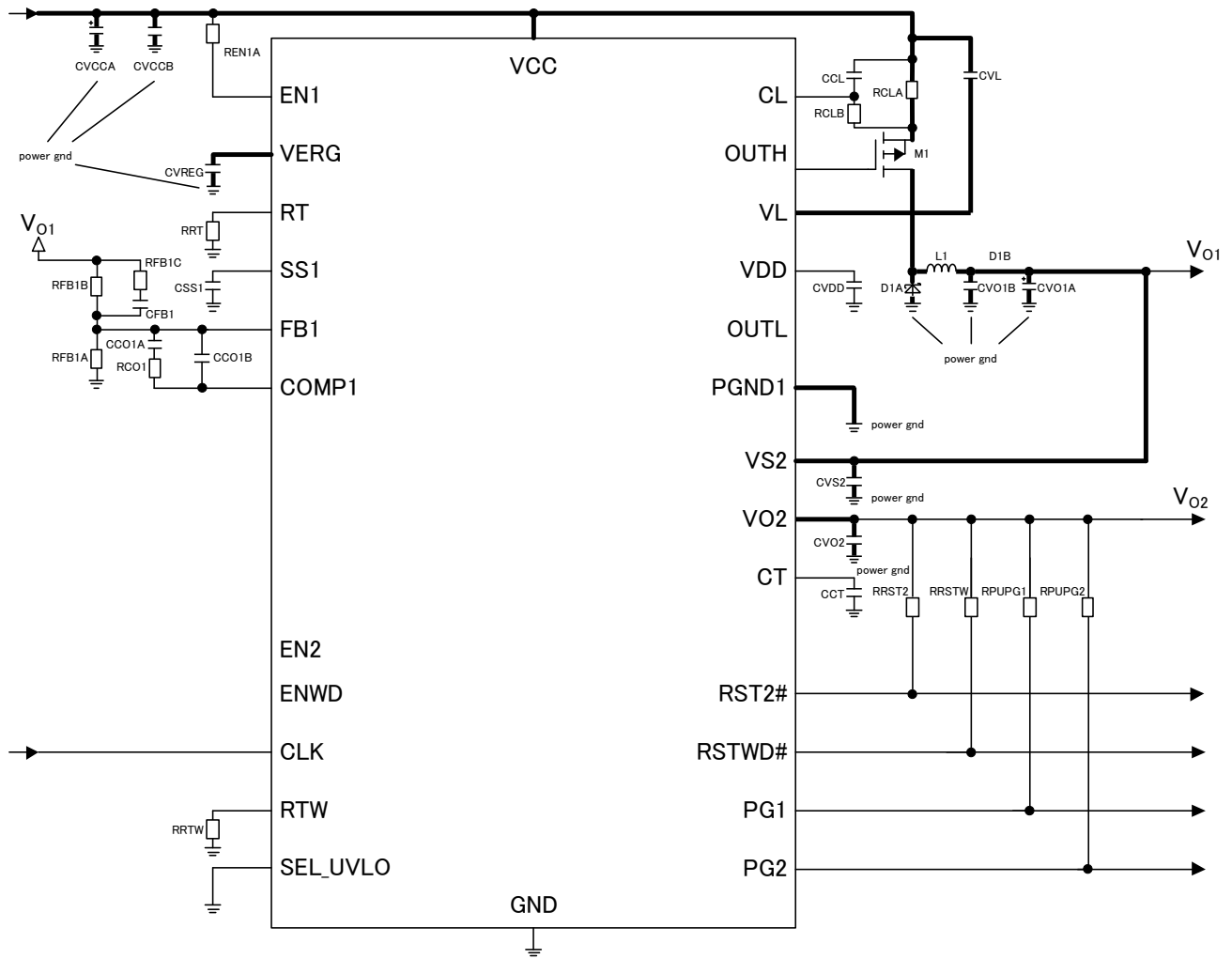


Figure 46. Application Example 3 (Buck - mode)

Example of Constant Setting (DC / DC1 Buck - Boost)

Name	Value		Parts No.	Size Code	Maker	Note
IC	-	-	BD39002EFV-C	10.00 × 7.60 × 1.00 mm	ROHM	
REN	150	kΩ	MCR03	1608	ROHM	
RRT	27	kΩ	MCR03	1608	ROHM	
RFB1A	10	kΩ	MCR03	1608	ROHM	
RFB1B	68	kΩ	MCR03	1608	ROHM	
RFB1C	0.1	kΩ	MCR03	1608	ROHM	At Buck - mode: 1.6 kΩ
RCO1	4.7	kΩ	MCR03	1608	ROHM	At Buck - mode: 36 kΩ
RRTW	47	kΩ	MCR03	1608	ROHM	
RCLA	110	mΩ	MCR10	2012	ROHM	
RCLB	110	mΩ	MCR10	2012	ROHM	
RRST2	10	kΩ	MCR03	1608	ROHM	
RRST3	10	kΩ	MCR03	1608	ROHM	
RRSTW	10	kΩ	MCR03	1608	ROHM	
RPUPG1	10	kΩ	MCR03	1608	ROHM	
RPUPG2	10	kΩ	MCR03	1608	ROHM	
RPUPG3	10	kΩ	MCR03	1608	ROHM	
CVCCA	47	μF	Electrolytic capacitor	-	-	
CVCCB	2.2	μF	GCM31CR71H225KA40	1608	murata	
CVREG	1	μF	GCM188R71C105KA49	1608	murata	
CVDD	1	μF	GCM188R11H104KA42	1608	murata	At Buck - mode: 0.1 μF
CSS1	0.033	μF	GCM188R11H333KA40	1608	murata	
CCO1A	47000	pF	GCM188R11H222KA01	1608	murata	At Buck - mode: 2200 pF
CCO1B	100	pF	GCM188R11H330KA01	1608	murata	At Buck - mode: 33 pF
CVS2	1	μF	GCM188R71C105KA49	1608	murata	
CCL	0.1	μF	GCM188R11H104KA42	1608	murata	
CVL	0.1	μF	GCM188R11H104KA42	1608	murata	
CVO1A	47	μF	Electrolytic capacitor			At Buck - mode: 100 μF
CVO1B	44	μF	GCM32ER71C226KE15	3225	murata	At Buck - mode: OPEN
CVO2	10	μF	GCM31CR71C106KA49	3216	murata	
CCT	0.1	μF	GCM188R11H104KA42	1608	murata	
L1	47	μH	SLF12565T-470M2R4-H	12.5 × 12.5 × 6.5mm	TDK	
D1A	SBD		RB050L-40	2.6 × 5.0 × 2 mm	ROHM	
D1B	SBD		RB050L-40	2.6 × 5.0 × 2 mm	ROHM	At Buck - mode: SHORT
M1	pchFET		RSD046P05	6.5 × 9.5 × 2.3 mm	ROHM	
M2	nchFET		RSD080N06	6.5 × 9.5 × 2.3 mm	ROHM	At Buck - mode: OPEN

Notes for pattern layout of PCB

- 1) Design the wirings shown in bold line as short as possible.
- 2) Place the input ceramic capacitor CVCCB as close to M1 as possible.
- 3) Place the RRT and RRTW as close to GND pin as possible.
- 4) Place the RFB1A and RFB1B as close to FB1 pin as possible and provide the shortest wiring from FB1 pin.
- 5) Place the RFB1A and RFB1B as far away from L1 as possible.
- 6) Separate power GND and signal GND so that SW noise doesn't affect the signal GND.

Power Dissipation

Maximum Junction Temperature Tj is 150 °C. If the junction temperature reaches 175 °C or higher, the circuit will shut down. Please make sure that the junction temperature must not exceed 150C at all time.

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. Ambient temperature Ta is less than 125 °C.
2. Tj is less than 150 °C.

Temperature Tj can be calculated by two ways as below.

1. To obtain Tj from the IC surface temperature Tc in actual use
2. To obtain Tj from the ambient temperature Ta

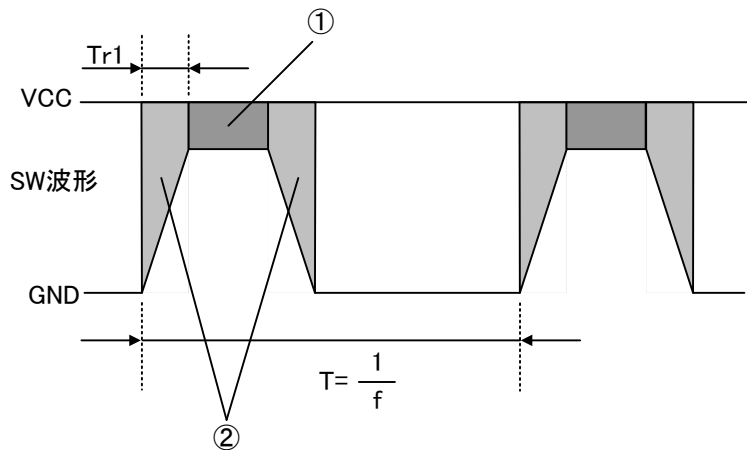
$$Tj = Tc + \theta_{jc} \times P_{TOTAL} \qquad Tj = Ta + \theta_{ja} \times P_{TOTAL}$$

The heat loss of the IC (P_{TOTAL}) is calculated by the equation below.

$$P_{TOTAL} = P_1 + P_2 + P_3$$

• DC / DC1 (at Buck)

$$P_1 = R_{onH1} \times I_{O1}^2 \times \frac{V_{O1}}{V_{CC}} + V_{CC} \times I_{CC} + Tr_1 \times V_{CC} \times I_{O1} \times \frac{f}{2} + Tf_1 \times V_{CC} \times I_{O1} \times \frac{f}{2}$$



$$\begin{aligned} \textcircled{1} & R_{onH1} \times I_{O2} \times \frac{V_{O1}}{V_{CC}} \\ \textcircled{2} & \frac{1}{2} \times (Tr_1 + Tf_1) \times \frac{1}{T} \times V_{CC} \times I_{O1} \\ & = Tr_1 \times V_{CC} \times I_{O1} \times \frac{f}{2} \\ & \quad + Tf_1 \times V_{CC} \times I_{O1} \times \frac{f}{2} \end{aligned}$$

Figure 47. SW1 Wave form

• LDO

$$P_2 = (VS_2 - VO_2) \times IO_2 + VS_2 \times ICC_2$$

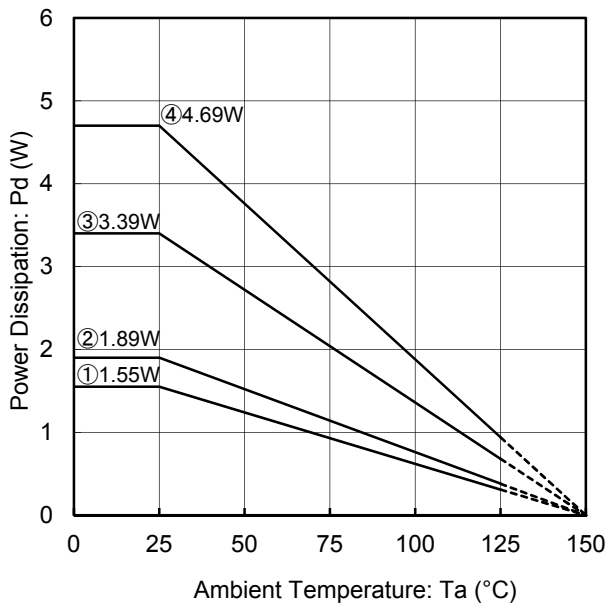
RONH1: ON resistance of external Pch-PowTr, VO1: DC / DC1 output voltage, VO2: LDO output voltage, VCC: Input voltage (VS2 = VO1), IO1: DC / DC1 output current, IO2: LDO output current

- ICC: circuit current (see page 5)
- Tr1: Switching rise time (About 15 ns)
- Tf1: Switching fall time (About 35 ns)
- f: Oscillation frequency

See the thermal derating characteristics (Figure 48) if the device used over the ambient temperature Ta = 25 °C. The characteristics of IC largely depend on temperature, and the IC must be used at maximum junction temperature (Tjmax) or lower. Even if the ambient temperature is 25 °C, there is a possibility junction temperature gets high as consequence of input voltage and load current. The IC must be used within power dissipation Pd.

Thermal resistance value θja is varied by the number of layers and copper foil area of the PCB. See Figure 48 for the thermal design.

Thermal Derating Characteristics



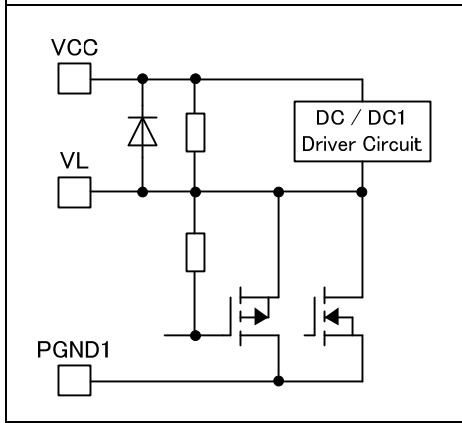
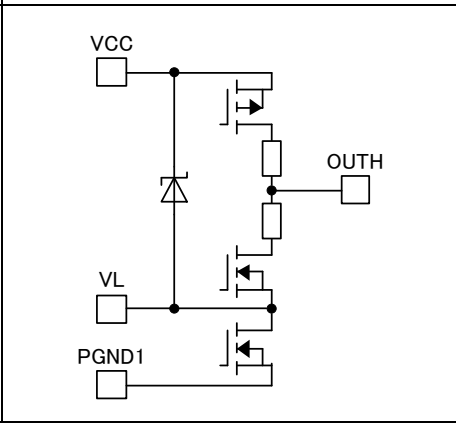
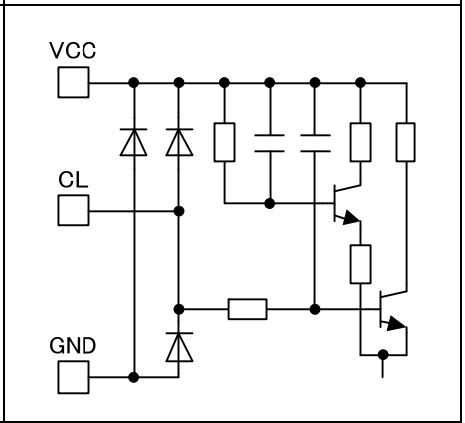
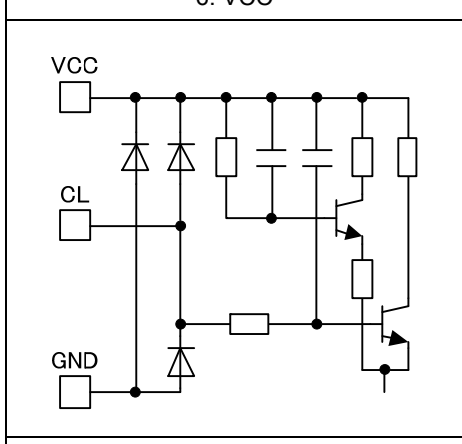
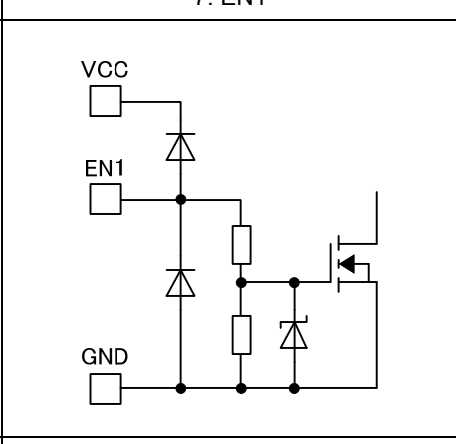
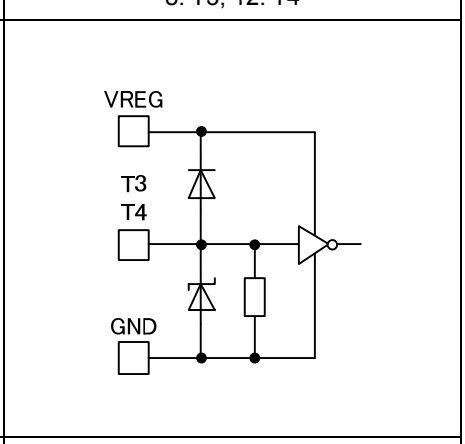
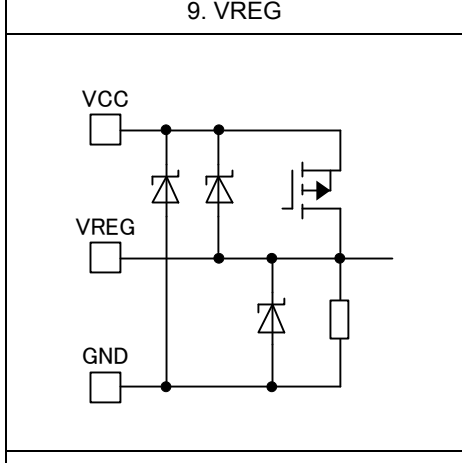
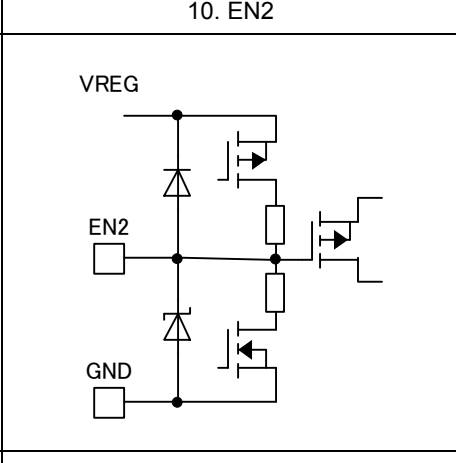
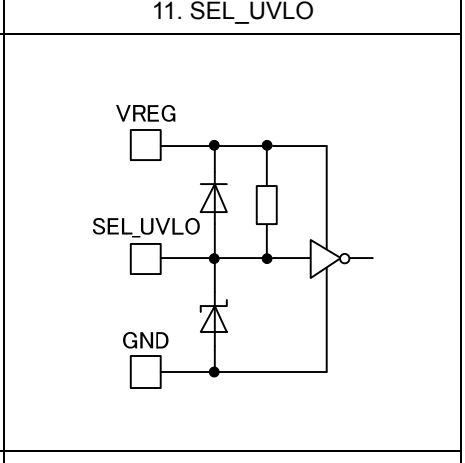
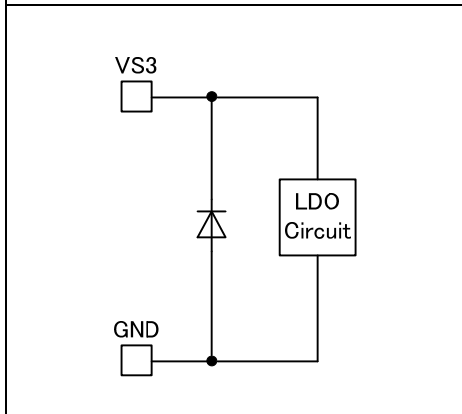
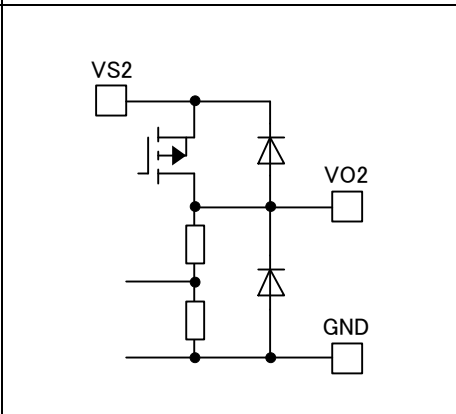
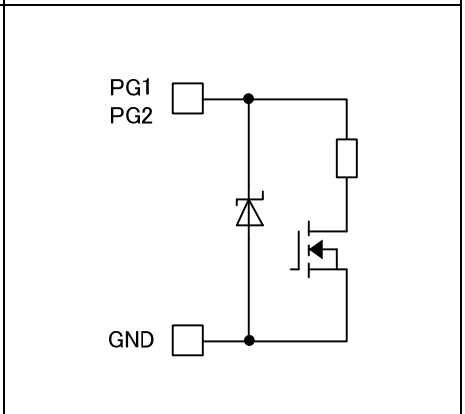
IC mounted on ROHM standard board
 • Board size: 70 mm × 70 mm × 1.6 mm
 • PCB and back metal are connected by soldering

- ① 1 layer board 70 × 70 × 1.6 mm (copper foil area 0 mm × 0 mm)
- ② 2 layer board 70 × 70 × 1.6 mm (copper foil 15 mm × 15 mm)
- ③ 2 layer board 70 × 70 × 1.6 mm (copper foil 70 mm × 70 mm)
- ④ 4 layer board 70 × 70 × 1.6 mm (copper foil 70 mm × 70 mm)

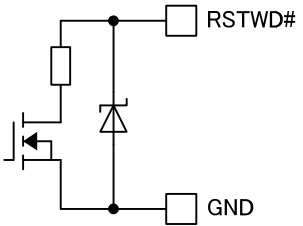
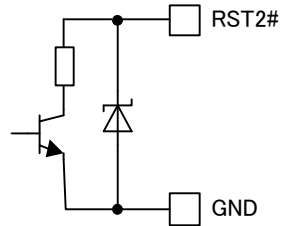
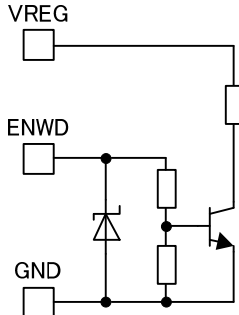
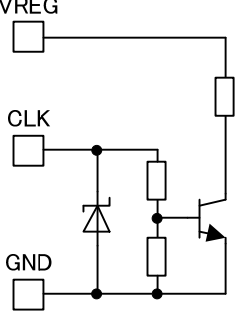
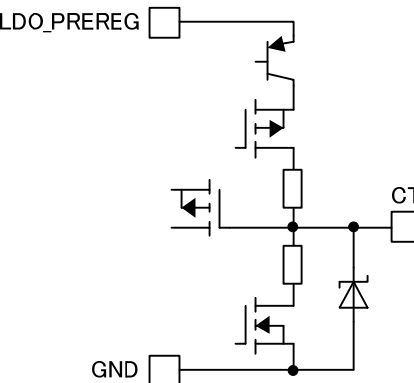
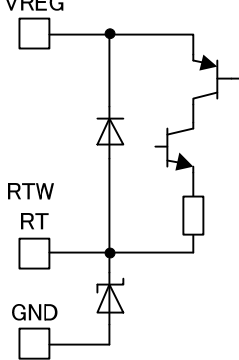
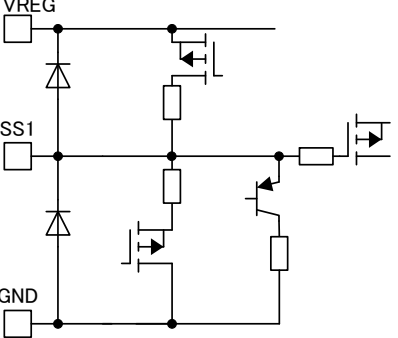
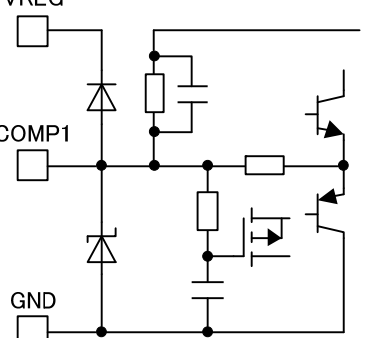
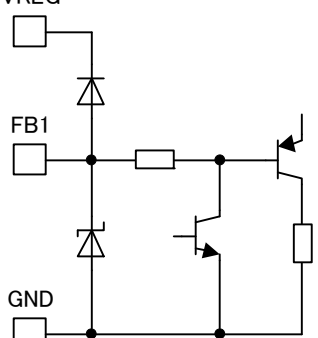
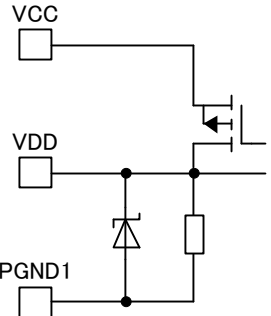
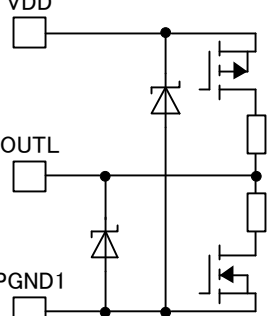
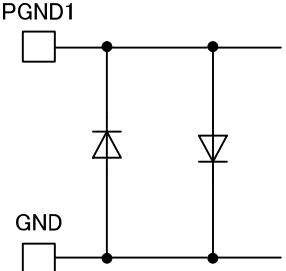
Board①: $\theta_{ja} = 80.6 \text{ }^\circ\text{C} / \text{W}$
 Board②: $\theta_{ja} = 65.8 \text{ }^\circ\text{C} / \text{W}$
 Board③: $\theta_{ja} = 36.8 \text{ }^\circ\text{C} / \text{W}$
 Board④: $\theta_{ja} = 26.6 \text{ }^\circ\text{C} / \text{W}$

Figure 48. Package data of HTSSOP-B30 (Reference data)

I / O Equivalence Circuit

<p>1. VL</p> 	<p>3. OUTH</p> 	<p>5. CL</p> 
<p>6. VCC</p> 	<p>7. EN1</p> 	<p>8. T3, 12. T4</p> 
<p>9. VREG</p> 	<p>10. EN2</p> 	<p>11. SEL_UVLO</p> 
<p>13. VS2</p> 	<p>14. VO2</p> 	<p>15. PG2, 16. PG1</p> 

I / O Equivalence Circuit - Continuance

<p>17. RSTWD#</p> 	<p>18. RST2#</p> 	<p>19. ENWD</p> 
<p>20. CLK</p> 	<p>21. CT</p> 	<p>22. RTW, 23. RT</p> 
<p>25. SS1</p> 	<p>26. COMP1</p> 	<p>27. FB1</p> 
<p>28. VDD</p> 	<p>29. OUTL</p> 	<p>30. PGND1</p> 

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Please make sure to have protection against reverse polarity, such as putting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Power supply line must be low impedance on the PCB. The power supply of digital and analog must be separated (even if the electrical potentials are the same) to prevent analog circuit from having digital noise by common impedance of line pattern (ground line must be designed in the same way)

Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that ground pin must have the lowest electrical potential at all time even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately, but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground voltage caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd is specified at the condition of 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size or copper area to prevent the IC from exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the specified characteristics can be approximately obtained. The electrical characteristics are guaranteed under the specified conditions.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To protect IC from static discharge damage, ground the IC during assembly and use similar precautions during transport and storage.

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Make sure that there is nothing between the pins, such as no metal particles, no water droplets (in very humid environment) and unintentional solder bridge deposited.

Operational Notes – continued

10. Unused Input Pins

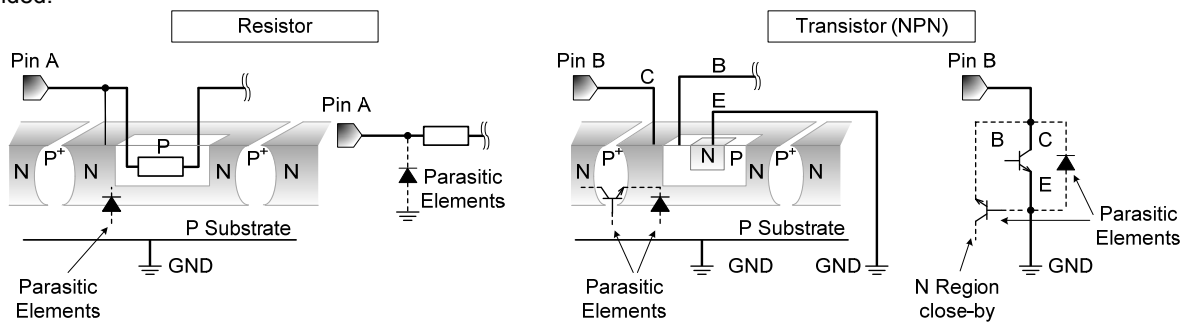
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If input pins left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.
When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant with the consideration of the capacitance change with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period of time, the junction temperature (T_j) rises, and TSD activated, which turns off all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings. Under no circumstances, TSD circuit should not be used for any purpose other than protecting the IC from exceeding the maximum rating.

14. Over Current Protection Circuit (OCP)

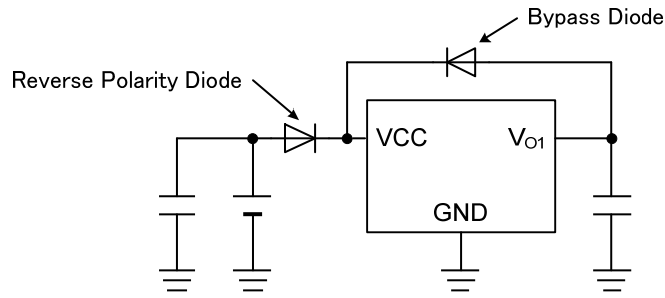
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is designed to avoid IC damaged from sudden and unexpected incidents, so should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

15. Power input at shutdown

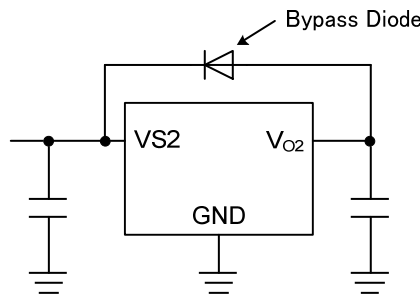
If VCC starts up in rapid period of time at shutdown (EN1 = OFF), VREG voltage may be output, which causes the IC to malfunction. Therefore, set the VCC rise time at 40V/ms or shorter.

16. Reverse Polarity and Surge voltage

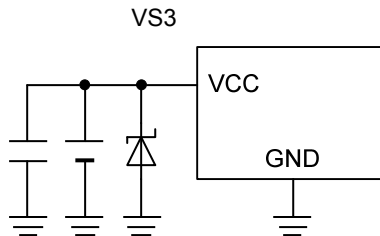
- If the VCC and pin potential are reversed, internal circuit or element may be damaged (example: VCC is shorted to GND while external capacitor charged) Putting diode for reverse protection in series of VCC or putting bypass diode between VCC is recommended.



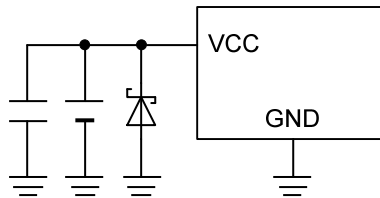
- If the VS2 and pin potential are reversed, internal circuit or element may be damaged (example: VCC is shorted to GND while external capacitor charged) Putting diode for reverse protection in series of VCC or putting bypass diode between VCC is recommended.



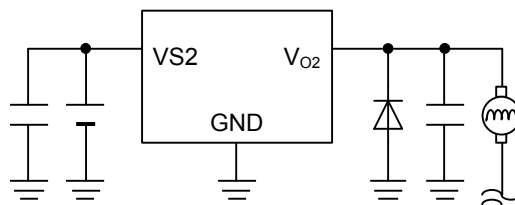
- Applying positive surge to the VCC
If there is a possibility of surge exceeding the rating applied to VCC, please put a power zener diode between VCC and GND.



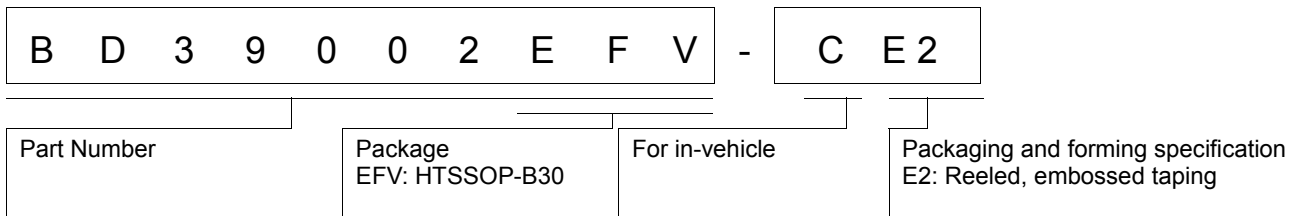
- Applying negative surge to the VCC
If there is a possibility that VCC gets lower than GND, please put a schottky diode between VCC and GND.



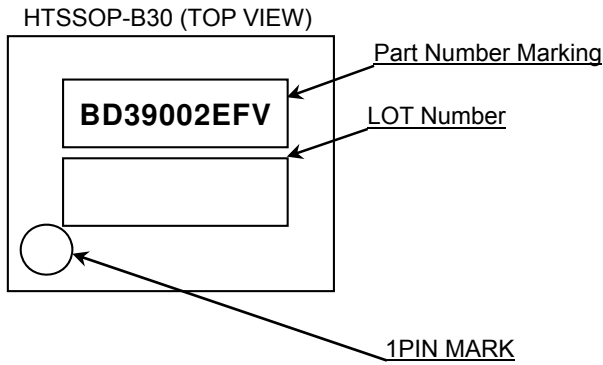
- Protection Diode
If there is a possibility of large inductive load is connected to the output pin (VO2) resulting in back-EMF at time of startup and shutdown, a protection diode should be placed as shown in the figure below.



Ordering Information

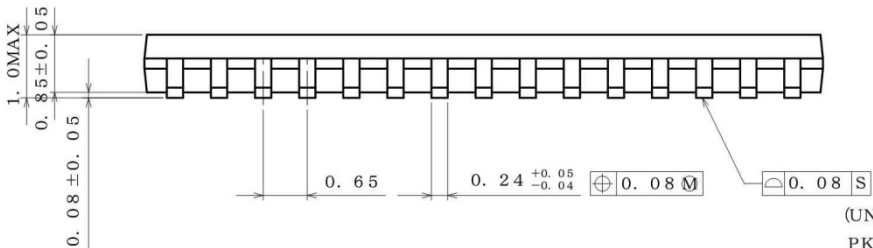
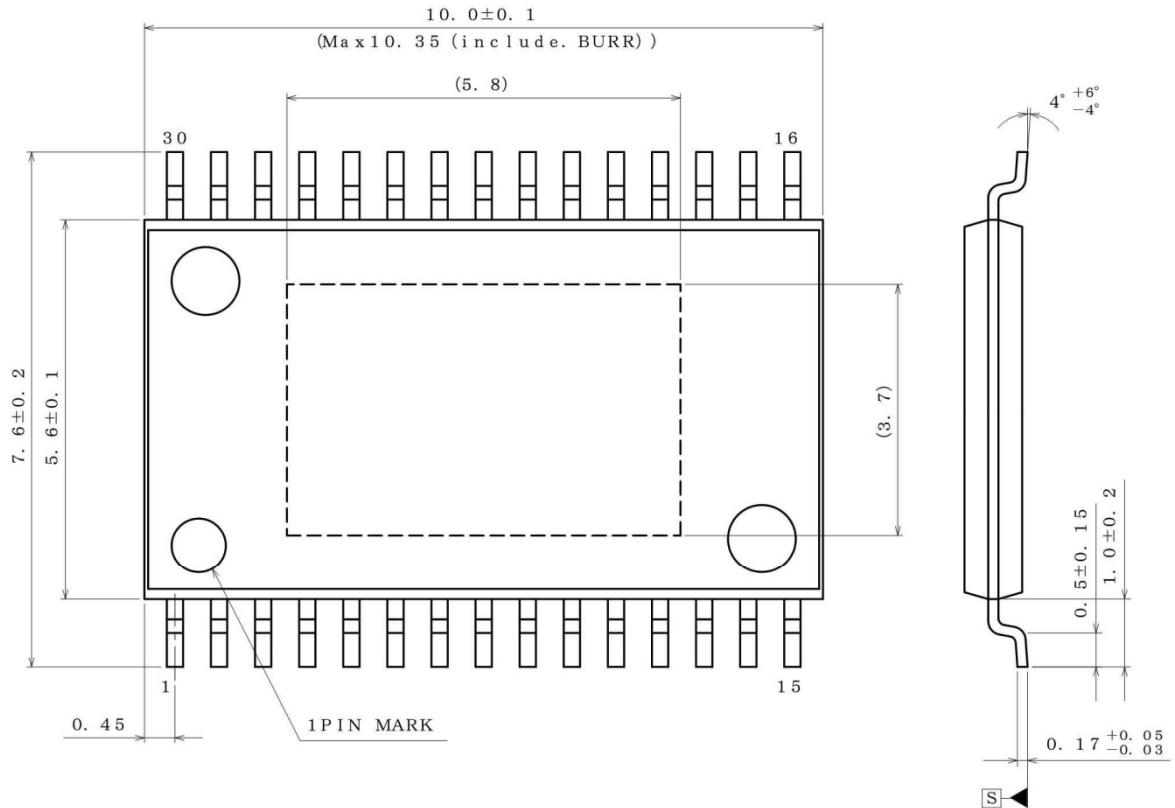


Marking Diagram



Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B30
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(UNIT : mm)
 PKG : HTSSOP-B30
 Drawing No. EX200-5002

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Reel

1pin

Direction of feed

* Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
2014.10.27	001	New release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
 - [a] Installation of protection circuits or other protective devices to improve system safety
 - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
 - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.
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