10-Bit, 210 MSPS ADC

AD9410

FEATURES

SNR = 54 dB with 99 MHz analog input
500 MHz analog bandwidth
On-chip reference and track and hold
1.5 V p-p differential analog input range
5.0 V and 3.3 V supply operation
3.3 V CMOS/TTL outputs
Power: 2.1 W typical at 210 MSPS
Demultiplexed outputs each at 105 MSPS
Output data format option
Data sync input and data clock output provided
Interleaved or parallel data output option

APPLICATIONS

Communications and radars
Local multipoint distribution services (LMDS)
High-end imaging systems and projectors
Cable reverse paths
Point-to-point radio links

FUNCTIONAL BLOCK DIAGRAM

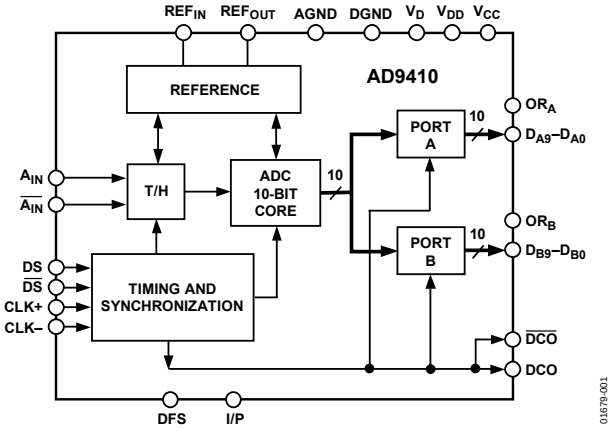

Figure 1.

GENERAL DESCRIPTION

The AD9410 is a 10-bit monolithic sampling analog-to-digital converter (ADC) with an on-chip track-and-hold circuit and is optimized for high speed conversion and ease of use. The product operates at a 210 MSPS conversion rate, with outstanding dynamic performance over its full operating range.

The ADC requires a 5.0 V and 3.3 V power supply and up to a 210 MHz differential clock input for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL-/CMOS-compatible and separate output power supply pins also support interfacing with 3.3 V logic.

The clock input is differential and TTL-/CMOS-compatible. The 10-bit digital outputs can be operated from 3.3 V (2.5 V to 3.6 V) supplies. Two output buses support demultiplexed data up to 105 MSPS rates and binary or twos complement output coding format is available. A data sync function is provided for timing-dependent applications. An output clock simplifies interfacing to external logic. The output data bus timing is selectable for parallel or interleaved mode, allowing for flexibility in latching output data.

Fabricated on an advanced BiCMOS process, the AD9410 is available in an 80-lead thin quad flat package, exposed pad specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. High Resolution at High Speed—The architecture is specifically designed to support conversion up to 210 MSPS with outstanding dynamic performance.
2. Demultiplexed Output—Output data is decimated by two and provided on two data ports for ease of data transport.
3. Output Data Clock—The AD9410 provides an output data clock synchronous with the output data, simplifying the timing between data and other logic.
4. Data Synchronization—A DS input is provided to allow for synchronization of two or more AD9410s in a system, or to synchronize data to a specific output port in a single AD9410 system.

Rev. A

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AD9410* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-297: Test Video A/D Converters Under Dynamic Conditions
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-835: Understanding High Speed ADC Testing and Evaluation

Data Sheet

- AD9410: 10-Bit, 210 MSPS ADC Data Sheet

TOOLS AND SIMULATIONS

- AD9410 IBIS Models

REFERENCE MATERIALS

Technical Articles

- Correlating High-Speed ADC Performance to Multicarrier 3G Requirements
- Designers Cast A Skeptical Eye On Mixed-Signal SOCs
- DNL and Some of its Effects on Converter Performance
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9410 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9410 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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10/00—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

V_{DD} = 3.3 V, V_D = 3.3 V, V_{CC} = 5.0 V; 2.5 V external reference; A_{IN} = −0.5 dBFS; clock input = 210 MSPS; T_A = 25°C; unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION				10		Bits
DC ACCURACY						
No Missing Codes	Full	IV		Guaranteed		
Differential Nonlinearity	25°C	I	−1.0	±0.5	+1.25	LSB
	Full	VI	−1.0		+1.5	LSB
Integral Nonlinearity	25°C	I	−2.5	±1.65	+2.5	LSB
	Full	VI	−3.0		+3.0	LSB
Gain Error	25°C	I	−6.0	0	+6.0	% FS
Gain Temperature Coefficient	Full	V		130		ppm/°C
ANALOG INPUT						
Input Voltage Range (With Respect to $\overline{A_{IN}}$)	Full	V		±768		mV p-p
Common-Mode Voltage	Full	V		3.0		V
Input Offset Voltage	25°C	I	−15	+3	+15	mV
	Full	VI	−20		+20	mV
Reference Voltage	Full	VI	2.4	2.5	2.6	V
Reference Temperature Coefficient	Full	V		50		ppm/°C
Input Resistance	Full	VI	610	875	1250	Ω
Input Capacitance	25°C	V		3		pF
Analog Bandwidth, Full Power	25°C	V		500		MHz
POWER SUPPLY						
Power Dissipation AC[1]	25°C	V		2.1		W
Power Dissipation DC[2]	Full	VI		2.0	2.4	W
I_{VCC}[2]	Full	VI		128	145	mA
I_{VD}[2]	Full	VI		401	480	mA
Power Supply Rejection Ratio, PSRR	25°C	I	−7.5	+0.5	+7.5	mV/V

[1] Clock input = 210 MSPS, A_{IN} = −0.5 dBFS, 10 MHz sine wave, I_{VDD} = 31 mA typical at C_{LOAD} = 5 pF.
[2] Clock input = 210 MSPS, A_{IN} = dc, outputs not switching.

SWITCHING SPECIFICATIONS

V_{DD} = 3.3 V, V_D = 3.3 V, V_{CC} = 5.0 V; 2.5 V external reference; A_{IN} = −0.5 dBFS; clock input = 210 MSPS; T_A = 25°C; unless otherwise noted.

Table 2.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	210			MSPS
Minimum Conversion Rate	Full	IV			100	MSPS
Clock Pulse Width High, t_{EH}	25°C	IV	1.2	2.4		ns
Clock Pulse Width Low, t_{EL}	25°C	IV	1.2	2.4		ns
Aperture Delay, t_A	25°C	V		1.0		ns
Aperture Uncertainty (Jitter)	25°C	V		0.65		ps rms
Output Valid Time, t_V	Full	VI	3.0			ns
Output Propagation Delay, t_{PD}	Full	VI			7.4	ns
Output Rise Time, t_R	25°C	V		1.8		ns
Output Fall Time, t_F	25°C	V		1.4		ns
CLKOUT Propagation Delay, t_{CPD}[1]	Full	VI	2.6	4.8	6.4	ns
Data to DCO Skew, (t_{PD} – t_{CPD})	Full	IV	0	1	2	ns
DS Setup Time, t_{SDS}	Full	IV	0.5			ns
DS Hold Time, t_{HDS}	Full	IV	0			ns
Interleaved Mode (A, B Latency)	Full	VI		A = 6, B = 6		Cycles
Parallel Mode (A, B Latency)	Full	VI		A = 7, B = 6		Cycles

[1] C_{LOAD} = 5 pF.

DIGITAL SPECIFICATIONS

V_{DD} = 3.3 V, V_D = 3.3 V, V_{CC} = 5.0 V; 2.5 V external reference; A_{IN} = −0.5 dBFS; clock input = 210 MSPS; T_A = 25°C; unless otherwise noted.

Table 3.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DIGITAL INPUTS						
DFS, Input Logic 1 Voltage	Full	IV	4			V
DFS, Input Logic 0 Voltage	Full	IV			1	V
DFS, Input Logic 1 Current	Full	V		50		µA
DFS, Input Logic 0 Current	Full	V		50		µA
I/P Input Logic 1 Current[1]	Full	V		400		µA
I/P Input Logic 0 Current[1]	Full	V		1		µA
CLK+, CLK– Differential Input Voltage	Full	IV	0.4			V
CLK+, CLK– Differential Input Resistance	Full	V		1.6		kΩ
CLK+, CLK– Common-Mode Input Voltage[2]	Full	V		1.5		V
DS, $\overline{DS}$ Differential Input Voltage	Full	IV	0.4			V
DS, $\overline{DS}$ Common-Mode Input Voltage	Full	V		1.5		V
Digital Input Pin Capacitance	25°C	V		3		pF
DIGITAL OUTPUTS						
Logic 1 Voltage (V_{DD} = 3.3 V)	Full	VI	V_{DD} – 0.05			V
Logic 0 Voltage (V_{DD} = 3.3 V)	Full	VI			0.05	V
Output Coding				Binary or Twos Complement		

[1] I/P pin Logic 1 = 5 V, Logic 0 = GND. It is recommended to use a series 2.5 kΩ (±10%) resistor to V_{DD} when setting to Logic 1 to limit input current.
[2] See Clock Input section.

AC SPECIFICATIONS

V_{DD} = 3.3 V, V_D = 3.3 V, V_{CC} = 5.0 V; 2.5 V external reference; A_{IN} = −0.5 dBFS; clock input = 210 MSPS; T_A = 25°C; unless otherwise noted.

Table 4.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Transient Response	25°C	V		2		ns
Overvoltage Recovery Time	25°C	V		2		ns
Signal-to-Noise Ratio, SNR (Without Harmonics)						
f_{IN} = 10.3 MHz	25°C	I	52.5	55		dB
f_{IN} = 82 MHz	25°C	I	52	54		dB
f_{IN} = 160 MHz	25°C	V		53		dB
Signal-to-Noise Ratio, SINAD (With Harmonics)						
f_{IN} = 10.3 MHz	25°C	I	51	54		dB
f_{IN} = 82 MHz	25°C	I	50	53		dB
f_{IN} = 160 MHz	25°C	V		52		dB
Effective Number of Bits, ENOB						
f_{IN} = 10.3 MHz	25°C	I	8.3	8.8		Bits
f_{IN} = 82 MHz	25°C	I	8.1	8.6		Bits
f_{IN} = 160 MHz	25°C	V		8.4		Bits
Second Harmonic Distortion						
f_{IN} = 10.3 MHz	25°C	I	−56	−65		dBc
f_{IN} = 82 MHz	25°C	I	−55	−63		dBc
f_{IN} = 160 MHz	25°C	V		−65		dBc
Third Harmonic Distortion						
f_{IN} = 10.3 MHz	25°C	I	−58	−69		dBc
f_{IN} = 82 MHz	25°C	I	−57	−67		dBc
f_{IN} = 160 MHz	25°C	V		−62		dBc
Spurious-Free Dynamic Range, SFDR						
f_{IN} = 10.3 MHz	25°C	I	56	61		dBc
f_{IN} = 82 MHz	25°C	I	54	60		dBc
f_{IN} = 160 MHz	25°C	V		58		dBc
Two-Tone Intermod Distortion, IMD[1]						
f_{IN1} = 80.3 MHz, f_{IN2} = 81.3 MHz	25°C	V		58		dBFS

[1] IN1, IN2 level = −7 dBFS.

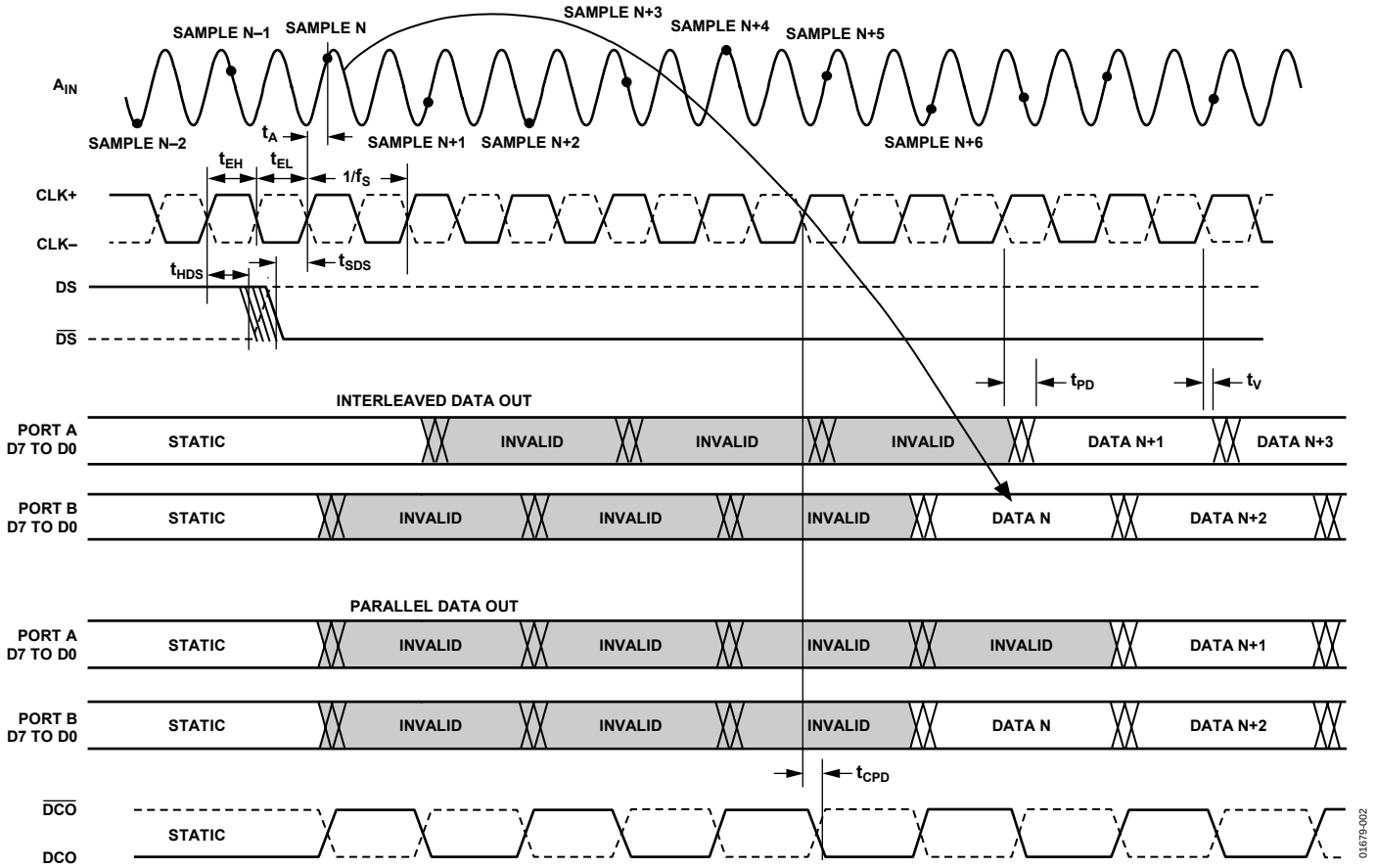

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_D, V_{CC}, V_{DD}	6 V
Analog Inputs	0 V to V_{CC} + 0.5 V
Digital Inputs	0 V to V_{DD} + 0.5 V
$VREF_{IN}$	0 V to V_D + 0.5 V
Digital Output Current	20 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature[1]	150°C

[1] Adequate dissipation of power from the AD9410 relies on all power and ground pins of the device being soldered directly to a copper plane on a PCB. In addition, the thermally enhanced package of the AD9410BSVZ has an exposed paddle on the bottom that must be soldered to a large copper plane, which, for convenience, can be the ground plane. Sockets for package style of the AD9410 device are not recommended.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLAINATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

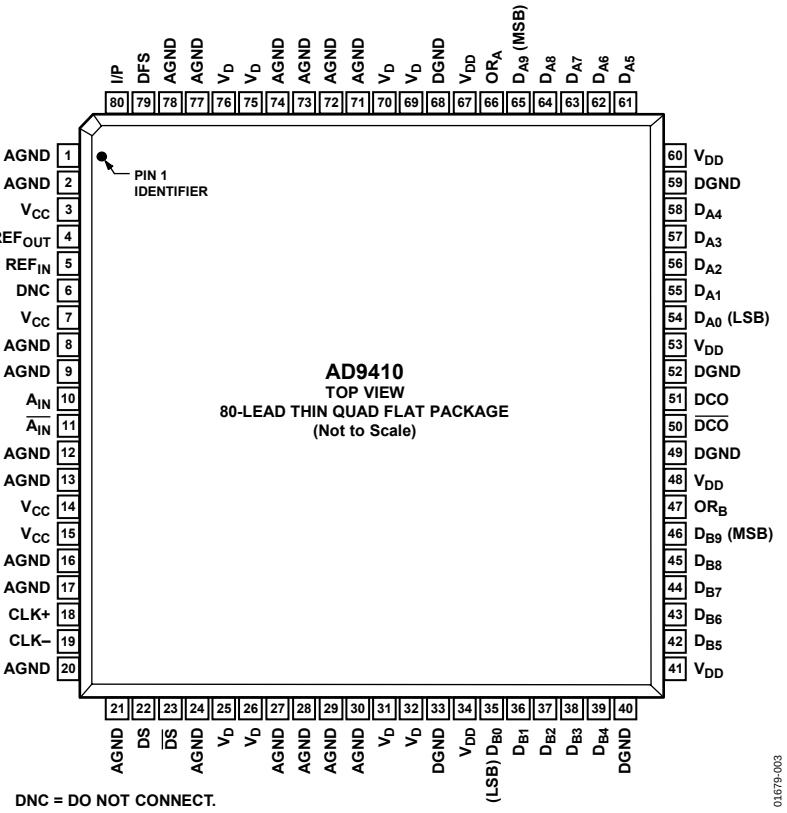

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2, 8, 9, 12, 13, 16, 17, 20, 21, 24, 27, 28, 29, 30, 71, 72, 73, 74, 77, 78	AGND	Analog Ground.
3, 7, 14, 15	V_{CC}	5 V Supply. (Regulate to within ±5%.)
4	REF_{OUT}	Internal Reference Output.
5	REF_{IN}	Internal Reference Input.
6	DNC	Do Not Connect.
10	A_{IN}	Analog Input—True.
11	$\overline{A_{IN}}$	Analog Input—Complement.
18	CLK+	Clock Input—True.
19	CLK–	Clock Input—Complement.
22	DS	Data Sync (Input)—True. Tie low if not used.
23	$\overline{DS}$	Data Sync (Input)—Complement. Float and decouple with 0.1 µF capacitor if not used.
25, 26, 31, 32, 69, 70, 75, 76	V_D	3.3 V Analog Supply. (Regulate to within ±5%.)
33, 40, 49, 52, 59, 68	DGND	Digital Ground.
34, 41, 48, 53, 60, 67	V_{DD}	3.3 V Digital Output Supply. (2.5 V to 3.6 V)
35 to 39	D_{B0} to D_{B4}	Digital Data Output for Channel B. (LSB = D_{B0}.)
42 to 46	D_{B5} to D_{B9}	Digital Data Output for Channel B. (MSB = D_{B9}.)
47	OR_B	Data Overrange for Channel B.
50	$\overline{DCO}$	Clock Output—Complement.

Pin No.	Mnemonic	Function
51	DCO	Clock Output—True.
54 to 58	D_{A0} to D_{A4}	Digital Data Output for Channel A (LSB = D_{A0}).
61 to 65	D_{A5} to D_{A9}	Digital Data Output for Channel A (MSB = D_{A9}).
66	OR_A	Data Overrange for Channel A.
79	DFS	Data Format Select. High = twos complement, and low = binary.
80	I/P	Interleaved or Parallel Output Mode. Low = parallel mode, and high = interleaved mode. If tying high, use a current limiting series resistor (2.5 kΩ) to the 5 V supply.

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the clock command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180° and taking the peak measurement again. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)
ENOB is calculated from the measured SINAD based on the equation

$$ENOB = \frac{SINAD_{MEASURED} - 1.76\,dB + 20\log\left(\frac{Full\ Scale\ Amplitude}{Input\ Amplitude}\right)}{6.02}$$

Clock Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the clock pulse should be left in Logic 1 state to achieve rated performance; pulse width low is the minimum time the clock pulse should be left in low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Full-Scale Input Power
Expressed in dBm. Computed using the equation

$$POWER_{FULLSCALE} = 10\log\left[\frac{V^2{}_{FULLSCALE_{rms}}}{\frac{|Z|_{INPUT}}{0.001}}\right]$$

Harmonic Distortion, Second
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least-square curve fit.

Minimum Conversion Rate
The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The clock rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of CLK+ and CLK− and the time when all output data bits are within valid logic levels.

Out-of-Range Recovery Time
Out-of-range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Noise (For Any Range Within the ADC)

$$V_{NOISE} = \sqrt{|Z| \times 0.001 \times 10\left(\frac{FS_{dBm} - SIGNAL_{dBFS}}{10}\right)}$$

where:
Z is the input impedance.
FS is the full scale of the device for the frequency in question.
SIGNAL is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio (PSRR)
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set 0.5 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics, but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude (set at 0.5 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. It may be reported in dBc (that is, degrades as signal level is lowered) or dBFS (always related back to converter full scale).

Transient Response Time
Transient response time is defined as the time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (that is, degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

Table 7. Output Coding (VREF = 2.5 V)

Step	$A_{IN} - \overline{A_{IN}}$	Digital Outputs Offset Binary	Digital Outputs Twos Complement	OR_A, OR_B
	>+0.768	11 1111 1111	01 1111 1111	1
1023	+0.768	11 1111 1111	01 1111 1111	0
.	.	.	.	.
.	.	.	.	.
513	+0.0015	10 0000 0001	00 0000 0001	0
512	0.0	10 0000 0000	00 0000 0000	0
511	–0.0015	01 1111 1111	11 1111 1111	0
.	.	.	.	.
.	.	.	.	.
0	–0.768	00 0000 0000	10 0000 0000	0
	< –0.768	00 0000 0000	10 0000 0000	1

EQUIVALENT CIRCUITS

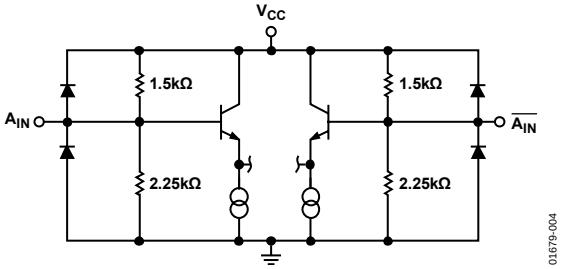

Figure 4. Equivalent Analog Input Circuit

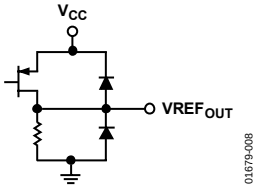

Figure 8. Equivalent Reference Output Circuit

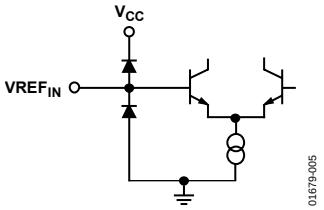

Figure 5. Equivalent Reference Input Circuit

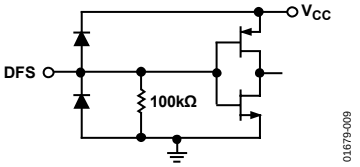

Figure 9. Equivalent DFS Input Circuit

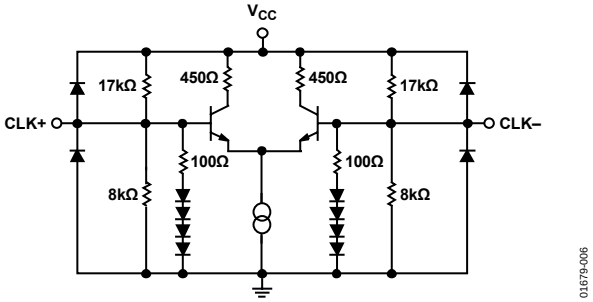

Figure 6. Equivalent Clock Input Circuit

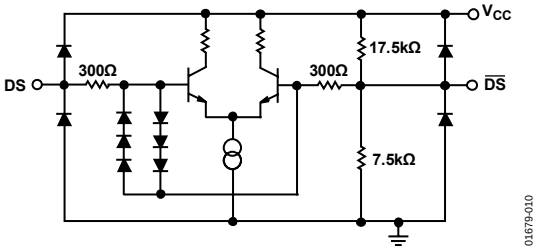

Figure 10. Equivalent DS Input Circuit

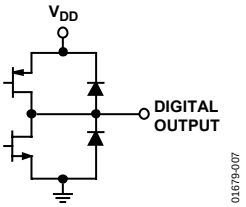

Figure 7. Equivalent Digital Output Circuit

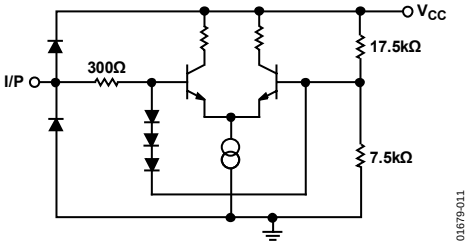

Figure 11. Equivalent I/P Input Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

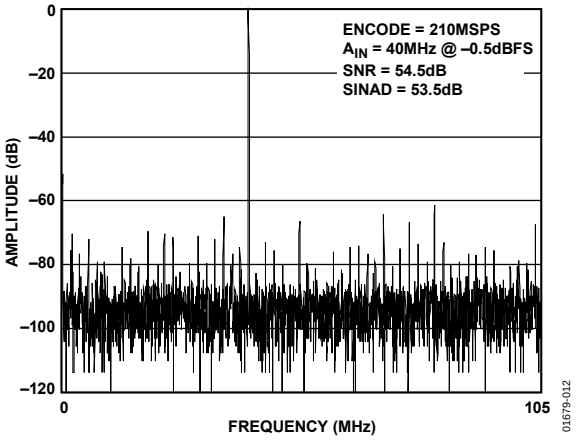

Figure 12. Single Tone at 40 MHz; 210 MSPS

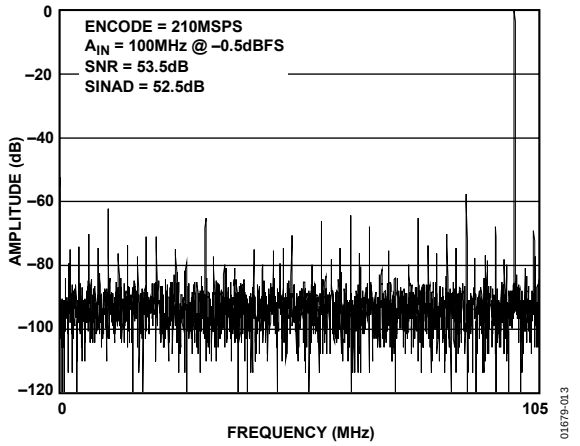

Figure 13. Single Tone at 100 MHz; 210 MSPS

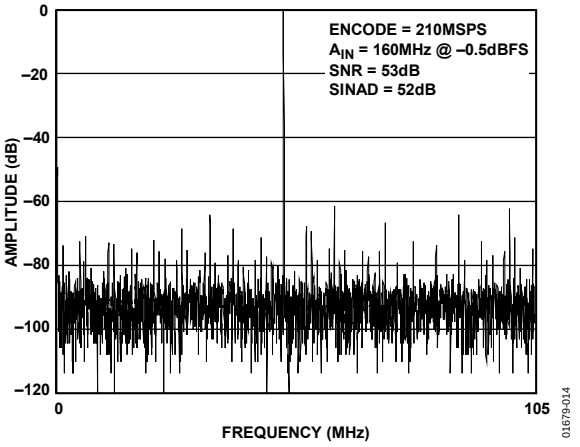

Figure 14. Single Tone at 160 MHz; 210 MSPS

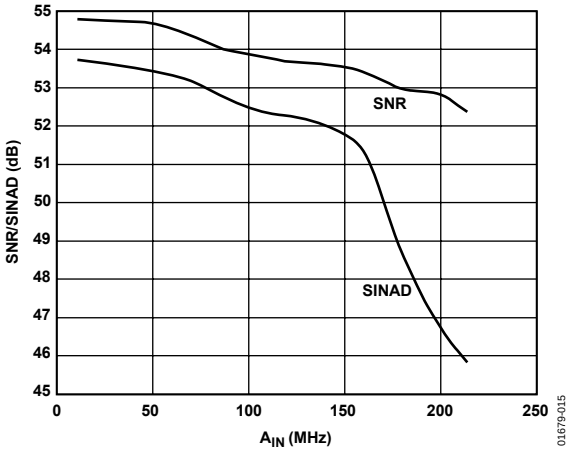

Figure 15. SNR/SINAD vs. A_{IN}; 210 MSPS

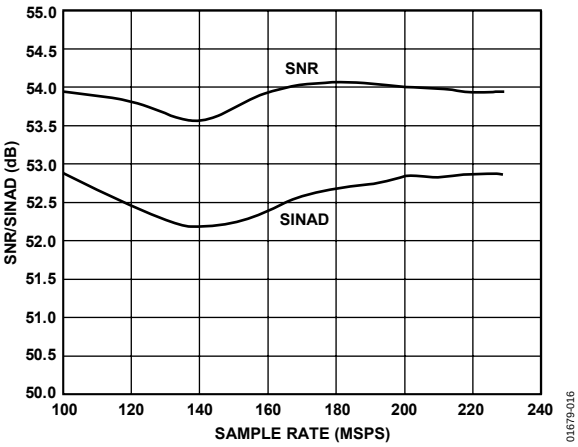

Figure 16. SNR/SINAD vs. Sample Rate; A_{IN} = 70 MHz

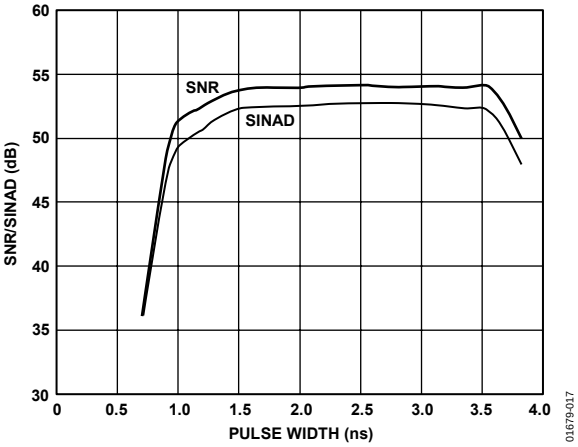

Figure 17. SNR/SINAD vs. Clock Positive Pulse Width (f_S = 210 MSPS, A_{IN} = 70 MHz)

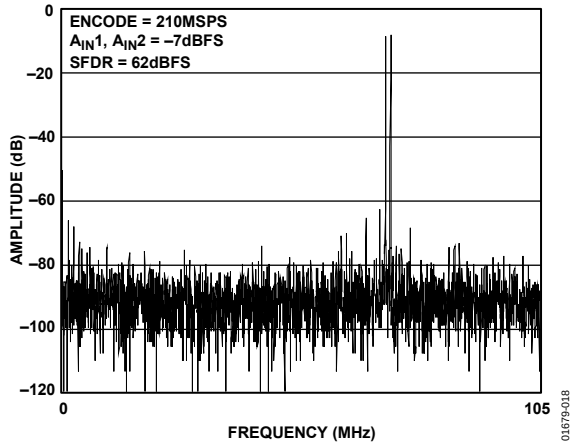

Figure 18. Two Tone Test $A_{IN}1 = 80.3$ MHz, $A_{IN}2 = 81.3$ MHz

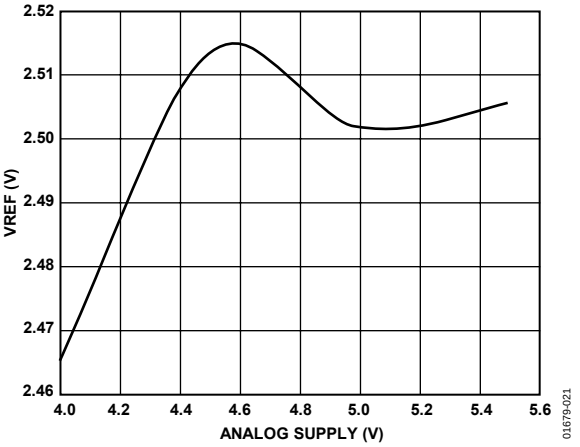

Figure 21. $VREF_{OUT}$ vs. Analog 5 V Supply

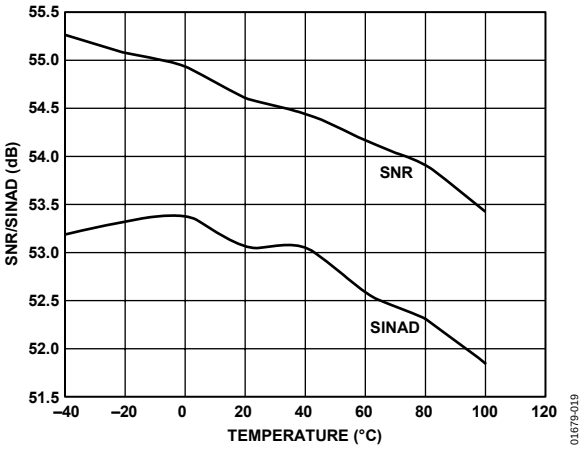

Figure 19. SNR/SINAD vs. Temperature, 210 MSPS, A_{IN} = 70 MHz

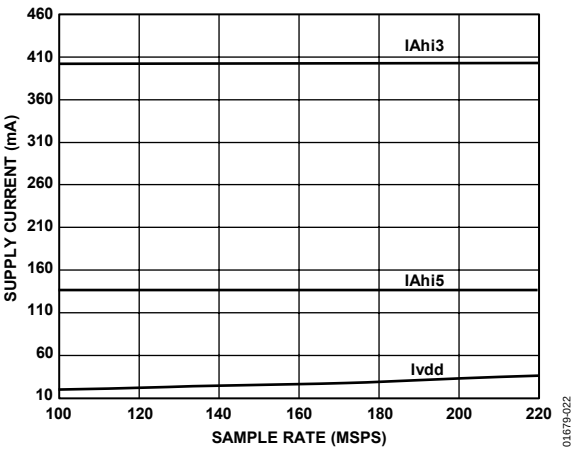

Figure 22. Power Supply Currents vs. Sample Rate

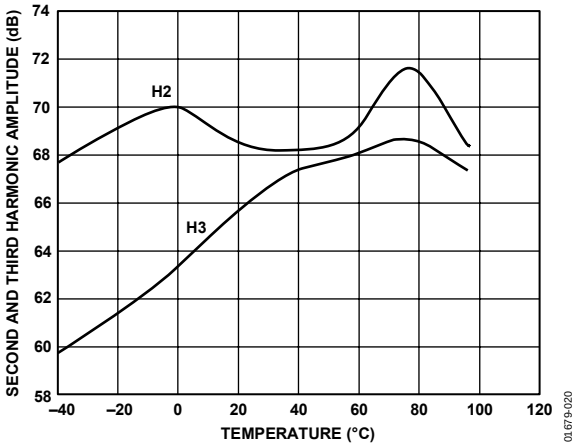

Figure 20. Second and Third Harmonics vs. Temperature; A_{IN} = 70 MHz, 210 MSPS

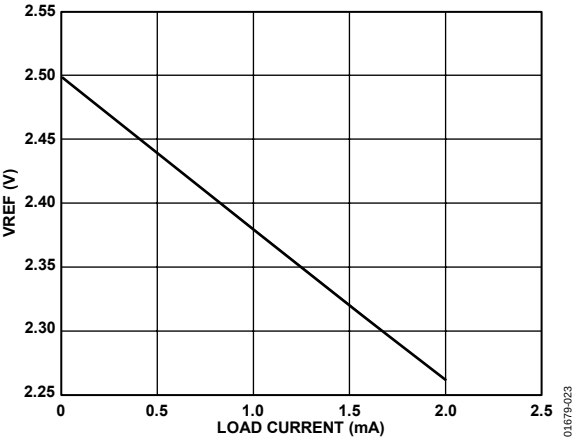

Figure 23. $VREF_{OUT}$ vs. I_{LOAD}

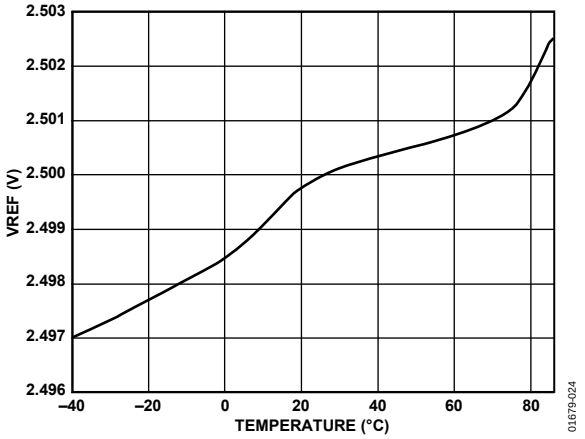

Figure 24. $VREF_{OUT}$ vs. Temperature

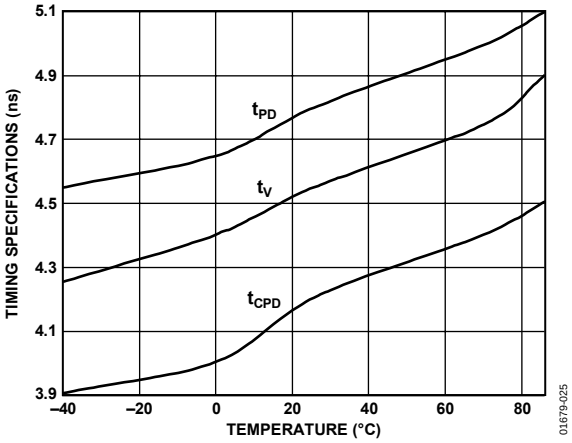

Figure 25. t_{PD}, t_V, t_{CPD} vs. Temperature

THEORY OF OPERATION

The AD9410 architecture is optimized for high speed and ease of use. The analog inputs drive an integrated high bandwidth track-and-hold circuit that samples the signal prior to quantization by the flash 10-bit core. For ease of use, the part includes an on-board reference and input logic that accepts TTL, CMOS, or PECL levels.

USING THE AD9410

Clock Input

Any high speed ADC is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock combines with the desired signal at the ADC output. For that reason, considerable care has been taken in the design of the clock input of the AD9410, and the user is advised to give commensurate thought to the clock source. To limit SNR degradation to less than 1 dB, a clock source with less than 1.25 ps rms jitter is required for sampling at Nyquist (for example, the Valpey Fisher VF561). Note that required jitter accuracy is a function of input frequency and amplitude. Refer to the Analog Devices, Inc. AN-501 application note, *Aperture Uncertainty and ADC System Performance*, for more information.

The clock input is fully TTL/CMOS compatible. The clock input can be driven differentially or with a single-ended signal. Best performance is obtained when driving the clock differentially. Both clock inputs are self-biased to $1/3 \times V_{CC}$ by a high impedance resistor divider (see the Equivalent Circuits section). Single-ended clocking, which can be appropriate for lower frequency or nondemanding applications, is accomplished by driving the clock input directly and placing a 0.1 µF capacitor at CLOCK.

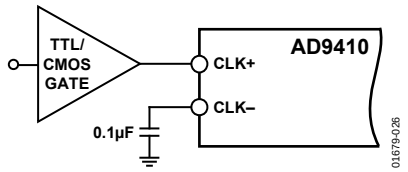

Figure 26. Driving Single-Ended Clock Input at TTL/CMOS Levels

An example where the clock is obtained from a PECL driver is shown in Figure 27. Note that the PECL driver is ac-coupled to the clock inputs to minimize input current loading. The AD9410 can be dc-coupled to PECL logic levels, resulting in the clock input currents increasing to approximately 8 mA typical, which is due to the difference in dc bias between the clock inputs and a PECL driver (see the Equivalent Circuits section).

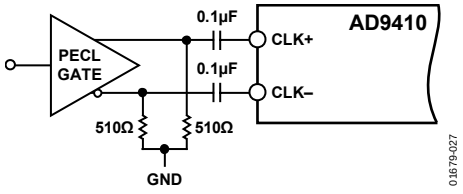

Figure 27. Driving the Clock Inputs Differentially

ANALOG INPUT

The analog input to the AD9410 is a differential buffer. For best dynamic performance, impedances at A_{IN} and $\overline{A_{IN}}$ should match. The analog input has been optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance degrades significantly if the analog input is driven with a single-ended signal. A wideband transformer, such as Mini-Circuits ADT1-1WT, can be used to provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog inputs are self-biased by an on-chip resistor divider to nominal 3 V (see the Equivalent Circuits section).

Special care was taken in the design of the Analog Input section of the AD9410 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1.5 V diff p-p.

The nominal differential input range is 768 mV p-p × 2.

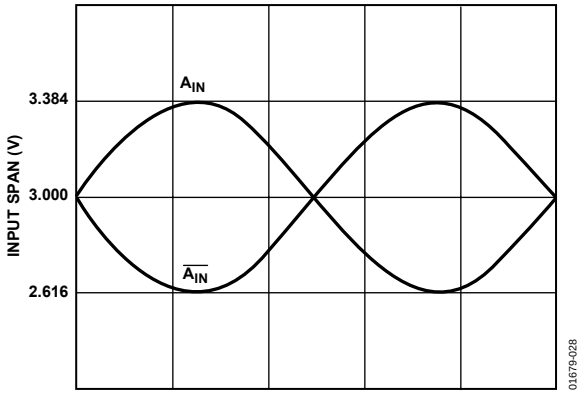

Figure 28. Typical Analog Input Levels

DIGITAL OUTPUTS

The digital outputs are TTL/CMOS compatible for lower power consumption. The outputs are biased from a separate supply (V_{DD}), allowing easy interface to external logic. The outputs are CMOS devices that swing from ground to V_{DD} (with no dc load). It is recommended to minimize the capacitive load the ADC drives by keeping the output traces short (<1 inch, for a total C_{LOAD} < 5 pF). It is also recommended to place low value (20 Ω) series damping resistors on the data lines to reduce switching transient effects on performance.

CLOCK OUTPUTS (DCO, $\overline{\text{DCO}}$)

The input clock is divided by two and available off-chip at DCO and $\overline{\text{DCO}}$. These clocks can facilitate latching off-chip, providing a low skew clocking solution (see Figure 2). These clocks can also be used in multiple AD9410 systems to synchronize the ADCs. Depending on application, DCO or $\overline{\text{DCO}}$ can be buffered and used to drive the DS inputs on a second AD9410, ensuring synchronization. The on-chip clock buffers should not drive more than 5 pF to 7 pF of capacitance to limit switching transient effects on performance.

VOLTAGE REFERENCE

A stable and accurate 2.5 V voltage reference is built into the AD9410 ($VREF_{OUT}$). The input range can be adjusted by varying the reference voltage. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage changes linearly within the ±5% tolerance.

TIMING

The AD9410 provides latched data outputs, with six pipeline delays in interleaved mode (see Figure 2). In parallel mode, the Port A has one additional cycle of latency added on-chip to line up transitions at the data ports, resulting in a latency of seven cycles for the Port A. The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9410; these transients can detract from the dynamic performance of the converter.

The minimum guaranteed conversion rate of the AD9410 is 100 MSPS. At internal clock rates below 100 MSPS, dynamic performance may degrade. Note that lower effective sampling rates can be obtained simply by sampling just one output port—decimating the output by two. Lower sampling frequencies can also be accommodated by restricting the duty cycle of the clock such that the clock high pulse width is a maximum of 5 ns.

DATA SYNC (DS)

The data sync input, DS, can be used in applications requiring that a given sample appear at a specific output Port A or Port B. When DS is held high, the ADC data outputs and clock do not switch and are held static. Synchronization is accomplished by the assertion (falling edge) of DS, within the timing constraints t_{SDS} and t_{HDS} relative to an clock rising edge. (On initial synchronization, t_{HDS} is not relevant.) If DS falls within the required setup time (t_{SDS}) before a given clock rising edge N, the analog value at that point is digitized and available at Port B six cycles later (interleaved mode). The next sample, N+1, is sampled by the next rising clock edge and available at Port A six cycles after that clock edge (interleaved mode). In dual parallel mode, Port A has a seven cycle latency, and Port B has a six cycle latency, but data is available at the same time.

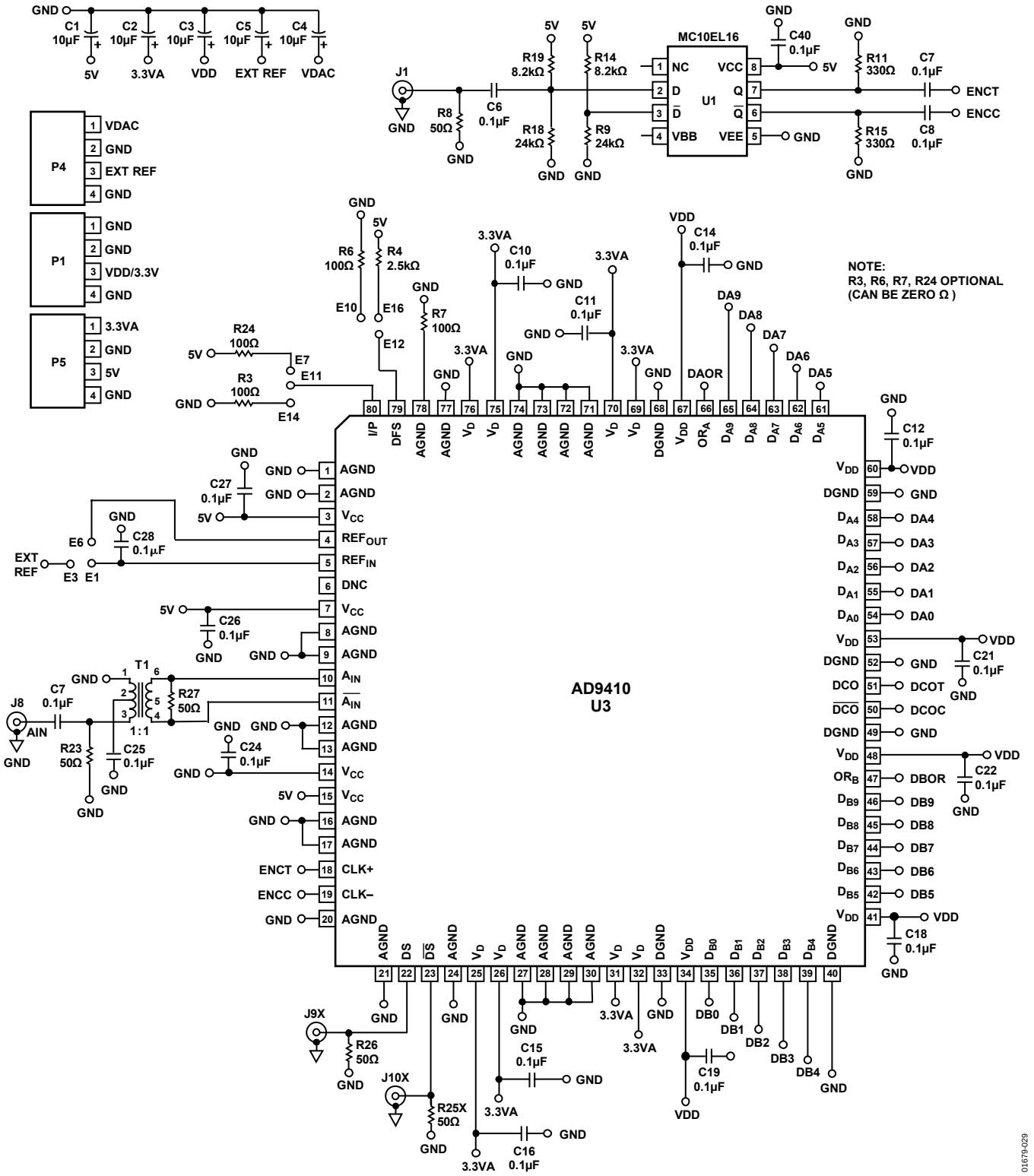

Figure 29. PCB Schematic Example

OUTLINE DIMENSIONS

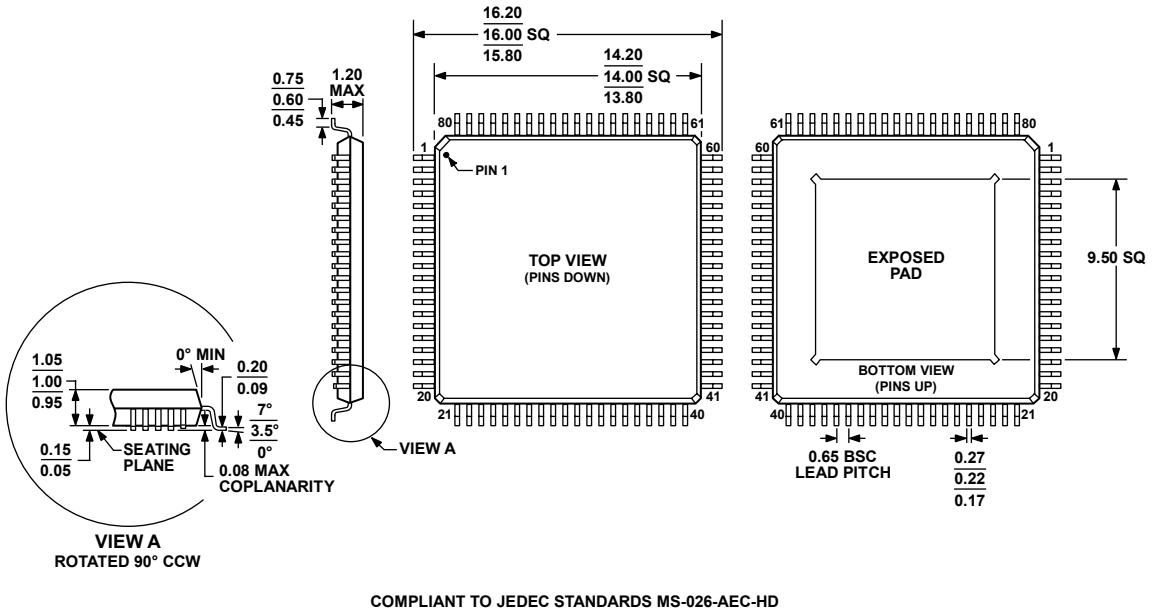

Figure 30. 80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-80-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Option
AD9410BSVZ[1]	−40°C to +85°C	80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-80-4

[1] Z = RoHS Compliant Part.

NOTES

C01679-0-7/07(A)