MagnaChip

MAP7102

Dual Output LCD Bias IC

General Description

The MAP7102 is designed to support positive / negative driven TFT-LCD panels. The two output rails are usually connected to the Source Driver IC. The device uses a single inductor scheme in order to provide the user the smallest solution size possible as well as high efficiency. With its input voltage range of 2.8V to 5.5V, it is optimized for products powered by single-cell batteries and output currents up to 50mA.

The device is delivered in a WLCSP package of 15 balls.

Application :

- TFT LCD Smartphones
- TFT LCD Tablets
- General Dual Power Supply Applications

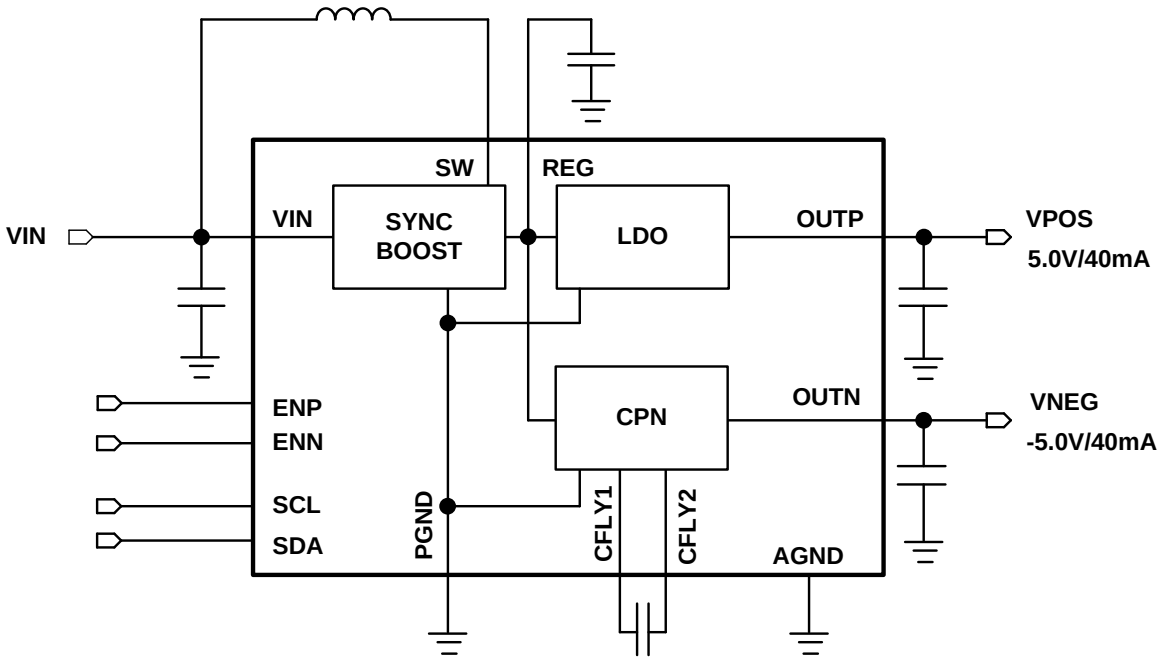
Features

- SIMO(Single-Inductor Multiple output) regulator Technology
- 86% Efficiency for 20mA Load current Between +5.0V and -5.0V.
- 2.8V to 5.5V Input Voltage Range
- Under-Voltage Lockout Rising/Falling
- Programmable Output Voltages
- Positive Output Voltage Range : 4.0V to 5.7V (0.1V Step)
- Negative Output Voltage Range : -4.0V to -5.7V (0.1V Step)
- 1%(Typ.) Output Voltage Accuracy
- Maximum Output Current : 50mA
- Programmable Active Discharge
- Excellent Line Regulation
- Advanced Power-Save Mode for Light-load Efficient
- Integrated Compensation and Feedback circuits
- Fully integrated FETs for Synchronous rectification
- Short Circuit Protection
- Thermal Shutdown Protection
- 15-Ball WLCSP Package

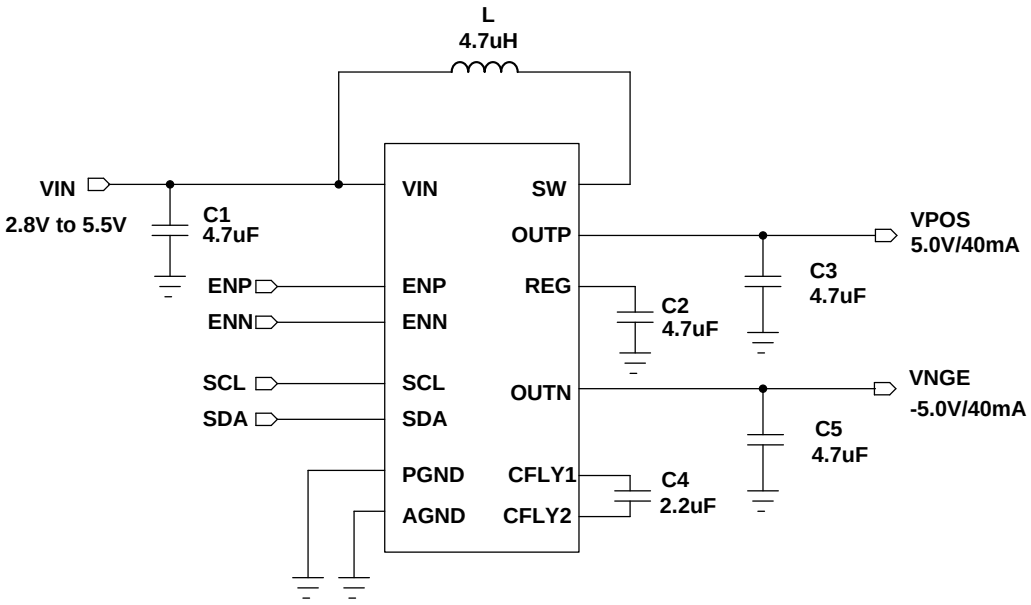
Ordering Information

Part Number	Top Marking	Junction Temperature Range	Package	RoHS Status
MAP7102WCRH	7102 LLL YWNMM	-40℃ to +85℃	15 bump 0.4mm pitch CSP	Halogen Free

Block Diagram



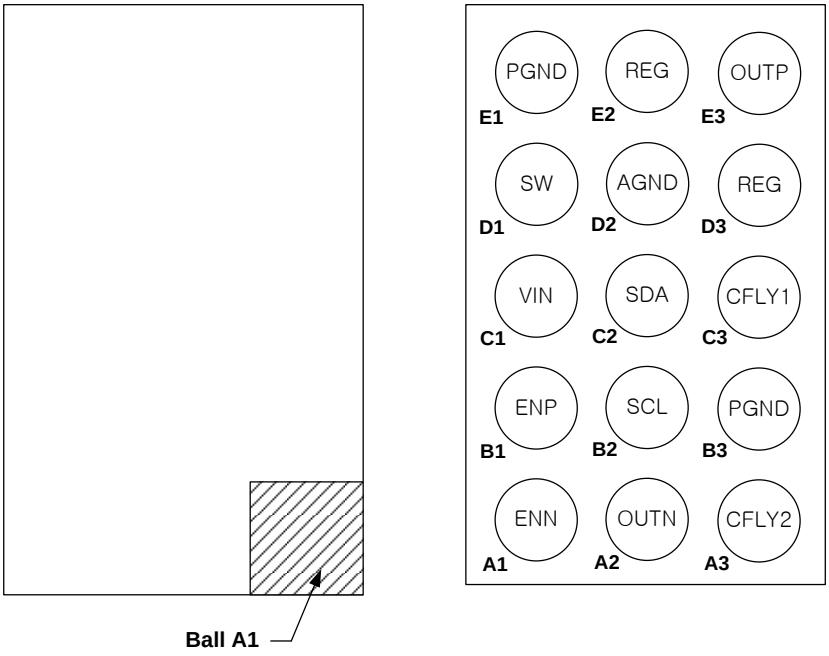
Application Circuit



Bill of Materials :

item	Part Number	Manufacturer	Description	Qty.
PMIC	MAP7102	Magnachip	Dual Output DC-DC	1
LX	DFE252012C	TOKO	4.7uH, 1.6A, 250mohm,	1
C4	GRM188R61C225KAAD	Murata	2.2μF, 16 V, 0603, X5R, ceramic	1
C1/C2/C3/C5	GRM188R61C475KAAJ	Murata	4.7μF, 16 V, 0603, X5R, ceramic	4

Pin Configuration



Top View Bottom View

PIN Description

Pin Name	Pin Number	Description
ENN	A1	Enable pin for V_{NEG} rail
OUTN	A2	Output pin of the negative charge pump (V_{NEG})
CFLY2	A3	Negative charge pump flying capacitor pin
ENP	B1	Enable pin for V_{POS} rail
SCL	B2	I²C interface clock signal pin
PGND	B3, E1	Power ground
VIN	C1	Input voltage supply pin
SDA	C2	I²C interface data signal pin
CFLY1	C3	Negative charge pump flying capacitor pin
SW	D1	Switch pin of the boost converter

AGND	D2	Analog ground
REG	D3, E2	Boost converter output pin
OUTP	E3	Output pin of the LDO (V_{POS})

Absolute Maximum Ratings

Absolute Maximum Ratings (Note)

Parameter	Value	Unit
CFLY1,OUTP, REG, SCL, SDA, VIN	-0.3 to 6.0	V
ENP, ENN	-0.3 to V_{IN} + 0.3V	V
SW	-0.3V to VOUTP+0.3	V
CFLY2, OUTN	-6.0 to 0.3	V
Operating ambient temperature range, T_A	-40 to +85	℃
Ambient Storage Temperature (Ts)	-65 to +150	℃
Junction Thermal Resistance (θ_{JA})(Note)	76.5	℃/W
ESD HBM Rating	2	kV
ESD MM Rating	200	V

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Parameter	Value	Unit
Input Voltage Range	2.8 to 5.5	V
Inductor	2.2 to 4.7	uH
Input Capacitor	4.7 to 10	uF
Flying Capacitor	2.2 to 4.7	uF
Output Capacitor	4.7 to 10	uF
Operating ambient temperature	-40 to +85	℃
Operating junction temperature	-40 to +125	℃

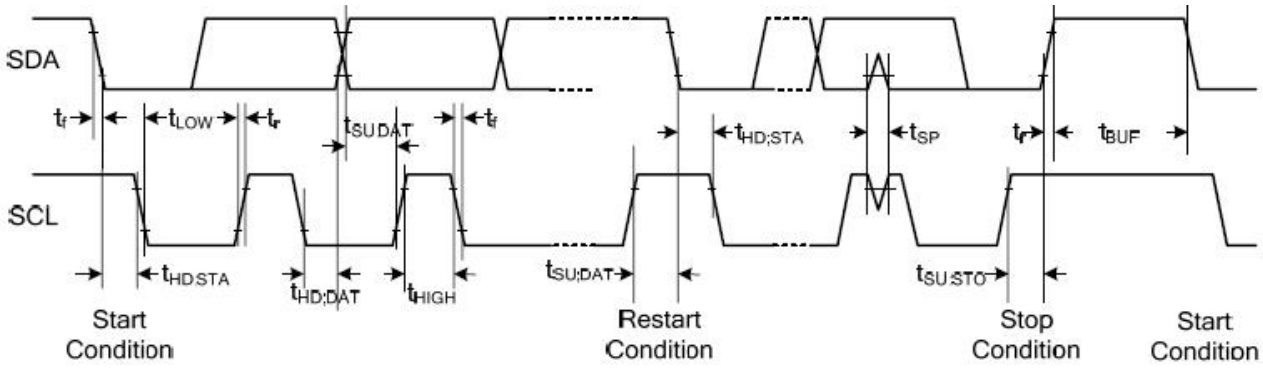
ELECTRICAL CHARACTERISTICS

V_{IN} = 3.8 V, ENN = ENP = V_{IN}, V_{POS} = 5.0 V, V_{NEG} = –5.0 V, T_A = –40°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
General Section						
V_{IN}	Input Voltage Range		2.8		5.5	V
V_{UVLO}	Under Voltage Lock Out	Rising Threshold voltage		2.6	2.8	V
		Falling Threshold Voltage		2.1	2.3	V
IQ(ON)	Quiescent Current	Enable=High, Switching Mode		1.3		mA
IQ(OFF)	Shutdown Current	Enable=Low		1	3	uA
V_{IH}	Enable High Threshold		1.2			V
V_{IL}	Enable Low Threshold				0.4	V
R_{EN}	Enable Pull down resistance	EN_P/N(Note1)		200		kΩ
T_{SD}	Thermal Shutdown Temperature	(Note1)		140		℃
T_{SD_HYS}	Thermal Shutdown Hysteresis	(Note1)		10		℃
Boost Converter_ VREG						
$I_{LIMVREG}$	VREG Current Limit	(Note1)	0.9	1.2	1.5	A
F_{SW}	Boost Switching Frequency		1.44	1.8	2.25	MHz
R_{ONLXPG}	Internal MOSFET Switch ON-Resistance from LXP to GND	IOUT= 100mA (Note1)		175		mΩ
R_{ONLXPO}	Internal MOSFET Switch ON-Resistance from LXP to VBST	IOUT= 100mA (Note1)		240		mΩ
I_{LXPLX}	LX Leakage Current	VLXP=5.0V, EN=0V			10	uA
tss	Soft Start time	(Note1)		0.7	2	ms
Negative Charge Pump Output _ VNEG						
V_{NEG}	Negative Output Voltage Range		-4.0		-5.7	V
	VNEG Output voltage Accuracy	2.8V<VIN<5.5V TA = –40°C to 85°C	-1.5		1.5	%
F_{SWN}	Charge Pump Switching Frequency		0.8	1.0	1.2	MHz
	Line Regulation	ΔVIN=1V, INEG=30mA(Note1)		0.04		%/V
	Load Regulation	(Note1)		0.19		%/50mA
I_{CPLX}	CP Leakage Current	VCP=6.0V, EN=0V			10	uA
R_{DISCH}	Discharge Resistance	(Note1)		20		Ω
t_{SSVNEG}	VNEG Soft Start time	(Note1)		0.7	2	ms
LDO Output _ VPOS						
V_{POS}	Positive Output Voltage Range		4.0		5.7	V
	VPOS Output voltage Accuracy	2.8V<VIN<5.5V TA = –40°C to 85°C	-1.5		1.5	%
VDRP1	Dropout Voltage LDO	IPOS=100mA			100	mV
	Line Regulation	ΔVIN=1V, IPOS=30mA(Note1)		0.04		%/V
	Load Regulation	(Note1)		0.31		%/50mA
I_{LDOLX}	VPOS Leakage Current	VPOS=0V, EN=0V			1	uA
R_{DISCH}	Discharge Resistance	(Note1)		70		Ω
t_{SSVPOS}	VPOS Soft Start time	(Note1)		0.7	2	ms

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I²C interface (Note 1)						
V_{OL}	Output Data Logic Low Voltage	I_{PULLUP}=4mA			0.17	V
I_{LEAK}	Input Leakage on SDA/SCL		-10		10	uA
t_{EN_I2C}	Minimum time Between EN high and I2C Enabled			0.5		ms
f_{SCL}	SCL Clock Frequency				400	kHz
t1	Bus Free Time Between stop and Start condition		1.3			us
t2	$t_{HD:STA}$ Hold Time after(Repeated) START condition	After this Period, the First Clock is generated	0.6			us
$t_{SU:STA}$	Repeated Start condition setup time		0.6			us
$t_{SU:STO}$	Stop Condition Setup Time		0.6			us
$t_{HD:DAT}$	Data Hold Time		300			ns
$t_{SU:DAT}$	Data Setup Time		100			ns
t_3	Low Period of SCL Clock		1.3			us
t_4	High Period of SCL Clock		0.6			us
t_F	Clock/Data Fall Time				300	ns
t_R	Clock/Data Rise Time				300	ns
C_{CDMAX}	Clock/data Maximum Capacitance				400	pF

Note1) Guaranteed by design; not test in production



Definition of timing for F/S-mode devices on the I²C bus

TYPICAL CHARACTERISTICS

V_{IN}= 3.8 V, V_{POS}= 5.0 V, V_{NEG}= –5.0 V, unless otherwise noted

TABLE OF GRAPHS

Efficiency [VPOS=5.0V,VNEG=-5.0V]

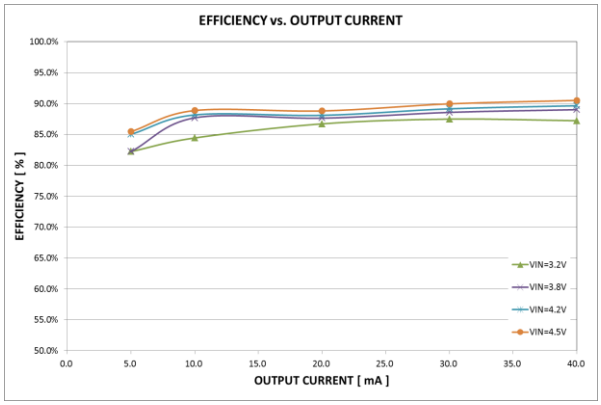


Figure 1. Efficiency – Inductor [4.7uH]

Quiescent Current vs. Input Voltage

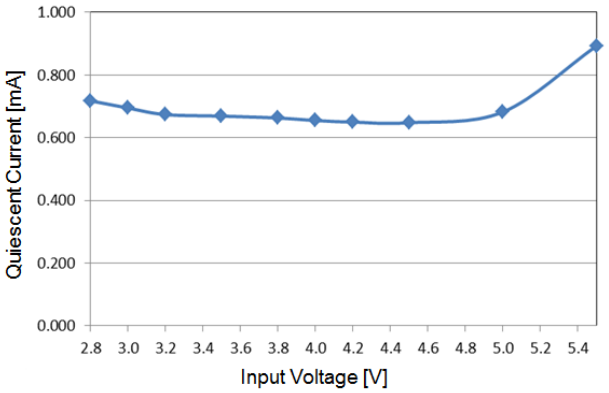


Figure 2. Quiescent Current

Power ON Sequence

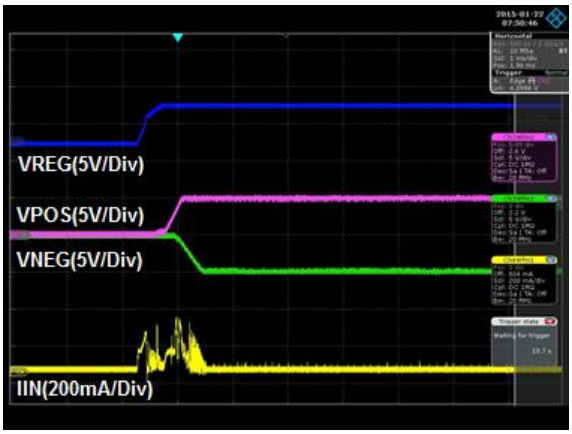


Figure 3. Power ON Sequence

Power OFF Sequence

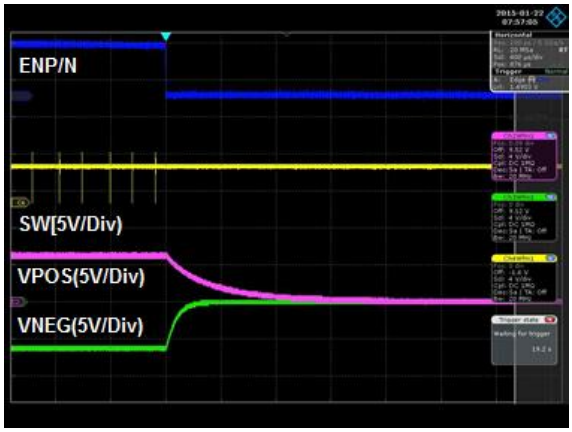


Figure 4. Power OFF Sequence

VPOS Ripple

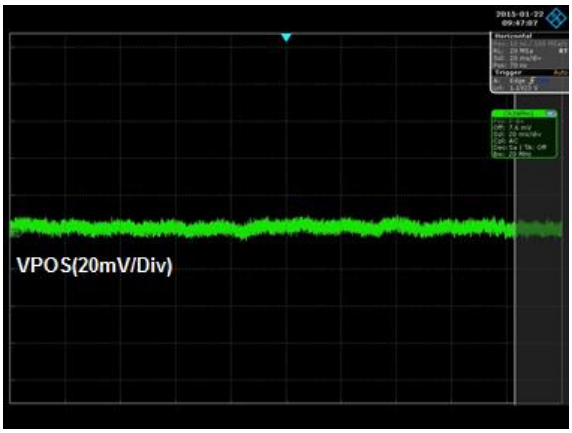


Figure 5. Power Up/Down with Fast Discharging

VNEG Ripple

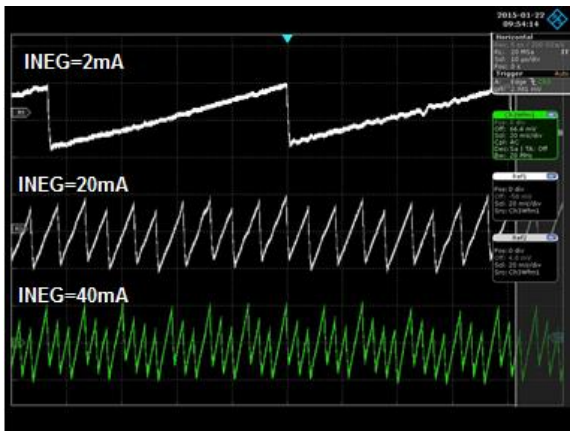


Figure 6. VNEG Ripple

VPOS Output Light Load

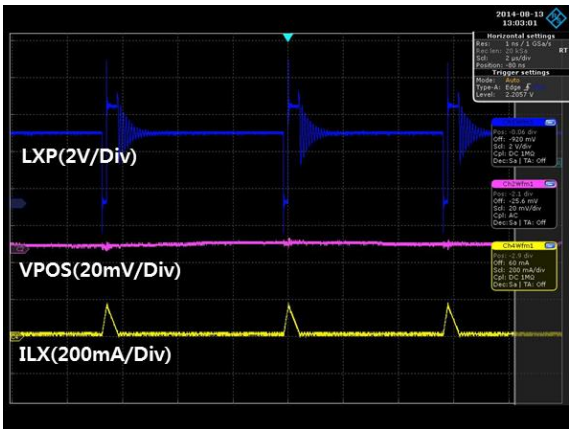


Figure 7. VPOS Output Voltage – Light Load(10mA)

VPOS Output Heavy Load

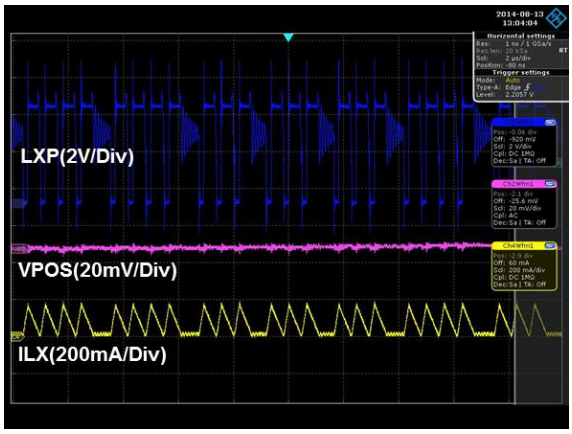


Figure 8. VPOS Output Voltage – Heavy Load(40mA)

VNEG Output Light Load

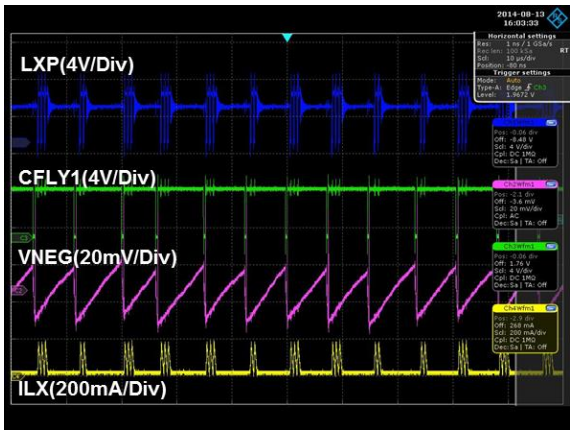


Figure 9. VNEG Output Voltage – Light Load(10mA)

VNEG Output Heavy Load

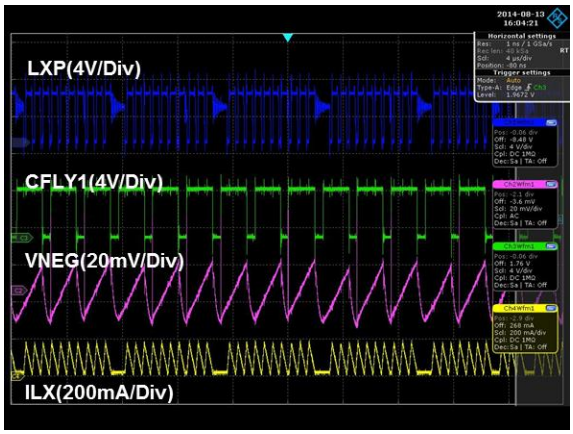


Figure 10. VNEG Output Voltage – Heavy Load(40mA)

VPOS Output Voltage vs. Input Voltage

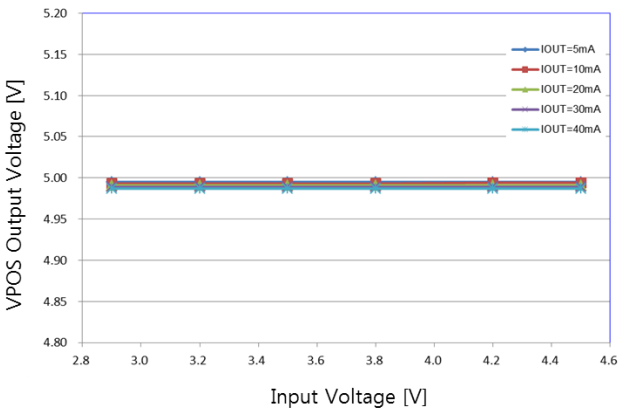


Figure 11. Line Regulation – VPOS=5.0V

VNEG Output Voltage vs. Input Voltage

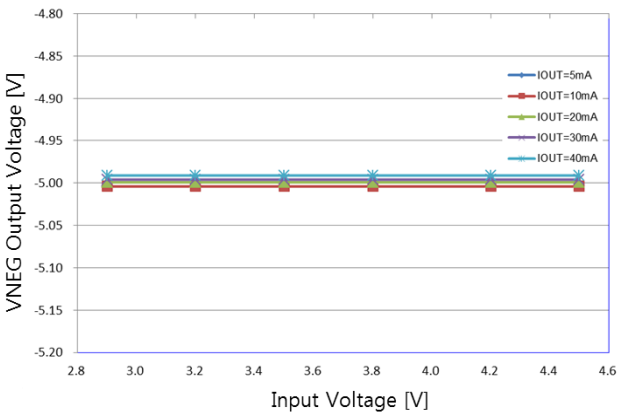


Figure 12. Line Regulation – VNEG=-5.0V

VPOS Output Voltage vs. Load Current

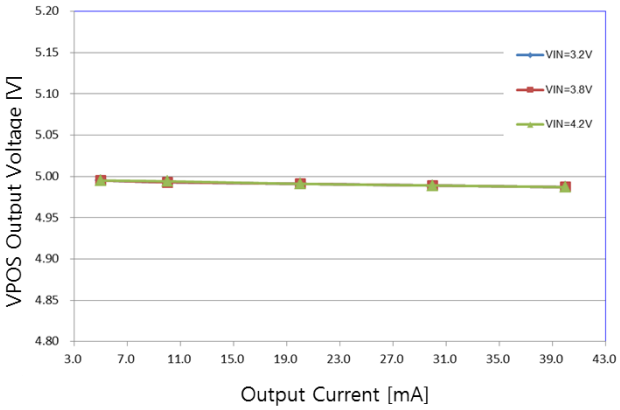


Figure 13. Load Regulation – VPOS=5.0V

VNEG Output Voltage vs. Load Current

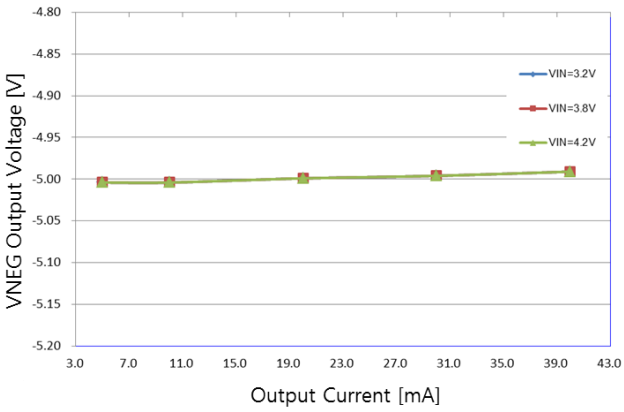


Figure 14. Load Regulation – VNEG=-5.0V

Load Transient

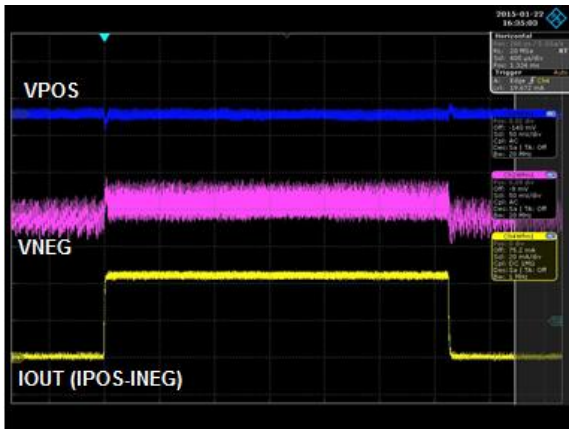


Figure 15. Load Regulation[VIN=2.9V, ΔIOUT=45mA]

Load Transient

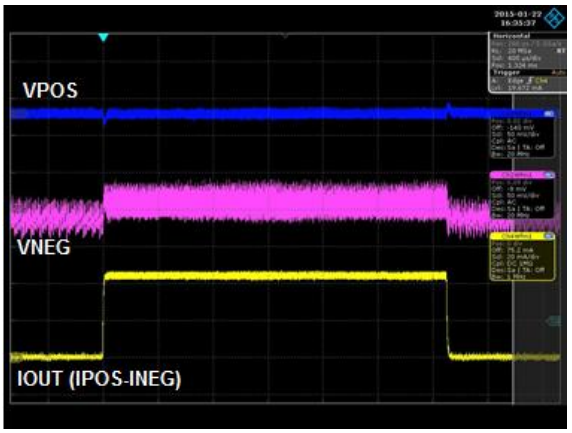


Figure 16. Load Regulation[VIN=3.8V, ΔIOUT=45mA]

Power Up/Down with Fast Discharging

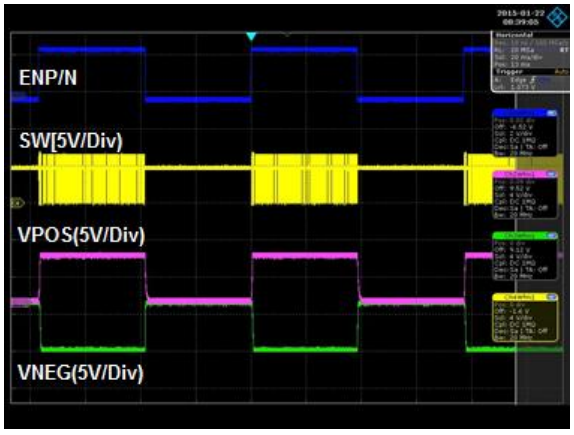


Figure 17. Power Up/Down with Fast Discharging

Applications

Under-voltage Lockout

If the input voltage falls below the V_{UVLO} level of 2.1V, all the DC/DC regulators of MAP7102 are disabled, and all the rails will restart with soft-start when input voltage is applied again

ENP/ENN

The ENP pin controls the output of VPOS and the ENN pin controls the output of VNEG. A high on either ENP or ENN will enable the boost converter VREG. VPOS, VNEG and VREG require both their respective EN pin high for each to be enabled

Power On / Off Sequence

The VREG boost regulator is activated when the input voltage is higher than the UVLO threshold, and either ENP or ENN are high. The VPOS output is activated if ENP is high and VREG has completed its soft-start. The VNEG output is activated if ENN is high and VREG has completed its soft-start.

ENP or ENN being pulled low shuts down VPOS or VNEG, respectively. If both ENP and ENN are pulled low, VPOS, VNEG and VREG are all turned off

The discharge resistors of the VPOS and VNEG output are 70Ω and 20Ω respectively.

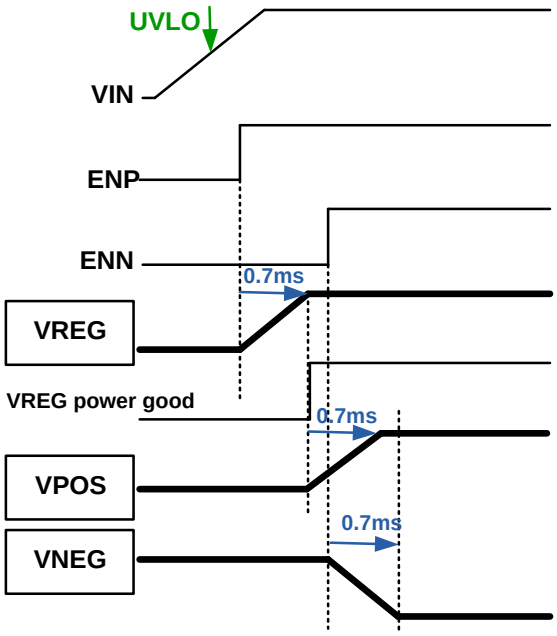


Figure 18: Example of power on sequence when ENN rising after VPOS soft-start finished

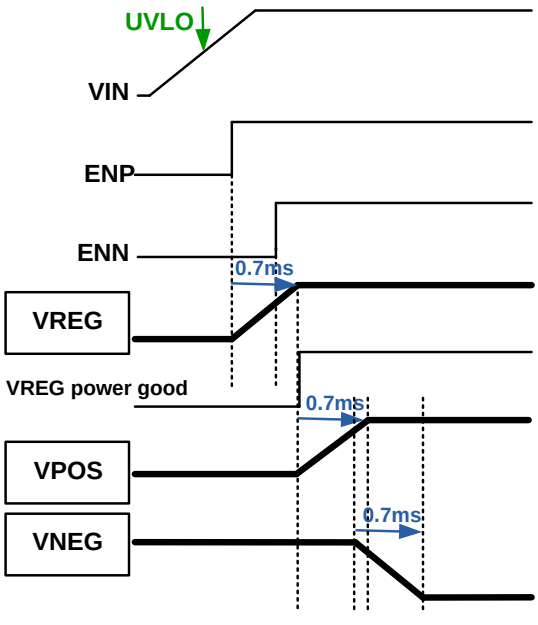


Figure 19: Example of power on sequence when both ENP and ENN rising before VREG soft-start finished

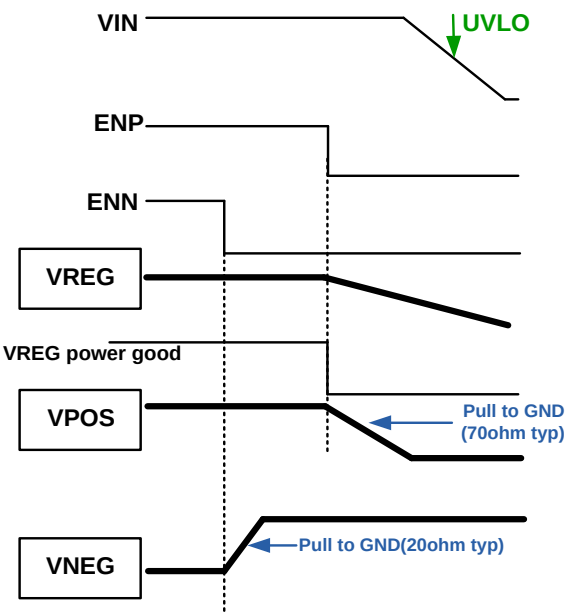


Figure 20: Example of power off sequence activated by ENP and ENN when VIN is above UVLO

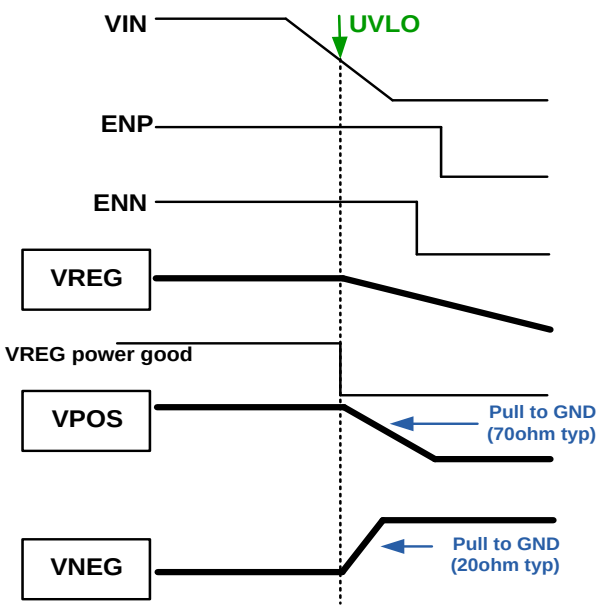


Figure 21: Example of power off sequence activated by VIN falling below UVLO

REGISTER MAP

Slave Address : 3Eh [Bit : 0111110x]

Table 1. I2C Registers

Register	R/W	Function	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	R/W	VPOS	Not Used			VPOS[4]	VPOS[3]	VPOS[2]	VPOS[1]	VPOS[0]
01h	R/W	VNEG	Not Used			VNEG[4]	VNEG[3]	VNEG[2]	VNEG[1]	VNEG[0]
03h	R/W	DIS	Not Used						DISP	DISN

Table 2. VPOS/VNEG Voltage Setting

NO.	CODE					HEX	VPOS	VNEG
	BIT4	BIT3	BIT2	BIT1	BIT0			
1	0	0	0	0	0	**00h**	**4.0V**	**-4.0V**
2	0	0	0	0	1	**01h**	**4.1V**	**-4.1V**
3	0	0	0	1	0	**02h**	**4.2V**	**-4.2V**
4	0	0	0	1	1	**03h**	**4.3V**	**-4.3V**
5	0	0	1	0	0	**04h**	**4.4V**	**-4.4V**
6	0	0	1	0	1	**05h**	**4.5V**	**-4.5V**
7	0	0	1	1	0	**06h**	**4.6V**	**-4.6V**
8	0	0	1	1	1	**07h**	**4.7V**	**-4.7V**
9	0	1	0	0	0	**08h**	**4.8V**	**-4.8V**
10	0	1	0	0	1	**09h**	**4.9V**	**-4.9V**
11	0	1	0	1	0	**0Ah**	**5.0V**	**-5.0V**

NO.	CODE					HEX	VPOS	VNEG
	BIT4	BIT3	BIT2	BIT1	BIT0			
12	0	1	0	1	1	**0Bh**	**5.1V**	**-5.1V**
13	0	1	1	0	0	**0Ch**	**5.2V**	**-5.2V**
14	0	1	1	0	1	**0Dh**	**5.3V**	**-5.3V**
15	0	1	1	1	0	**0Eh**	**5.4V**	**-5.4V**
16	0	1	1	1	1	**0Fh**	**5.5V**	**-5.5V**
17	1	0	0	0	0	**10h**	**5.6V**	**-5.6V**
18	1	0	0	0	1	**11h**	**5.7V**	**-5.7V**

I²C BUS Control

I²C INTERFACE

Data transmission from the main *u*P to MAP7102 and vice versa takes place through the I²C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to a positive supply voltage must be externally connected)

INTERFACE PROTOCOL

The interface protocol is composed of five commands below table.

Table 3. I²C protocol commands

Command	Type	Description	State
START	Condition	A start condition	SCL=1, SDA 1 to 0
STOP	Condition	A stop condition	SCL=1, SDA 0 to 1
DEVICE ADDR + W/R	Byte	A device address and W/R	Write=0 / Read=1
ADDR	Byte	A Register address byte	-
DATA	Byte	A Data byte	-

The Register address byte determines the first register in which the read or write operation takes places. When the read or write operation is finished, the register address is automatically incremented.

Table 4. I2C Packet format

START	7	6	5	4	3	2	1	0	ACK	7	6	5	4	3	2	1	0	ACK	7	6	5	4	3	2	1	0	ACK	STOP
	DEVICE ADDRESS (7Bit)							R/W		REGISTER ADDRESS (8Bit)									DATA (Bit)									

START AND STOP CONDITIONS

Both Data and Clock lines remain HIGH when the bus is not busy. As shown in below figure, a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

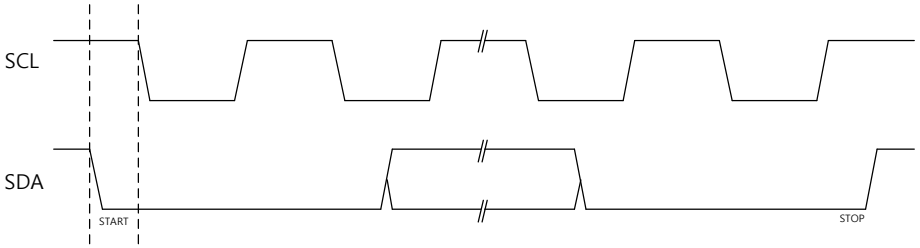


Figure 22 Timing Diagram on I^{2}C Bus

DATA VALIDITY

The data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

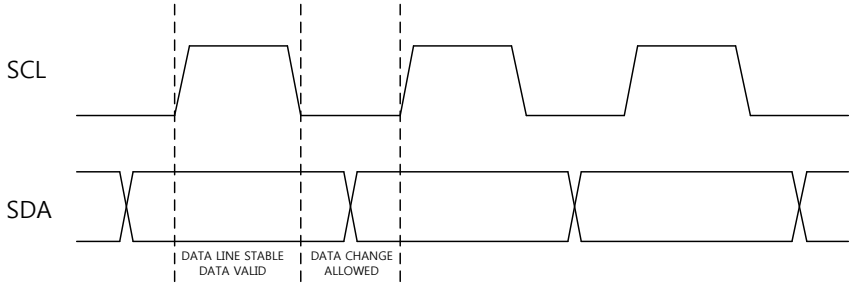


Figure 23 Data validity on I^{2}C Bus

DATA ACKNOWLEGE

The master (*u*P) puts a resistive HIGH level on the SDA line during the acknowledge bit. The MSB is transferred first. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Any change in the SDA line at this time will be interpreted as a control signal.

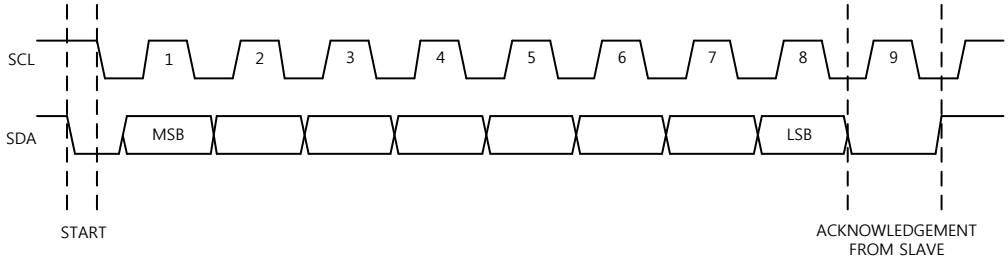


Figure 24 Data acknowledge on I^{2}C Bus

WRITING TO A SINGLE REGISTER

Writing to a single register starts with a START bit followed by the 7 bit device address of MAP7102. The 8th bit is the W/R bit, which is 0 in this case. W/R=1 means a reading operation. Then the master waits for an acknowledge from MAP7102. Then the 8 bit address of register is sent to MAP7102. It is also followed by an acknowledge pulse. The last transmitted byte is the data that is going to be written to the register. It is again followed by an acknowledge pulse from MAP7102. The master then generates a STOP bit and the communication is over.

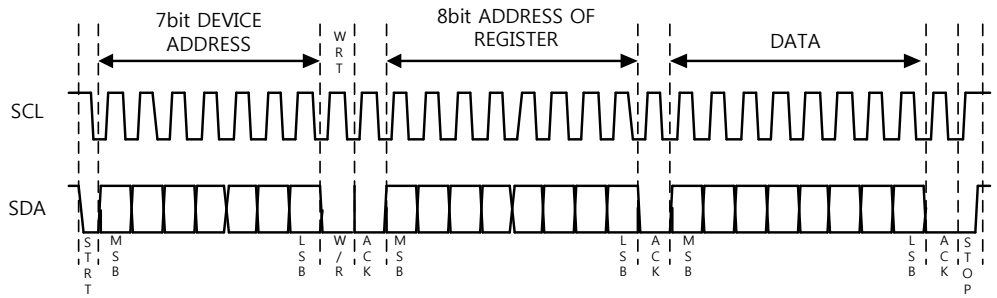


Figure 25 Writing to a single register

WRITING TO MULTIPLE REGISTERS WITH INCREMENTAL ADDRESSING

It would be unpractical to send several times the device address and the address of the register when writing to multiple registers. MAP7102 supports writing to multiple registers with incremental addressing. When data is written to a register, the address register is automatically incremented. So the next data can be sent without sending the device address and the register address again.

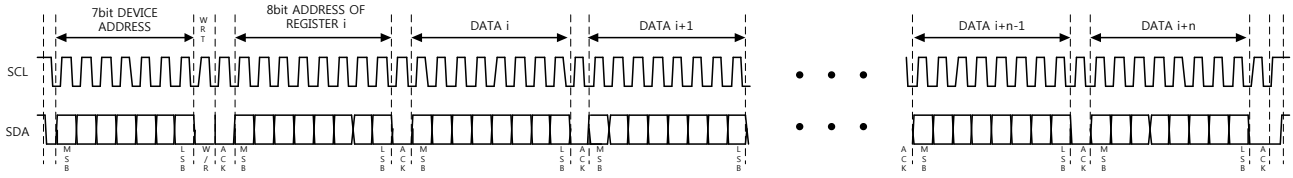


Figure 26 Writing to multiple registers

READING FROM A SINGLE REGISTER

The reading operation starts with a START bit followed by the 7bit device address of MAP7102. The 8-th bit is the W/R bit, which is 0 in this case. MAP7102 confirms the receiving of the address + W/R bit by an acknowledge pulse. The address of the register which should be read is sent afterwards and confirmed again by an acknowledge pulse of MAP7102 again. Then the master generates a START bit again and sends the device address followed by the W/R bit, which is 1 now. MAP7102 confirms the receiving of the address+ W/R bit by an acknowledge pulse and starts to send the data to the master. No acknowledge pulse from the master is required after receiving the data. Then the master generates a STOP bit to terminate the communication.

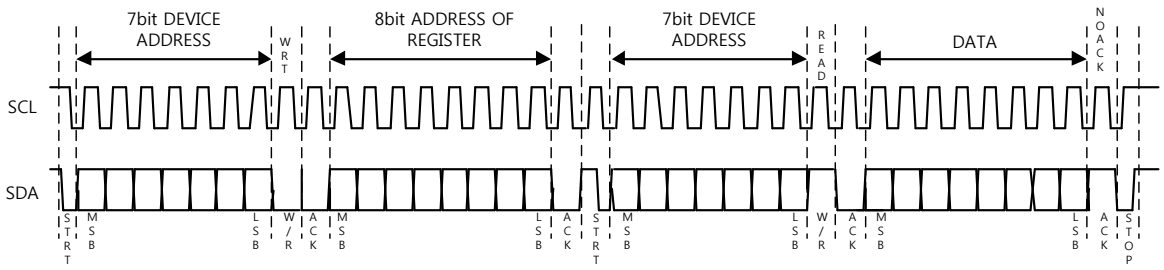


Figure 27 Reading from a single register

READING FROM MULTIPLE REGISTERS WITH INCREMENTAL ADDRESSING

Reading from multiple registers starts in the same way like reading from a single register. As soon as the first register is read, the register address is automatically incremented. If the master generates an acknowledge pulse after receiving the data from the first register, then reading of the next register can start immediately without sending the device address and the register address again. The last acknowledge pulse before the STOP bit is not required.

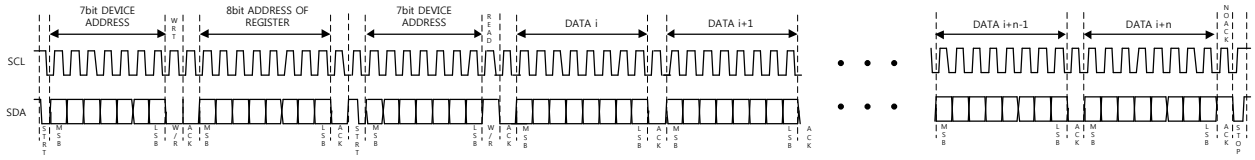
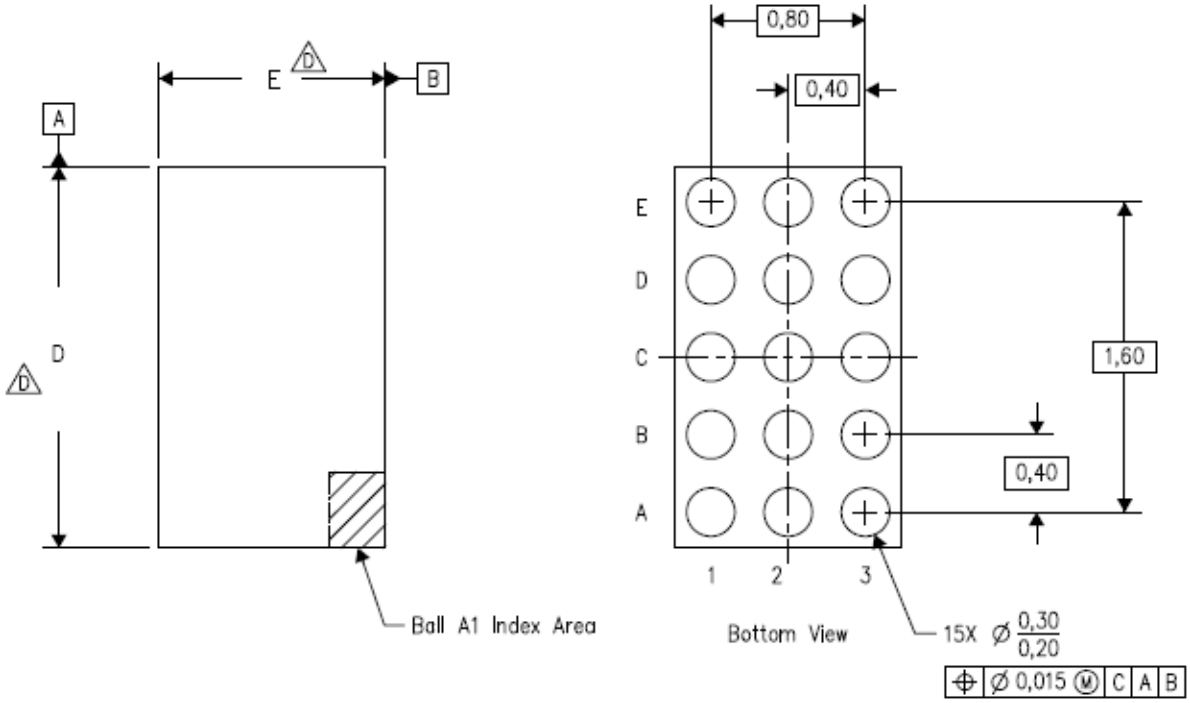
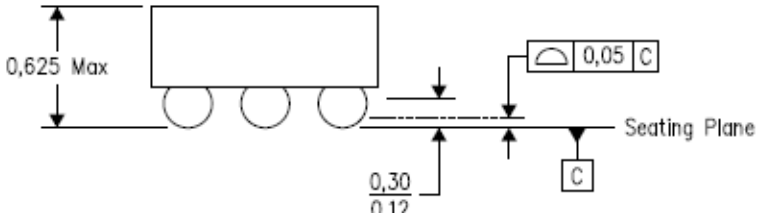


Figure 28 Reading from multiple registers

PACKAGE INFORMATION

E : 1550 ± 30um. D : 2150 ± 30um.





REVISION HISTROY

Date	Version	Changes
2013.05.07	0.0	Initial Release.
2013.06.27	0.1	VPOS/VNEG Output Voltage range : 6.0V → 5.7V, -6.0V → -5.7V Register Map change.
2013.11.22	0.2	Electrical Characteristic Spec updated - Maximum Current : 80mA → 50mA - External Component Change - VPOS/VNEG Line & Load Regulation → Test Condition & Spec change
2014.01.21	0.3	Maximum rate Spec updated - All Control Pin : -0.3V to 6.6V → -0.3V to 6.0V - SW pin Spec : -0.3V to 6.6V → -0.3V to VOUTP+0.3V
2014.09.15	0.4	Add to Graph Input voltage Range change : Min 2.5V → Min 2.8V VPOS/VNEG Load Regulation Spec Change : VNEG : 6mV → 0.19%/mA, VPOS : 5mV → 0.31%/mA Boost Current limit & RDS(ON) : Design Guaranteed
2015.01.27	1.0	Final Datasheet
2015.03.31	1.1	UVLO rising threshold voltage : 2.3V → 2.6V