

High Precision Hall Effect Latch for Consumer Applications

Hall Effect Latch

TLV4968-1T

TLV4968-1TA

TLV4968-1TB

TLV4968-1T

Data Sheet

Revision 1.0, 2015-05-18

Sense & Control

Table of Contents

1	Product Description	5
1.1	Overview	5
1.2	Features	5
1.3	Target Applications	5
2	Functional Description	6
2.1	General	6
2.2	Pin Configuration (top view)	6
2.3	Pin Description	6
2.4	Block Diagram	7
2.5	Functional Block Description	7
2.6	Default Start-up Behavior	9
3	Specification	10
3.1	Application Circuit	10
3.2	Absolute Maximum Ratings	11
3.3	Operating Range	12
3.4	Electrical and Magnetic Characteristics	12
4	Package Information	14
4.1	Package Outline	14
4.2	Packing Information	16
4.3	TO92S-3-2 Distance between Chip and Package	16
4.4	Package Marking	17
5	Revision History	18

List of Tables

Table 1	Ordering Information	5
Table 2	Pin Description	6
Table 3	Absolute Maximum Rating Parameters	11
Table 4	ESD Protection ($T_A = 25\text{ °C}$)	11
Table 5	Operating Conditions Parameters	12
Table 6	General Electrical Characteristics	12
Table 7	Magnetic Characteristics	13

List of Figures

Figure 1	Image of TLV4968-1T TO92S-3-1 TO92S-3-2	5
Figure 2	Pin Configuration and Center of Sensitive Area	6
Figure 3	Functional Block Diagram TLV4968-1T.....	7
Figure 4	TLV4968-1T	8
Figure 5	Output Signal TLV4968-1T.....	8
Figure 6	Illustration of the Start-up Behavior of the TLV4968-1T	9
Figure 7	Basic Application Circuit #1: Only Pull-Up Resistor is necessary	10
Figure 8	Enhanced Application Circuit #2 for extended ESD robustness	10
Figure 9	Definition of Magnetic Field Direction TO92S-3-2, TO92S-3-1.....	13
Figure 10	Package Outline TLV4968-1TA: TO92S-3-1 (All Dimensions in mm).....	14
Figure 11	Package Outline TLV4968-1TB: TO92S-3-2 (All Dimensions in mm).....	15
Figure 12	Packing of the TLV4968-1TB TO92S-3-2	16
Figure 13	Distance between Chip and Package	16
Figure 14	Marking of TLV4968-1T	17

Product Description

1 Product Description



1.1 Overview

Characteristic	Supply Voltage	Supply Current	Sensitivity	Interface	Temperature T_A
Bipolar Hall Effect Latch	3.0~26 V	1.6 mA	B_{OP} : 1 mT B_{RP} : -1 mT	Open Drain Output	-40 °C to 125 °C

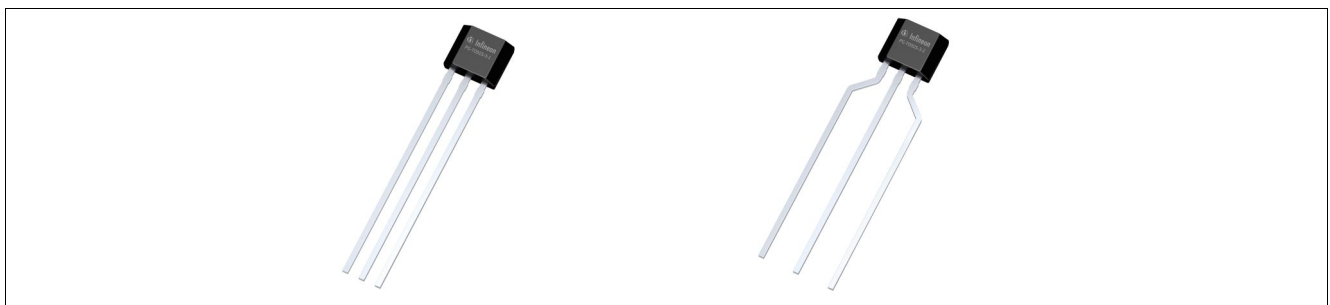


Figure 1 Image of TLV4968-1T TO92S-3-1 TO92S-3-2

1.2 Features

- 3.0 V to 26 V operating supply voltage
- Operation from unregulated power supply
- Output overcurrent & overtemperature protection
- Active error compensation
- High stability of magnetic thresholds
- High ESD performance
- Leaded, halogen-free package TO92S-3-1 for TLV4968-1TA, TO92S-3-2 for TLV4968-1TB

1.3 Target Applications

Target applications for the TLV496x Hall switch family are all applications which require a high precision Hall Latch with an operating temperature range from -40 °C to 125 °C.

The magnetic behavior as a latch and switching thresholds of typical ± 1 mT make the device especially suited for the use with a pole wheel for index counting applications, for rotor position detection as in brushless DC motor commutation and for white goods or open/closing detection.

For automotive applications please refer to the Infineon TLE Hall Switches series.

Table 1 Ordering Information

Product Name	Product Type	Ordering Code	Package
TLV4968-1TA	Hall Latch	SP001274788	TO92S-3-1 (Bulk)
TLV4968-1TB	Hall Latch	SP001283508	TO92S-3-2 (Ammo pack)

1) Only the package is halogen-free.

Functional Description

2 Functional Description

2.1 General

The TLV4968-1T is an integrated Hall effect designed specifically for highly accurate applications with superior supply voltage capability, and temperature stability of the magnetic thresholds.

2.2 Pin Configuration (top view)

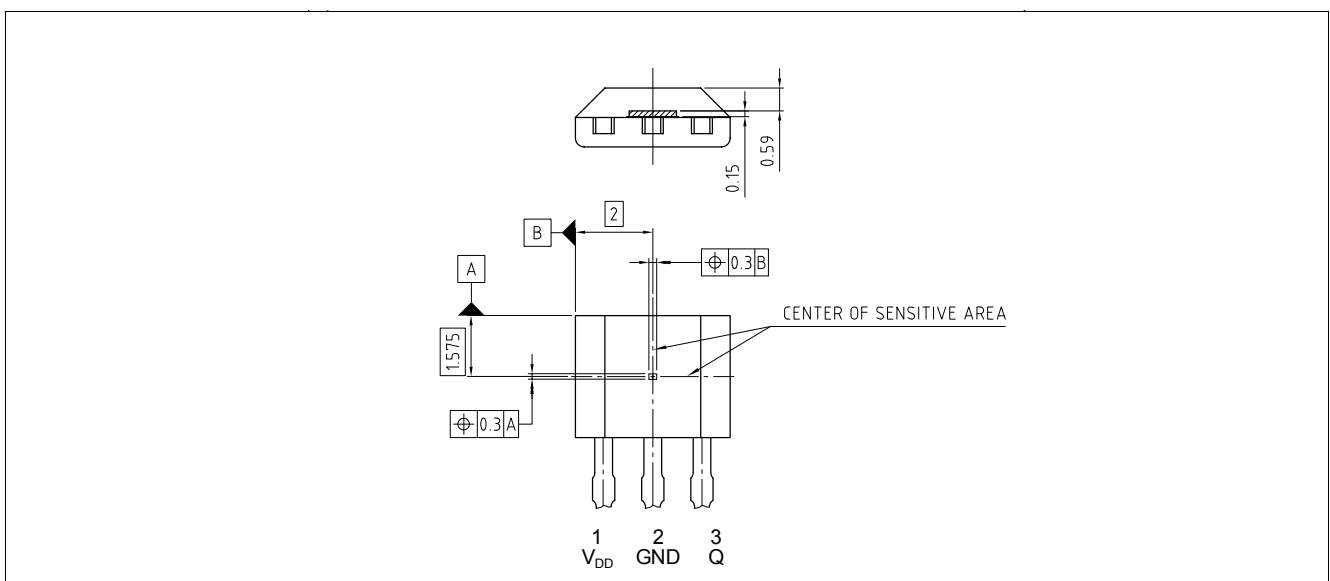


Figure 2 Pin Configuration and Center of Sensitive Area

2.3 Pin Description

Table 2 Pin Description

Pin No.	Symbol	Function
1	VDD	Supply voltage
2	GND	GND
3	Q	Output

Functional Description

2.4 Block Diagram

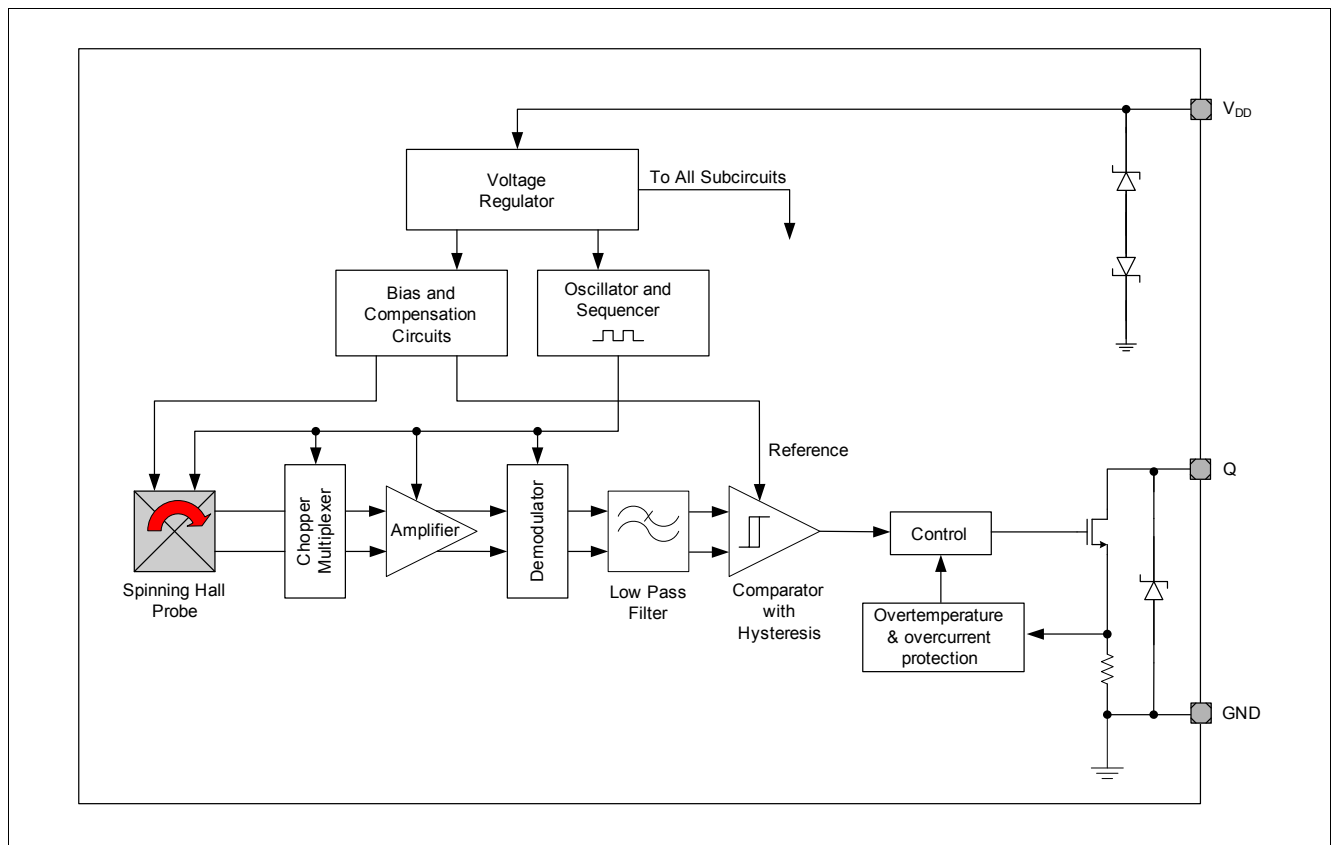


Figure 3 Functional Block Diagram TLV4968-1T

2.5 Functional Block Description

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

The output transistor has an integrated overcurrent and overtemperature protection.

Functional Description

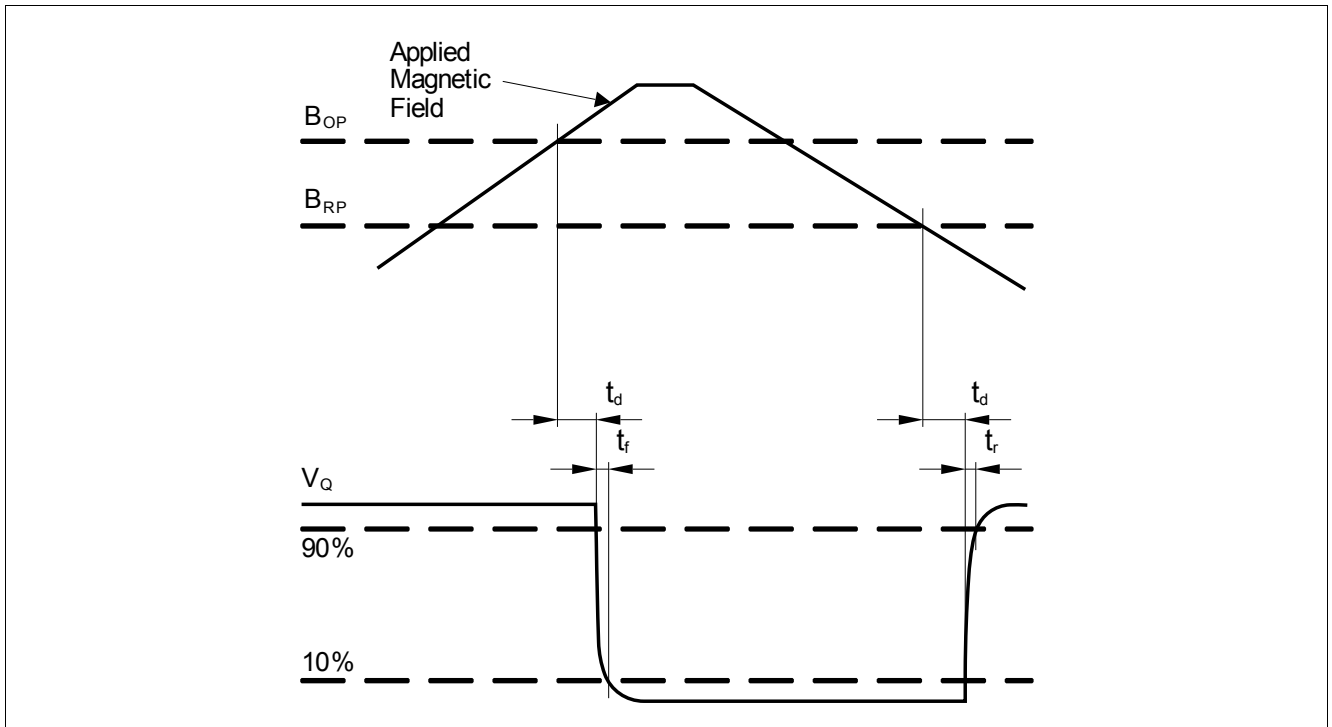


Figure 4 TLV4968-1T

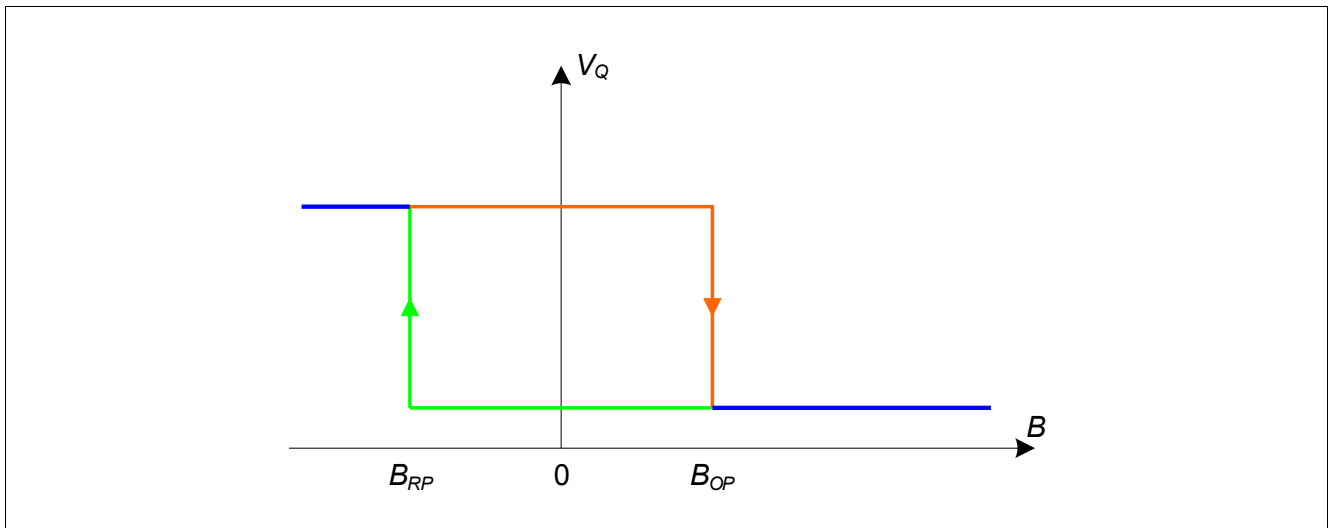


Figure 5 Output Signal TLV4968-1T

Functional Description

2.6 Default Start-up Behavior

The magnetic thresholds exhibit a hysteresis $B_{HYS} = B_{OP} - B_{RP}$. In case of a power-on with a magnetic field B within hysteresis ($B_{OP} > B > B_{RP}$) the output of the sensor is set to the pull up voltage level (V_Q) per default. After the first crossing of B_{OP} or B_{RP} of the magnetic field the internal decision logic is set to the corresponding magnetic input value.

V_{DDA} is the internal supply voltage which is following the external supply voltage V_{DD} .

This means for $B > B_{OP}$ the output is switching, for $B < B_{RP}$ and $B_{OP} > B > B_{RP}$ the output stays at V_Q .

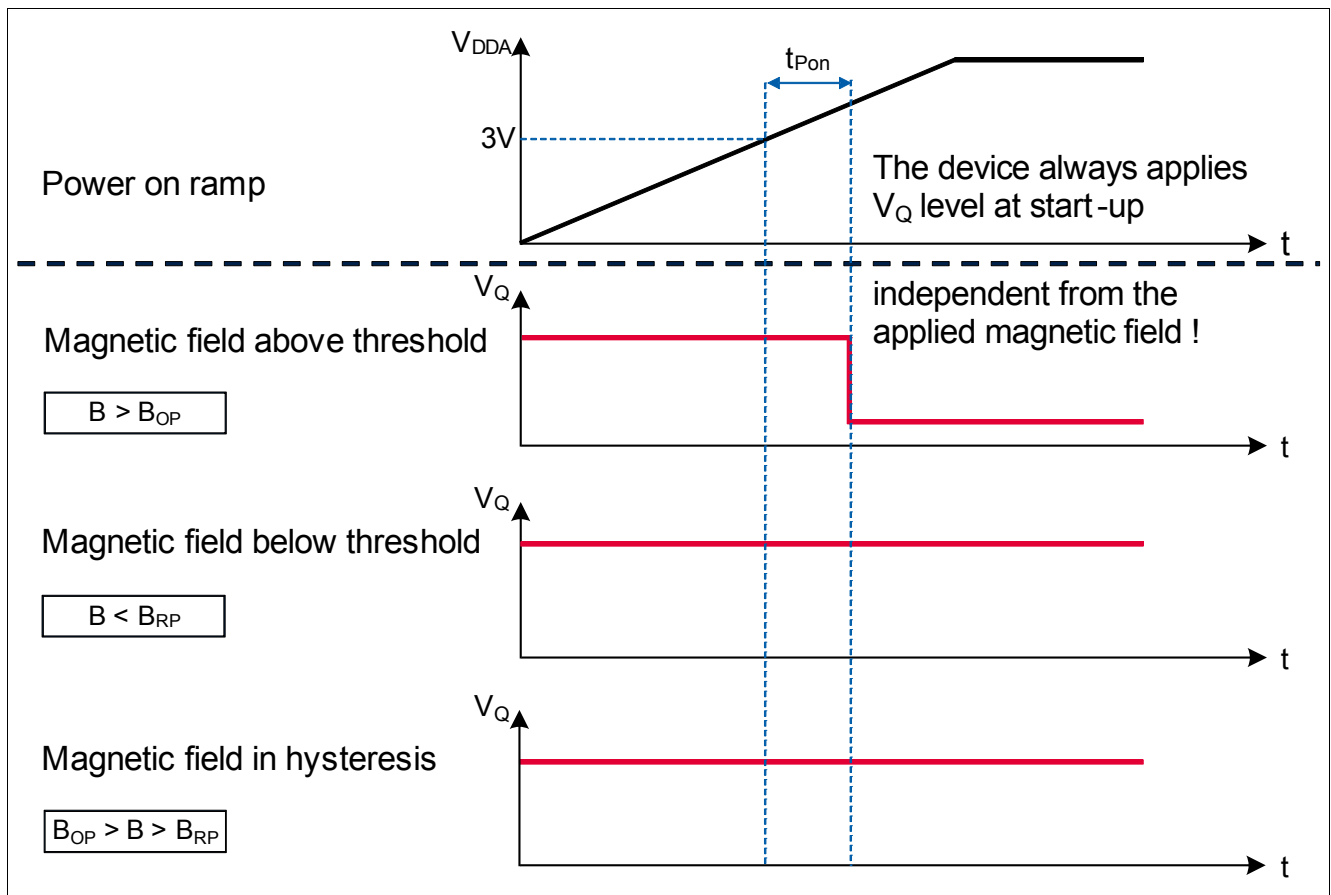


Figure 6 Illustration of the Start-up Behavior of the TLV4968-1T

Specification

3 Specification

3.1 Application Circuit

The following **Figure 7** shows the basic option of an application circuit. Only a pull-up resistor R_Q is necessary. The resistor R_Q has to be in a dimension to match the applied V_S to keep I_Q limited to the operating range of maximum 25 mA.

e.g.: $V_S = 12\text{ V}$; $I_Q = 12\text{ V}/1200\ \Omega = 10\text{ mA}$

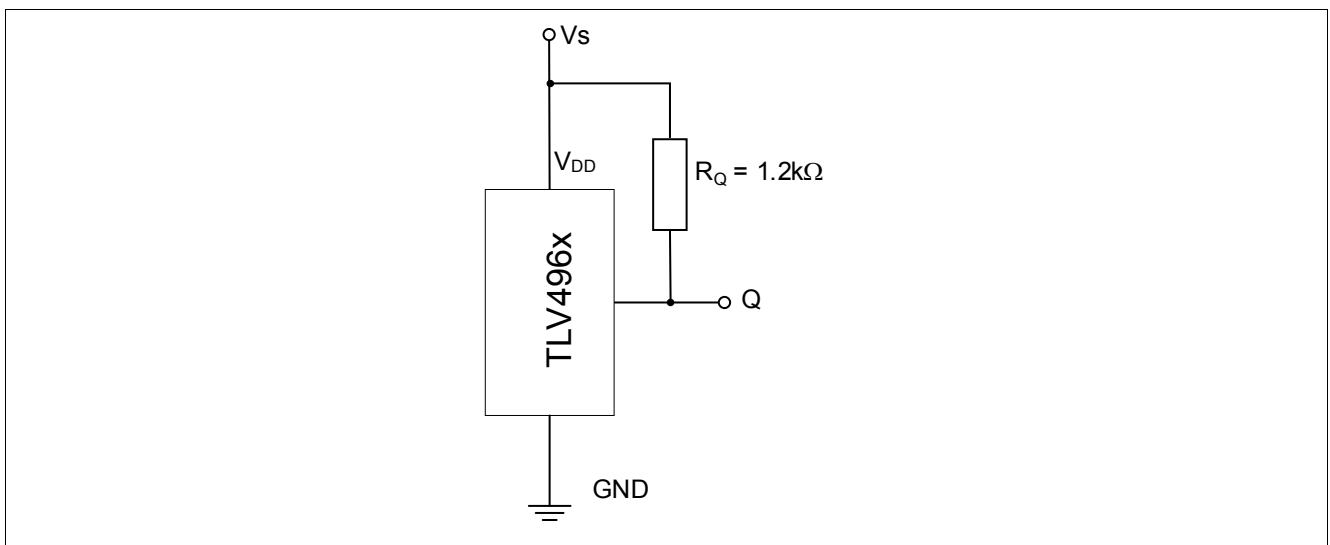


Figure 7 Basic Application Circuit #1: Only Pull-Up Resistor is necessary

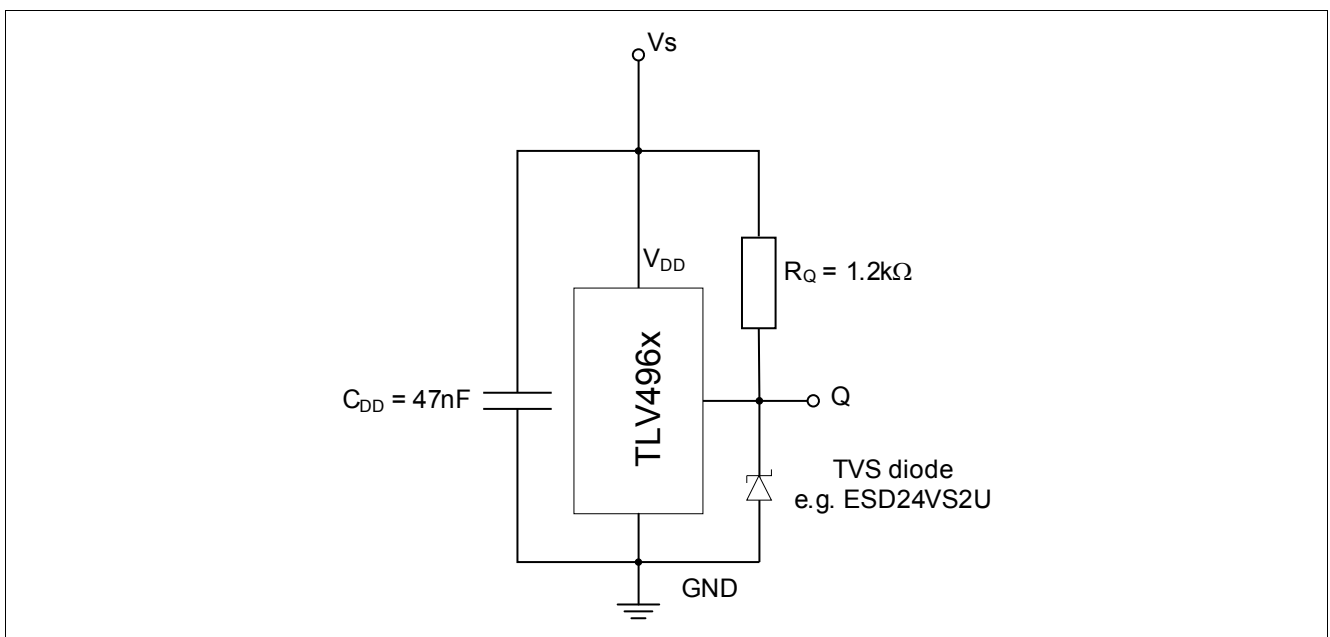


Figure 8 Enhanced Application Circuit #2 for extended ESD robustness

With an additional capacitor C_{DD} and a transient voltage suppression (TVS) diode an extended ESD robustness on system level is achieved (**Figure 8**).

Specification

3.2 Absolute Maximum Ratings

Table 3 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage ¹⁾	V_{DD}	3	–	26	V	–
Output voltage	V_Q	-0.5	–	26	V	–
Reverse output current	I_Q	-70	–	–	mA	–
Junction temperature ¹⁾	T_J	-40	–	150	°C	–
Storage temperature	T_S	-40	–	150	°C	–
Thermal resistance Junction ambient	R_{thJA}	–	–	250	K/W	for TO92S-3-2 (2s2p)

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Calculation of the dissipated power P_{DIS} and junction temperature T_J of the chip:

e.g. for: $V_{DD} = 12\text{ V}$, $I_S = 2.5\text{ mA}$, $V_{QSAT} = 0.5\text{ V}$, $I_Q = 20\text{ mA}$

Power dissipation: $P_{DIS} = 12\text{ V} \times 2.5\text{ mA} + 0.5\text{ V} \times 20\text{ mA} = 30\text{ mW} + 10\text{ mW} = 40\text{ mW}$

Temperature $\Delta T = R_{thJA} \times P_{DIS} = 250\text{ K/W} \times 40\text{ mW} = 10\text{ K}$

For $T_A = 50\text{ °C}$: $T_J = T_A + \Delta T = 50\text{ °C} + 10\text{ K} = 60\text{ °C}$

Table 4 ESD Protection¹⁾ ($T_A = 25\text{ °C}$)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ESD voltage (HBM) ²⁾	V_{ESD}	-4	–	4	kV	$R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$
ESD voltage (CDM) ³⁾	V_{ESD}	-1	–	1	kV	–

1) Characterization of ESD is carried out on a sample basis, not subject to production test.

2) Human Body Model (HBM) tests according to ANSI/ESDA/JEDEC JS-001.

3) Charge device model (CDM) tests according to JESD22-C101.

Specification

3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLV4968-1T.

All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

Table 5 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.0	–	26 ¹⁾	V	–
Output voltage	V_Q	3.0	–	26	V	–
Operation temperature	T_A	-40	–	125	°C	$R_{thJA} \leq 250K/W$
Output current	I_Q	0	–	25	mA	–

1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.

3.4 Electrical and Magnetic Characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to $V_{DD} = 12\text{ V}$ and $T_A = 25^\circ\text{C}$. The below listed specification is valid in combination with the application circuit shown in [Figure 7](#) and [Figure 8](#)

Table 6 General Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply current	I_S	1.1	1.6	2.5	mA	–
Output current limitation	I_{QLIMIT}	30	56	70	mA	internally limited & thermal shutdown
Output fall time ¹⁾	t_f	0.17	0.4	1	μs	1.2 k Ω / 50 pF, see Figure 4
Output rise time ¹⁾	t_r	0.4	0.5	1	μs	1.2 k Ω / 50 pF, see Figure 4
Delay time ¹⁾²⁾	t_d	12	15	30	μs	see Figure 4
Power-on time ¹⁾³⁾	t_{PON}	–	80	150	μs	$V_{DD} = 3\text{ V}$, $B \leq B_{RP} - 0.5\text{ mT}$ or $B \geq B_{OP} + 0.5\text{ mT}$

1) Not subject to production test, verified by design/characterization.

2) Systematic delay between magnetic threshold reached and output switching.

3) Time from applying $V_{DD} = 3.0\text{ V}$ to the sensor until the output is valid.

Specification

Table 7 Magnetic Characteristics

Parameter	Symbol	T (°C)	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Operating point	B_{OP}	-40	-0.3	1.1	2.3	mT	-
		25	-0.4	1.0	2.3	mT	-
		125	-0.4	0.9	2.1	mT	-
Release point	B_{RP}	-40	-2.3	-1.1	0.3	mT	-
		25	-2.3	-1.0	0.4	mT	-
		125	-2.1	-0.9	0.4	mT	-
Hysteresis	B_{HYS}	-40	1.2	2.1	3.1	mT	-
		25	1.1	2.0	2.9	mT	-
		125	1.0	1.8	2.7	mT	-
Temperature compensation of magnetic thresholds ¹⁾	T_C	-	-	-1000	-	ppm/K	-

1) Not subject to production test, verified by design/characterization.

Field Direction Definition

Positive magnetic fields are defined with the south pole of the magnet to the branded side of package.

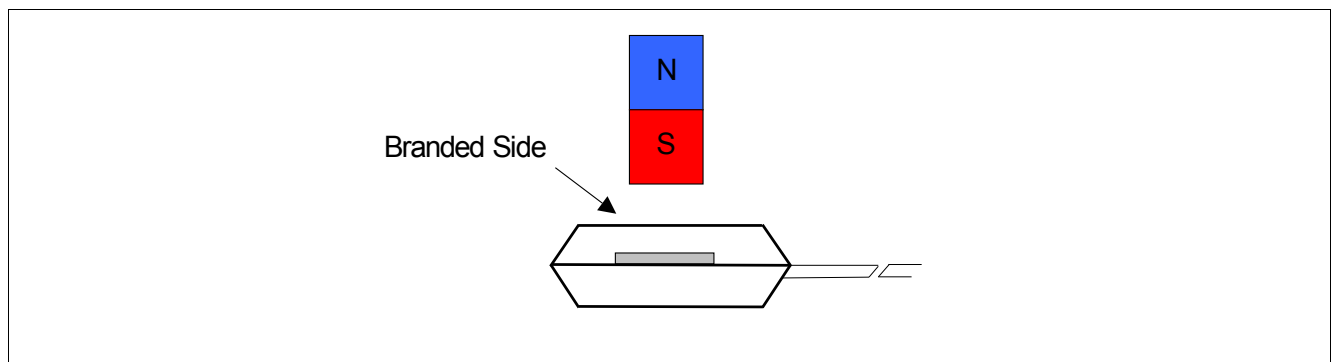


Figure 9 Definition of Magnetic Field Direction T092S-3-2, T092S-3-1

Package Information

4 Package Information

The TLV4968-1TA is available in Bulk packing with TO92S-3-1-package.

The TLV4968-1TB is available in AMMO packing with TO92S-3-2-package.

4.1 Package Outline

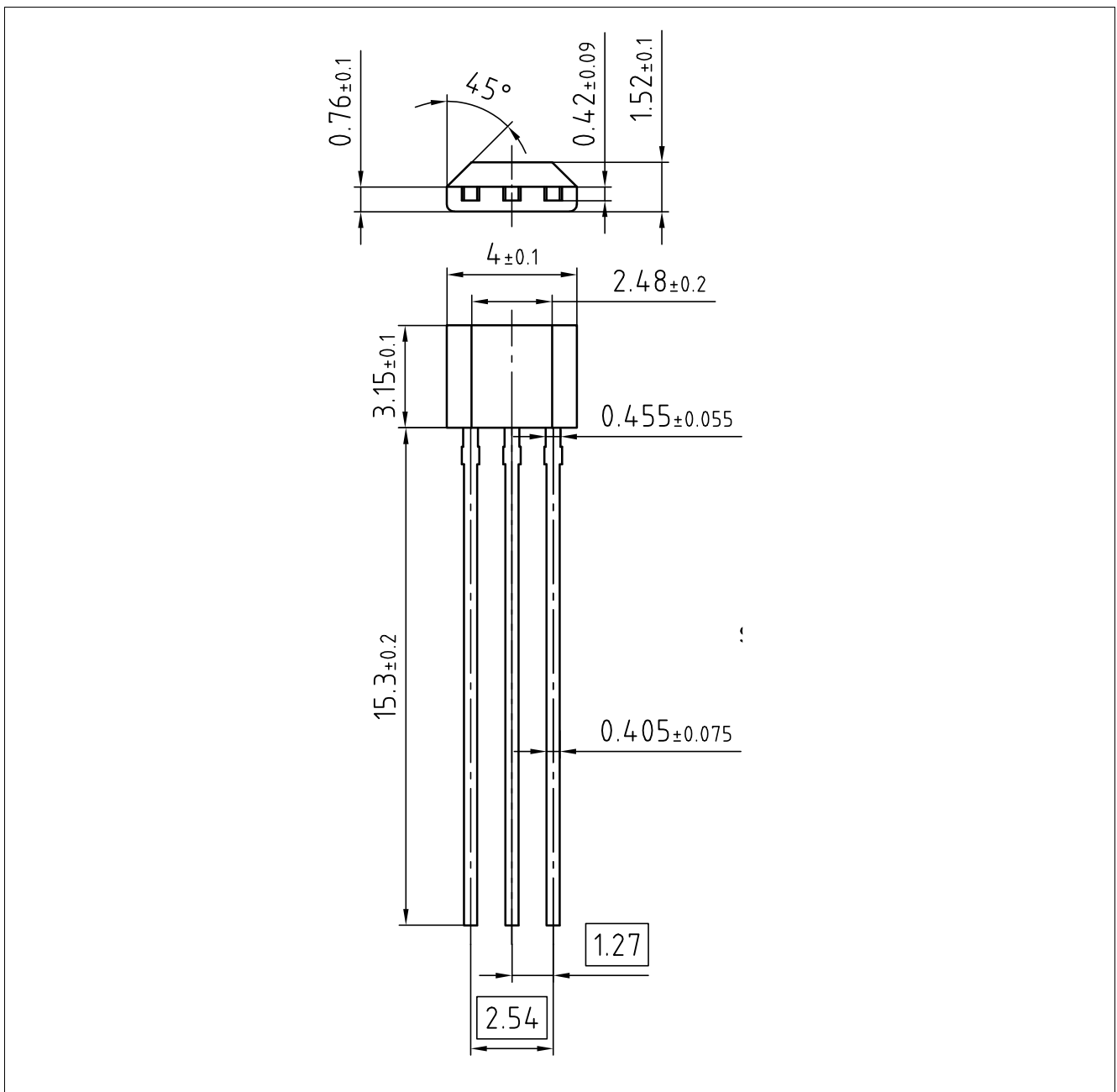


Figure 10 Package Outline TLV4968-1TA: TO92S-3-1 (All Dimensions in mm)

Package Information

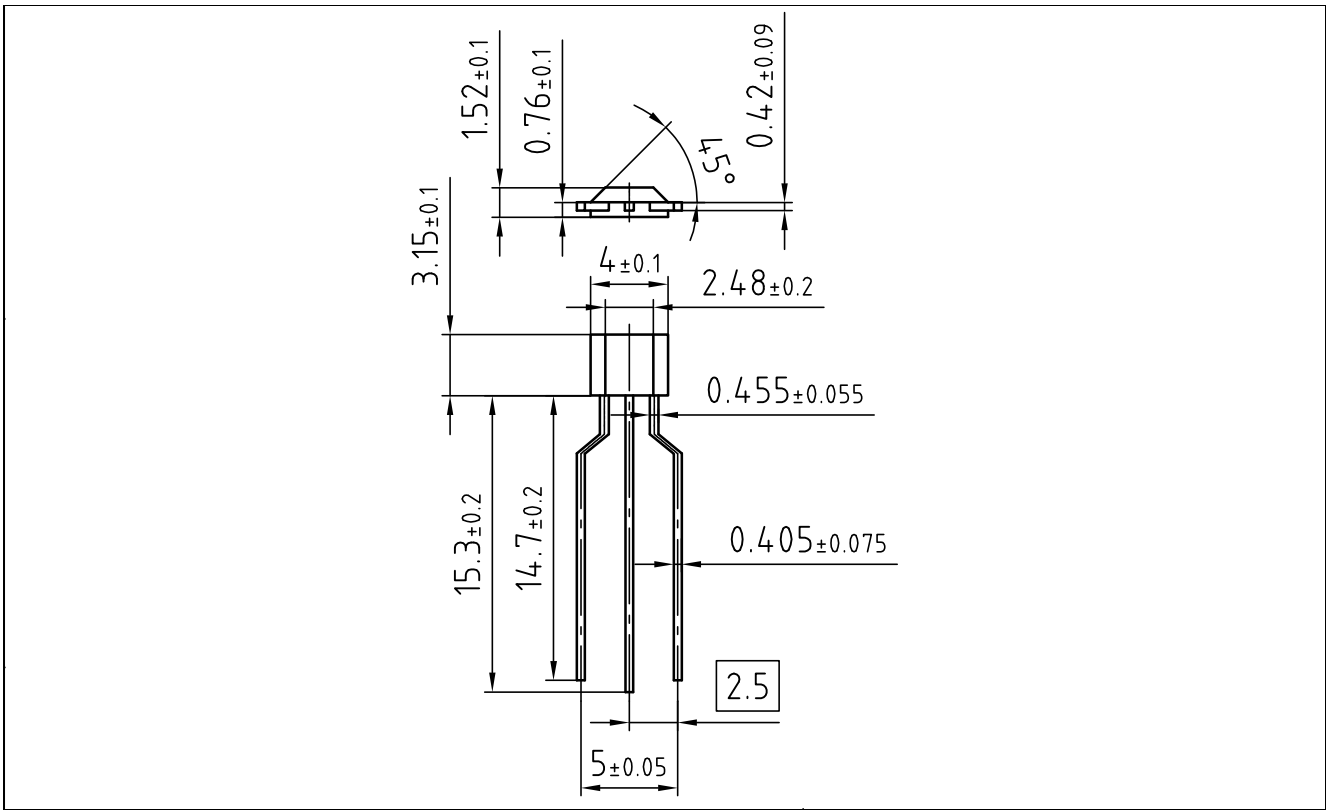


Figure 11 Package Outline TLV4968-1TB: TO92S-3-2 (All Dimensions in mm)

Package Information

4.4 Package Marking

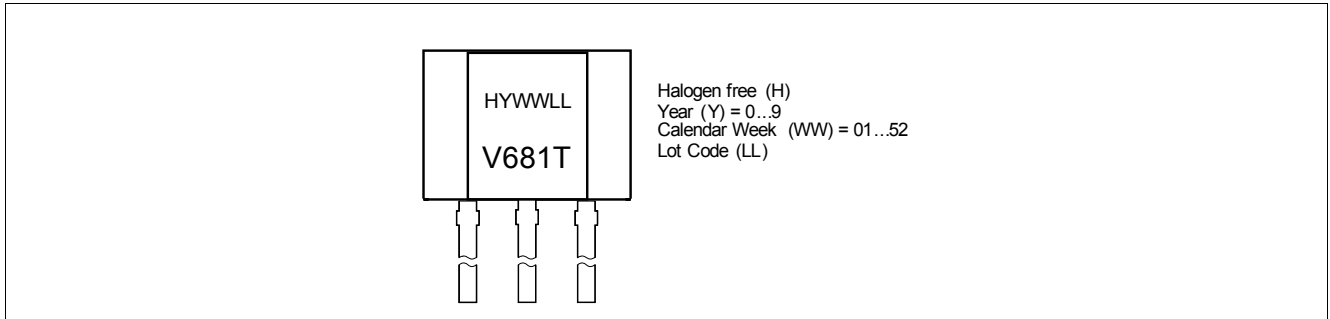


Figure 14 Marking of TLV4968-1T

Revision History**5 Revision History**

Revision	Date	Changes
1.0	2015-05-18	Initial release.

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolMOS™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EconoPACK™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I²RF™, ISOFACE™, IsoPACK™, LITIX™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOS™, SmartLEWIS™, SPOC™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, µVision™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2011-11-11

www.infineon.com

Edition 2015-05-18

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2014 Infineon Technologies AG.

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.