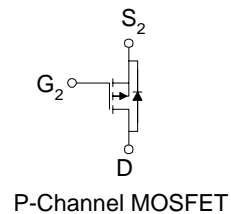
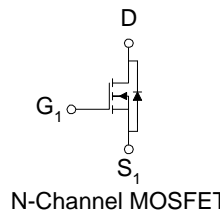
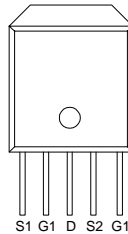


P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	45 @ $V_{GS} = 2.5V$	29
	35 @ $V_{GS} = 4.5V$	36
-26.5	70 @ $V_{GS} = -2.5V$	-20
	52 @ $V_{GS} = -4.5V$	-26

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-26.5	V
Gate-Source Voltage		V_{GS}	± 12	± 12	
Continuous Drain Current ^a	$T_A = 25^\circ C$	I_D	36	-26	A
	$T_A = 70^\circ C$		30	-21	
Pulsed Drain Current ^b		I_{DM}	40	-40	
Continuous Source Current (Diode Conduction) ^a		I_S	30	-30	A
Power Dissipation ^a	$T_A = 25^\circ C$	P_D	50	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175		$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	0.6			V
		V _{GS} = V _{DS} , I _D = -250 uA	P	-0.6			
Gate-Body Leakage	I _{GSS}	V _{GS} = -12 V, V _{DS} = 0 V	P			±100	nA
		V _{GS} = 12 V, V _{DS} = 0 V	N			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V	P			-1	uA
		V _{DS} = 24 V, V _{GS} = 0 V	N			1	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	N	20			A
		V _{DS} = -5 V, V _{GS} = -4.5 V	P	-20			
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 6.9 A	N			35	mΩ
		V _{GS} = 2.5 V, I _D = 6 A				45	
		V _{GS} = -4.5 V, I _D = -5.2 A	P			52	
		V _{GS} = -2.5 V, I _D = -4.2 A				70	
Forward Transconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 6.9 A	N		25		S
		V _{DS} = -15 V, I _D = -5.2 A	P		10		
Dynamic							
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =4.5V, I _D =6.9A P-Channel V _{DS} =-15V, V _{GS} =-4.5V, I _D =-5.2A	N		6.0		nC
			P		25		
Gate-Source Charge	Q _{gs}		N		1.0		
			P		2.4		
Gate-Drain Charge	Q _{gd}		N		1.5		
			P		3.9		
Turn-On Delay Time	t _{d(on)}	N-Chaneel V _{DD} =15V, V _{GS} =4.5V, I _D =1A , R _{GEN} =6Ω, P-Channel V _{DD} =-15V, V _{GS} =-4.5V, I _D =-1A R _{GEN} =6Ω	N		7.4		nS
			P		7.6		
Rise Time	t _r		N		4		
			P		6.8		
Turn-Off Delay Time	t _{d(off)}		N		22.2		
			P		33.6		
Fall-Time	t _f		N		3.6		
			P		23.2		

Notes

- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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