Initial Release

High Speed ±100V 2A Integrated Ultrasound Pulser

Features

- HVCMOS technology for high performance
- 0 to ±100V output voltage
- ±2A source and sink current
- Built-in damping for RTZ waveform capability
- Gate-clamp for quick output amplitude ramping
- Up to 40MHz operation frequency
- ±3ns matched delay times
- Second harmonic is less than -40dB
- 1.8V to 3.3V CMOS logic interface
- 7x7 thermally-enhanced 44-lead QFN MCM

Application

- Medical ultrasound imaging

General Description

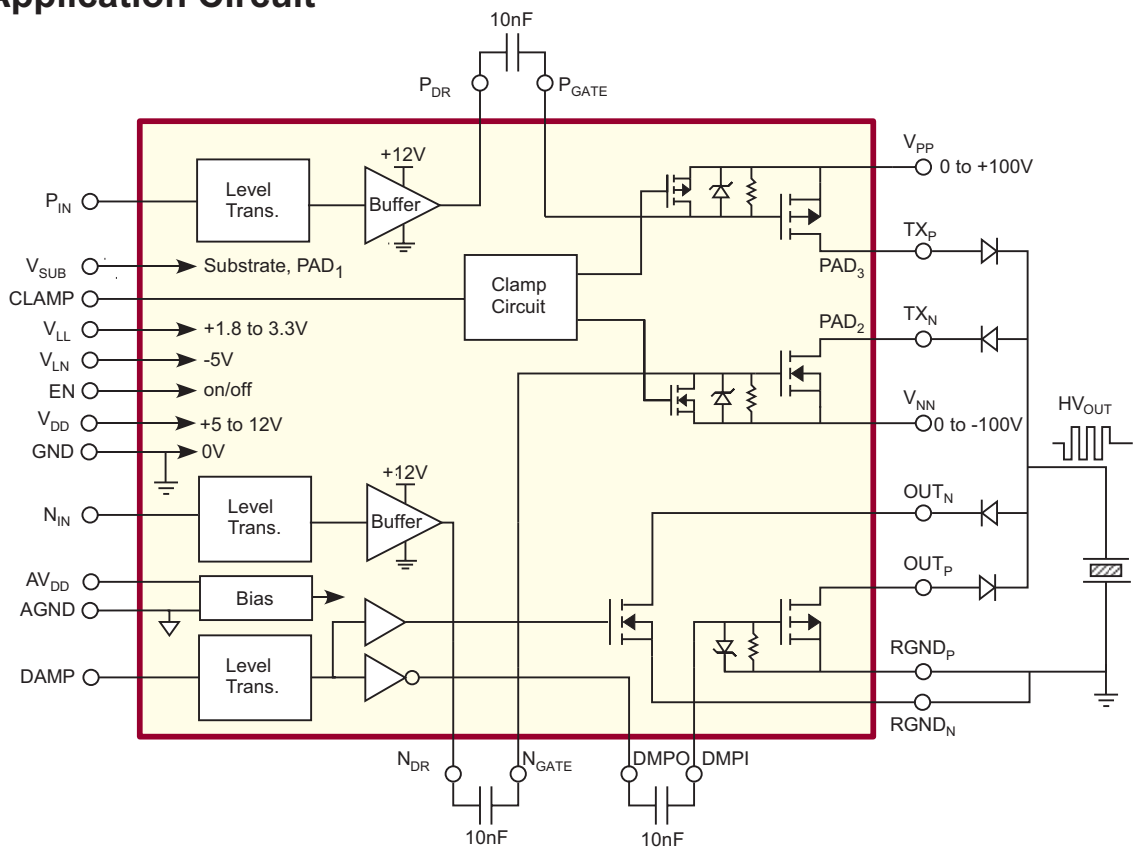
The Supertex HV732 is a single, complete, high-voltage, high-speed, ultrasound transmitter pulser. It is designed for medical ultrasound imaging applications.

The HV732 has built-in damping for faster RTZ waveform capability and high voltage MOSFET gate-clamping function for quick ramping of the output voltage amplitude.

The HV732 consists of a control logic circuit, level translators, MOSFET gate drive buffers, clamp circuits, and high current, high voltage MOSFETs as the ultrasound transmitter pulser output stage.

In the output stage there are two pairs of MOSFETs. Each pair consists of a P-channel and an N-channel MOSFET. They are designed to have the same impedance, and can provide peak currents of over ±2 amps. The built-in MOSFET gate driver outputs swing 0 to 12V on P_{DR} and N_{DR} pins. The P-channel damp output swings 0 to –5V on the DMPO pin.

Typical Application Circuit



NR040506

Ordering Information

Device	Package Options	
	44-Lead QFN	
HV732	HV732K6	HV732K6-G

-G indicates package is RoHS compliant ('Green')

Power-Up Sequence

1	V_{PP} and V_{SUB}
2	V_{NN}
3	V_{LN}
4	V_{DD}
5	V_{LL}

Absolute Maximum Ratings

Parameter	Value
V_{LL}, logic supply	-0.5V to +5.5V
V_{DD}, positive gate drive supply	-0.5V to +15V
AV_{DD}, positive gate drive supply	-0.5V to +15V
V_{LN}, Negative gate drive supply	-5.5V to +0.5V
V_{PP}-V_{NN}, differential high voltage supply	+220V
V_{PP}, high voltage positive supply	-0.5V to +200V
V_{NN}, high voltage negative supply	+0.5V to -200V
Storage temperature	-65°C to 150°C
Thermal enhanced package power dissipation	1.5W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Operating Supply Voltages and Current

(Over recommended operating conditions unless otherwise specified: $AV_{DD} = V_{DD} = 12V$, $V_{LL} = 3.3V$, $V_{LN} = -5V$, $T_A = 25°C$)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{LL}	Logic supply	1.8	3.3	3.6	V	---
AV_{DD}	Positive analog supply	9.0	-	12.6	V	---
V_{DD}	Positive drive supply	9.0	-	12.6	V	---
V_{PP}	High voltage positive supply for $HV_{OUT}P1$	0	-	100	V	---
V_{NN}	High voltage negative supply for $HV_{OUT}N1$	-100	-	0	V	---
V_{LN}	High voltage negative supply for $HV_{OUT}N2$	-4.75	-5.0	-5.25	V	---
V_{SUB}	High voltage positive supply for to bias substrate	-	-	100	V	Need to be the most positive supply on the device
I_{DDQ}	V_{DD} current EN = Low	-	175	290	µA	---
I_{DDEN}	V_{DD} current EN = High	-	1.7	2.8	mA	$P_{IN} = N_{IN}$ = Low
I_{DDEN}	V_{DD} current at 5MHz PW	-	7.5	-	mA	f = 5.0MHz, PW D% = 1.0% No cap on P_{DR}, N_{DR}
I_{PPQ}	V_{DD} current EN = Low	-	2.0	5.0	µA	V_{PP} = +100V, V_{NN} = -100V
I_{PPEN}	V_{DD} current EN = High	-	140	180	µA	$P_{IN} = N_{IN}$ = Low, V_{PP} = +100V, V_{NN} = -100V
I_{NNQ}	V_{DD} current EN = Low	-	-1.0	-3.0	µA	V_{PP} = +100V, V_{NN} = -100V

Operating Supply Voltages and Current (cont.)

(Over recommended operating conditions unless otherwise specified: $AV_{DD} = V_{DD} = 12V$, $V_{LL} = 3.3V$, $V_{LN} = -5V$, $T_A = 25°C$)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{NNEN}	V_{DD} current EN = High	-	-140	-180	µA	$P_{IN} = N_{IN}$ = Low, V_{PP} = +100V, V_{NN} = -100V
I_{LLQ}	V_{DD} current EN = Low	-	1.0	5.0	µA	---
I_{LLEN}	V_{DD} current EN = High	-	16	25	µA	$P_{IN} = N_{IN}$ = Low
I_{LNQ}	V_{DD} current EN = Low	-	-1.0	-5.0	µA	---
I_{LNEN}	V_{DD} current EN = High	-	-230	-320	µA	$P_{IN} = N_{IN}$ = Low

DC Electrical Characteristics

(Over recommended operating conditions unless otherwise specified: $AV_{DD} = V_{DD} = 12V$, $V_{LL} = 3.3V$, $V_{LN} = -5V$, $T_A = 25°C$)

Output P-Channel MOSFET, TX_P

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	-2.0	-	-	A	V_{GS} = -10V, V_{DS} = -25V
R_{ON}	Channel resistance	-	-	8	Ω	V_{GS} = -10V, I_{DS} = -1.0A
R_{GS}	Gate to source resistor	10	-	50	KΩ	I_{GS} = -100µA
V_{GS}	Source to gate zener voltage	-13.2	-	-25	V	I_{GS} = -2.0µA
V_{GSF}	Gate zener forward voltage	-0.5	-	-0.8	V	---
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	I_{DS} = -1.0mA
C_{ISS}	Input capacitance	-	-	200	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1Mhz
C_{OSS}	Output capacitance	-	25	55	pF	

Output N-Channel MOSFET, TX_N

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	2.0	-	-	A	V_{GS} = -10V, V_{DS} = -25V
R_{ON}	Channel resistance		-	7.0	Ω	V_{GS} = -10V, I_{DS} = -1.0A
R_{GS}	Gate to source resistor	10	-	50	KΩ	I_{GS} = -100µA
V_{GS}	Source to gate zener voltage	13.2	-	25	V	I_{GS} = -2.0µA
V_{GSF}	Gate zener forward voltage	0.5	-	0.8	V	---
$V_{GS(th)}$	Gate threshold voltage	1.0	-	2.0	V	I_{DS} = -1.0mA
C_{ISS}	Input capacitance	-	-	110	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1Mhz
C_{OSS}	Output capacitance	-	28	60	pF	

Output P-Channel Damp MOSFET, OUT_P

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	-	-1.0	-	A	V_{GS} = -10V, V_{DS} = -25V
R_{ON}	Channel resistance	-	-	30	Ω	V_{GS} = -10V, I_{DS} = -1.0A
R_{GS}	Gate to source resistor	-	75	100	KΩ	I_{GS} = -100µA
V_{GS}	Source to gate zener voltage	-13.2	-	-25	V	I_{GS} = -2.0µA
V_{GSF}	Gate zener forward voltage	0.5	-	0.8	V	---
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.6	V	I_{DS} = -1.0mA
C_{ISS}	Input capacitance	-	-	200	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1Mhz
C_{OSS}	Output capacitance	-	-	60	pF	

Output N-Channel Damp MOSFET, OUT_N

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	1.0	-	-	A	V_{GS} = 10V, V_{DS} = 25V
R_{ON}	Channel resistance	-	-	22	Ω	V_{GS} = 10V, I_{DS} = 0.5A
V_{GS}	Source to gate zener voltage	1.0	-	2.6	V	I_{DS} = 1.0µA
C_{ISS}	Input capacitance	-	-	110	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1Mhz
C_{OSS}	Output capacitance	-	-	60	pF	

P-Channel Gate Driver Output, P_{DR}

Symbol	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance	-	10	15	Ω	I_{PDR} = 100mA
R_{SOURCE}	Output source resistance	-	8.0	13	Ω	I_{PDR} = -100mA
I_{PDR}	Peak output sink current	-	2.0	-	A	---
I_{PDR}	Peak output source current	-	-2.0	-	A	---

N-Channel Gate Driver Output, N_{DR}

Symbol	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance	-	8.0	13	Ω	I_{NDR} = 100mA
R_{SOURCE}	Output source resistance	-	9.0	14	Ω	I_{NDR} = -100mA
I_{NDR}	Peak output sink current	-	1.0	-	A	---
I_{NDR}	Peak output source current	-	-1.0	-	A	---

P-Channel Gate Driver Output, DMPO

Symbol	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance	-	26	30	Ω	I_{DMPO} = 100mA
R_{SOURCE}	Output source resistance	-	15	30	Ω	I_{DMPO} = -100mA
I_{DMPO}	Peak output sink current	-	0.3	-	A	---
I_{DMPO}	Peak output source current	-	-0.3	-	A	---

P-Channel Gate Clamp MOSFET

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	-	100	-	A	---
R_{ON}	Channel resistance	-	60	80	Ω	---
C_{OSS}	Output capacitance	-	40	-	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1Mhz

N-Channel Gate Clamp MOSFET

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	-	50	-	A	---
R_{ON}	Channel resistance	-	25	50	Ω	---
C_{OSS}	Output capacitance	-	40	-	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1Mhz

Logic Inputs

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{irf}	Inputs rise and fall time	-	-	10	ns	Logic input edge speed requirement
V_{IH}	Input logic high voltage	$0.8V_{LL}$	-	V_{LL}	V	---
V_{IL}	Input logic low voltage	0	-	$0.2V_{LL}$	V	---
I_{IH}	Input logic high current	-	-	1.0	µA	---
I_{IL}	Input logic low current	-1.0	-	-	µA	---

AC Electrical Characteristics

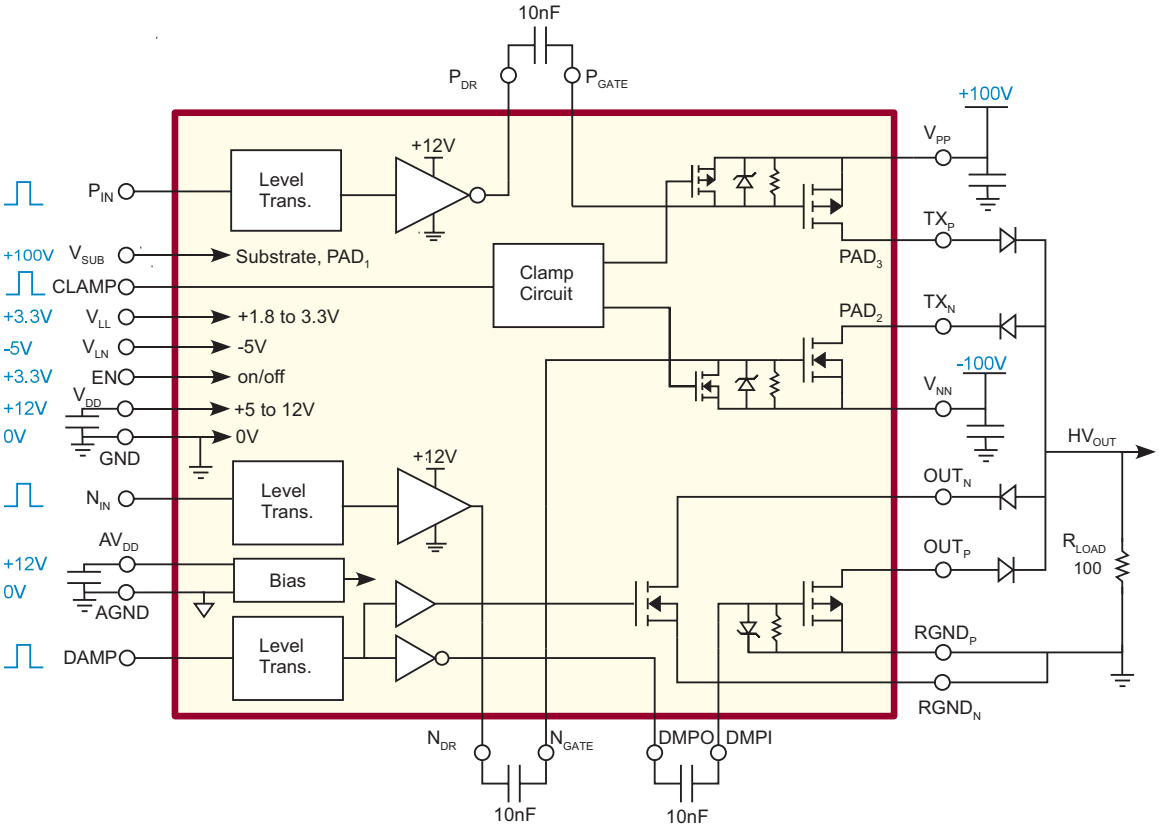
(Over recommended operating conditions unless otherwise specified: $AV_{DD} = V_{DD} = 12V$, $V_{LL} = 3.3V$, $V_{LN} = -5V$, $T_A = 25°C$)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{out}	Output frequency range	-	-	40	MHz	See test curcuit and timing diagram
tr	Output rise time	-	10	-	ns	See relevant test circuit and timing diagram. Load = 1.0kΩ/220pF
tf	Output fall time	-	10	-	ns	
tdr	Delay time on rise time	-	12	-	ns	
tdf	Delay time on fall time	-	12	-	ns	
Δt_{delay}	Delay time matching	-	-	±3.0	ns	From device to device
HD2	Second harmonic distortion	-	-40	-	dB	100Ω resistor load
t_{jitter}	Output jitter	-	80	-	ps	Standard deviation of t_d samples (1k)
t_{EN}	Enable time	-	30	50	µs	See timing diagram
$t_{DMPON(P)}$	Damp switch on delay (P)	-	17	22	ns	OUT_P 50Ω to -15V, 10nF from DMPO to DMPI. See timing diagram.
$t_{DMPOFF(P)}$	Damp switch off delay (P)	-	20	26	ns	
$t_{DMPON(N)}$	Damp switch on delay (N)	-	13	17	ns	OUT_N 50Ω to +15V. See timing diagram.
$t_{DMPOFF(N)}$	Damp switch off delay (N)	-	13	17	ns	
$t_{CLPON(P)}$	Clamp switch on delay (P)	-	430	1000	ns	P_{GATE} 75Ω to 0V, 10nF to P_{DR}, V_{PP} = +12V. See timing diagram.
$t_{CLPOFF(P)}$	Clamp switch off delay (P)	-	490	1000	ns	
$t_{CLPON(N)}$	Clamp switch on delay (N)	-	330	550	ns	N_{GATE} 75Ω to 0V, 10nF to N_{DR}, V_{NN} = -12V. See timing diagram.
$t_{CLPOFF(N)}$	Clamp switch off delay (N)	-	316	500	ns	
t_{PWRUP}	Device power-up delay	-	150	200	µs	All power supplies up and stable

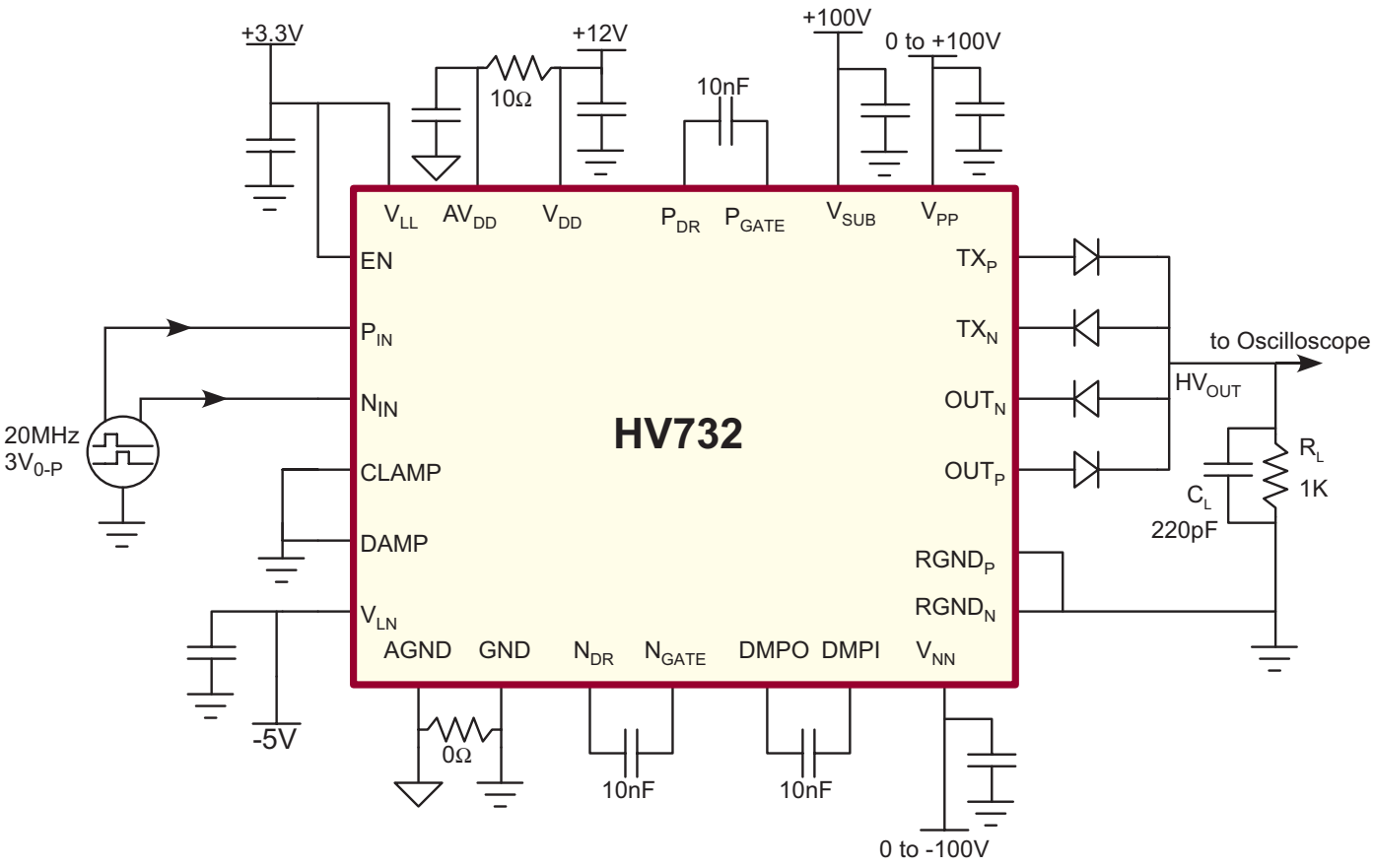
Truth Table

Logic Control Inputs					Gate Drive Output			HV Output		Damp Output	
EN	P_{IN}	N_{IN}	CLAMP	DAMP	P_{DR}	N_{DR}	DMPO	TX_P	TX_N	OUT_P	OUT_N
1	0	0	0	0	H	L	H	OFF	OFF	OFF	OFF
1	**1**	0	0	0	**L**	L	H	**ON**	OFF	OFF	OFF
1	0	**1**	0	0	H	**H**	H	OFF	**ON**	OFF	OFF
1	**X**	**X**	**1**	0	H	L	H	OFF	OFF	OFF	OFF
1	0	0	0	**1**	H	L	**L**	OFF	OFF	**ON**	**ON**
0	X	X	X	X	H	L	H	OFF	OFF	OFF	OFF

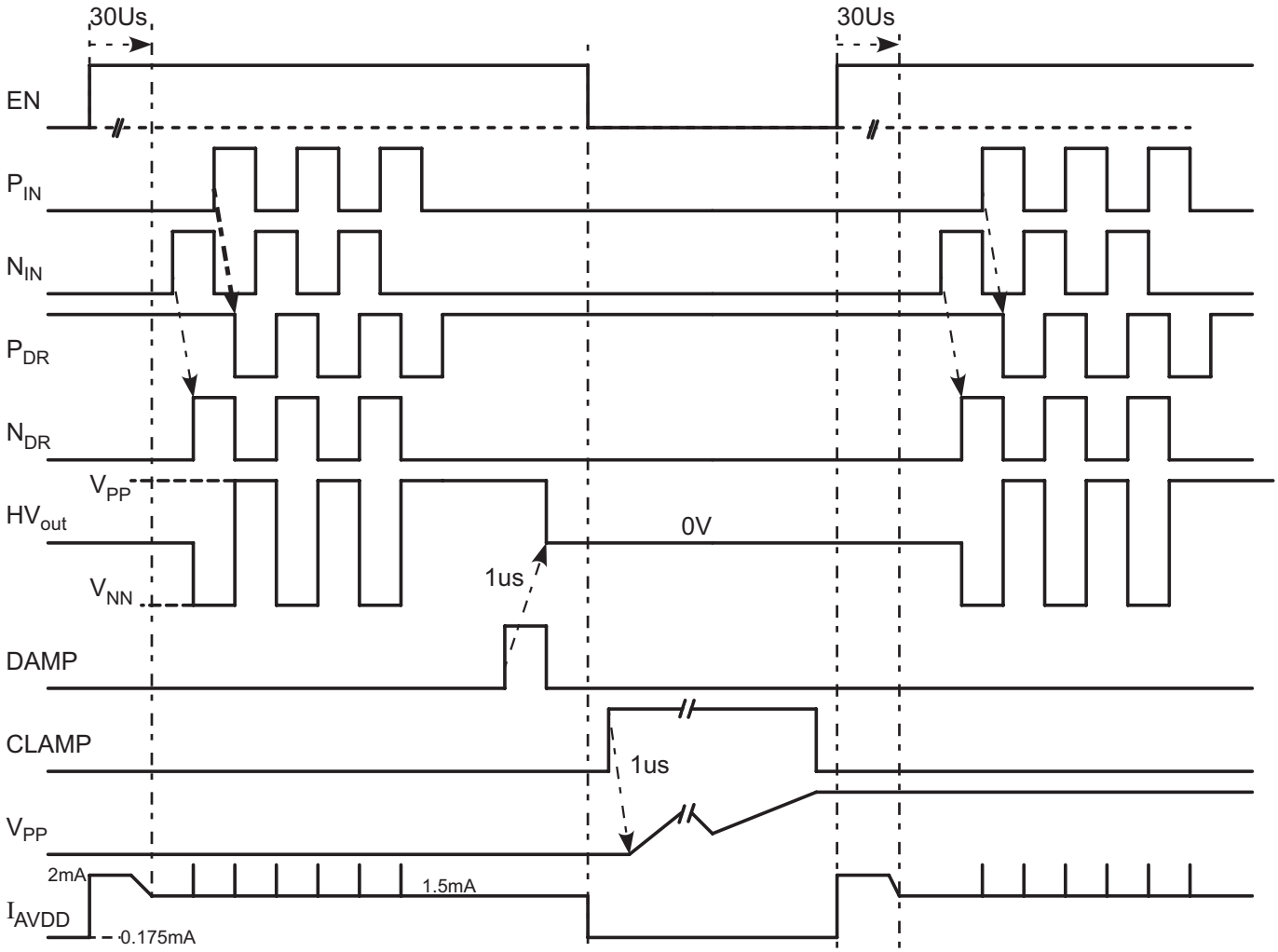
HV732 Test Circuit



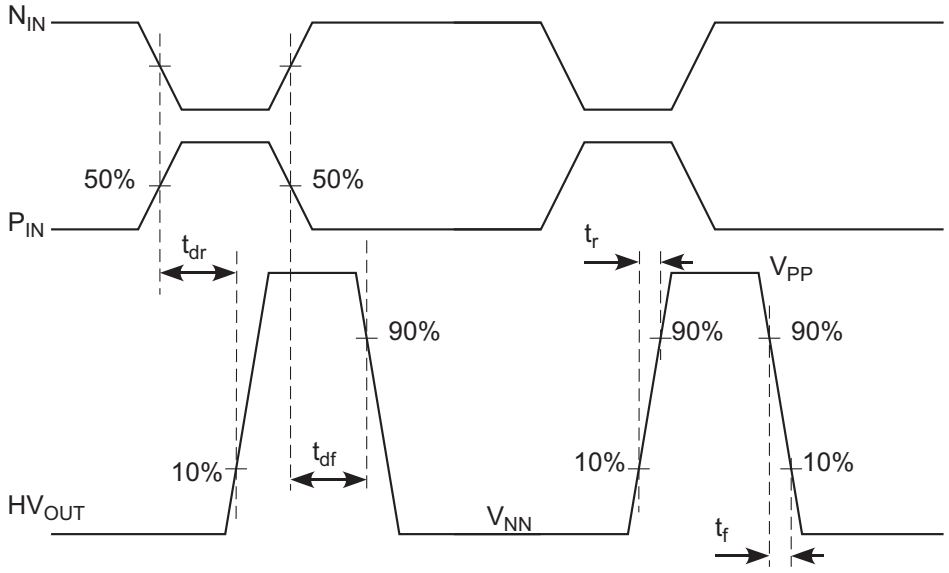
HV732 TX Switching Time Test



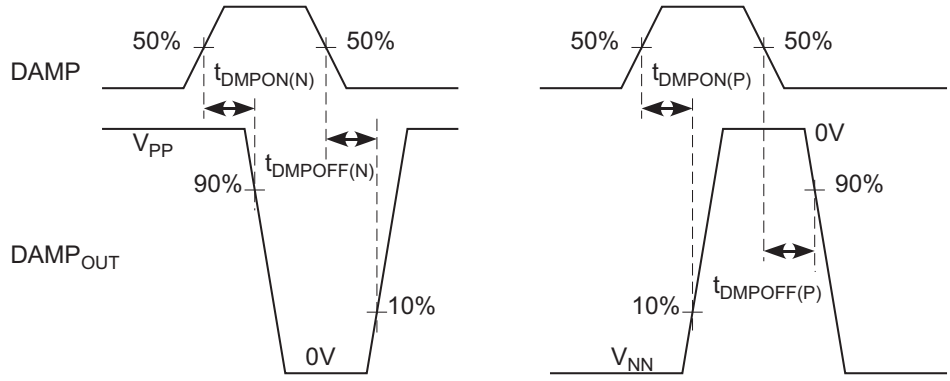
HV732 Timing Diagram



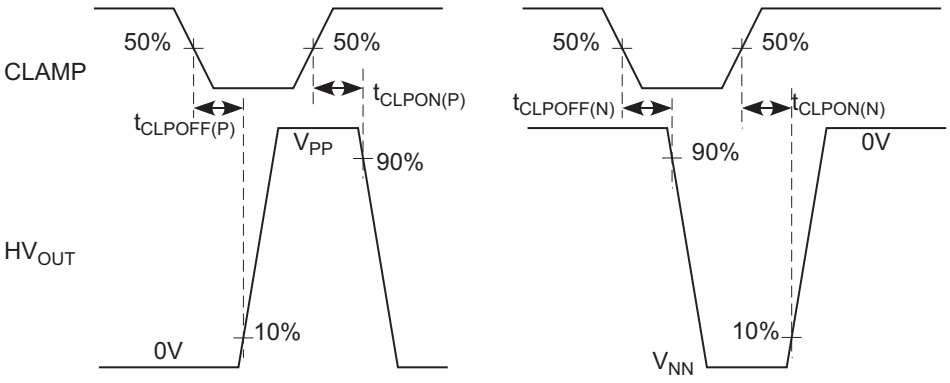
HV732 TX Switching Time Diagram



HV732 DAMP Switching Time Diagram



HV732 Clamp Switching Time Diagram

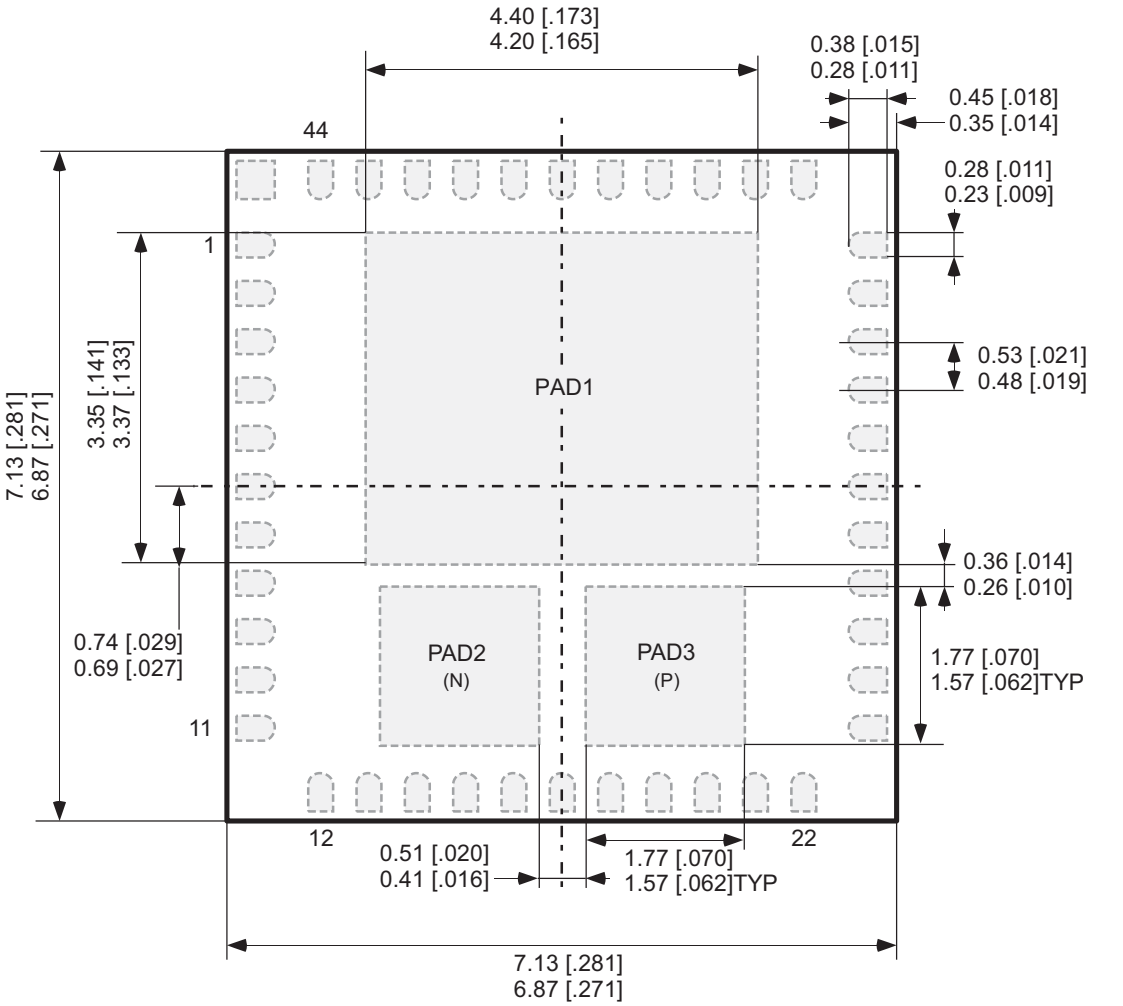


Pin Description

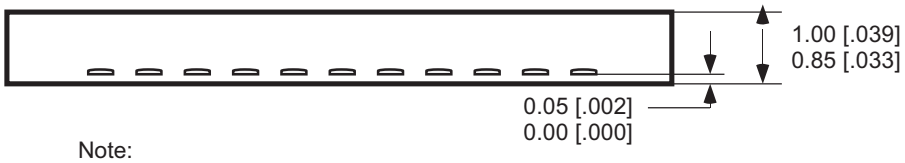
Pin	Function	Description
1	DMPO	Output of low voltage drive buffer for P-channel damp, 10nF external cap to pin 34 (DMPI)
2	GND	Drive power ground
3	N_{DR}	Output of low voltage drive buffer for N-DMOS, 10nF external cap to pin 9 (NGATE)
4	V_{DD}	Positive voltage supply for drive circuitry (+12V)
5	VDD	Positive voltage supply for drive circuitry (+12V)
6	V_{SUB}	Substrate connection of control / driver die chip (connected to the most positive supply, V_{PP})
7	$RGND_N$	Ground return of damp N-DMOS source
8	OUT_N	Output of damp N-DMOS drain (open drain output)
9	NGATE	Gate input of the high voltage N-DMOS, 10nF external cap from pin 3 (N_{DR})
10	V_{NN}	Negative high voltage power supply (-100V)
11	V_{NN}	Negative high voltage power supply (-100V)
12	V_{NN}	Negative high voltage power supply (-100V)
13	V_{NN}	Negative high voltage power supply (-100V)
14	V_{NN}	Negative high voltage power supply (-100V)
15	TX_N	Output of the high voltage N-DMOS drain (open drain output)
16	TX_N	Output of the high voltage N-DMOS drain (open drain output)
17	NC	No connection
18	TX_P	Output of the high voltage P-DMOS drain (open drain output)
19	TX_P	Output of the high voltage P-DMOS drain (open drain output)
20	V_{PP}	Positive high voltage power supply (+100V)
21	V_{PP}	Positive high voltage power supply (+100V)
22	V_{PP}	Positive high voltage power supply (+100V)
23	V_{PP}	Positive high voltage power supply (+100V)
24	V_{PP}	Positive high voltage power supply (+100V)
25	PGATE	Gate input of the high voltage P-DMOS, 10nF external cap from pin 31 (P_{DR})
26	OUT_P	Damp P-DMOS drain (open drain output)
27	$RGND_P$	Ground return of damp P-DMOS
28	V_{SUB}	Substrate connection of control / driver die chip (connected to the most positive supply, V_PP)
29	V_{DD}	Positive voltage supply for drive circuitry (+12V)
30	V_{DD}	Positive voltage supply for drive circuitry (+12V)
31	P_{DR}	Output of low voltage drive buffer for P-DMOS, 10nF external cap to pin 25 (PGATE)
32	GND	Drive power ground
33	GND	Drive power ground
34	DMPI	Connects to damp power P-DMOS gate, 10nF cap to pin 1 (DMPO)
35	P_{IN}	Input logic control of the high voltage P-DMOS pin 18 &19 (TX_P), Hi = on, Low = off
36	V_{LN}	Negative low voltage power supply (–5V)
37	AV_{DD}	Positive analog voltage power supply (+12V)
38	AGND	Analog signal ground (0V)
39	V_{SUB}	Substrate connection of control / driver chip (connected to the most positive supply)
40	EN	Control / drive chip power enable Hi = on, Low = off
41	DAMP	Input of damp control on both pin 26 (OUT_P) and pin 8 (OUT_N), Hi = on, Low = off
42	CLAMP	Input of clamp switches on both gates of output P-DMOS and N-DMOS, Hi = on, Low = off
43	V_{LL}	Positive voltage supply of low voltage logic (+1.8V to +5V)
44	N_{IN}	Input logic control of the high voltage N-DMOS pin 15 & 16 (TX_N), Hi = on, Low = off

Note: The three thermal slabs on the bottom of the package must be externally connected PAD1 to V_{SUB}, PAD2 to TX_N, and PAD3 to TX_P.

44-Lead QFN (K6) Package Outline



Top View



Note:
1. Dimensions in mm. [Inch]
2. Radius is 0.127mm
3. Three thermal slabs on the bottom of the package must be externally connected PAD1 to V_{SUB}, PAD2 to TX_N, and PAD3 to TX_P.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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