AN2566
Application note

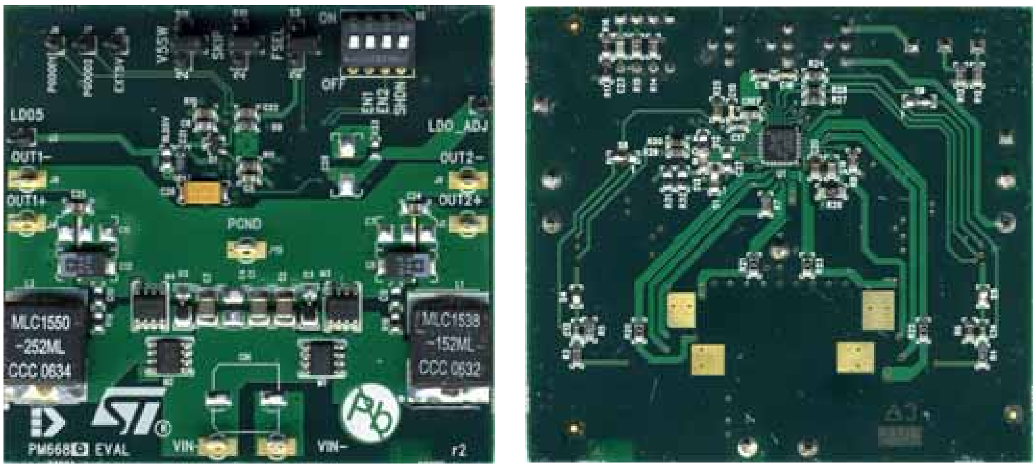
PM6680 evaluation kit dual step-down controller with auxiliary voltages for notebook power system

Introduction

PM6680A evaluation kit order code: STEVAL-ISA053V1.

The PM6680 is a dual step-down controller with adjustable output voltages for notebook computer power systems. The PM6680 evaluation kit is designed to test the performance of the PM6680 by employing a typical application circuit that allows testing of all PM6680 device functions. The kit features two switching sections, with (typically) 1.5 V and 1.05 V outputs, from a 6 V to 28 V input battery voltage. The operating switching frequency of the two switching sections is 200 kHz / 300 kHz, respectively. Each switching section delivers more than 5 A output current. Moreover, an internal linear regulator can provide 5 V @ 100 mA peak current.

Figure 1. PM6680 evaluation kit



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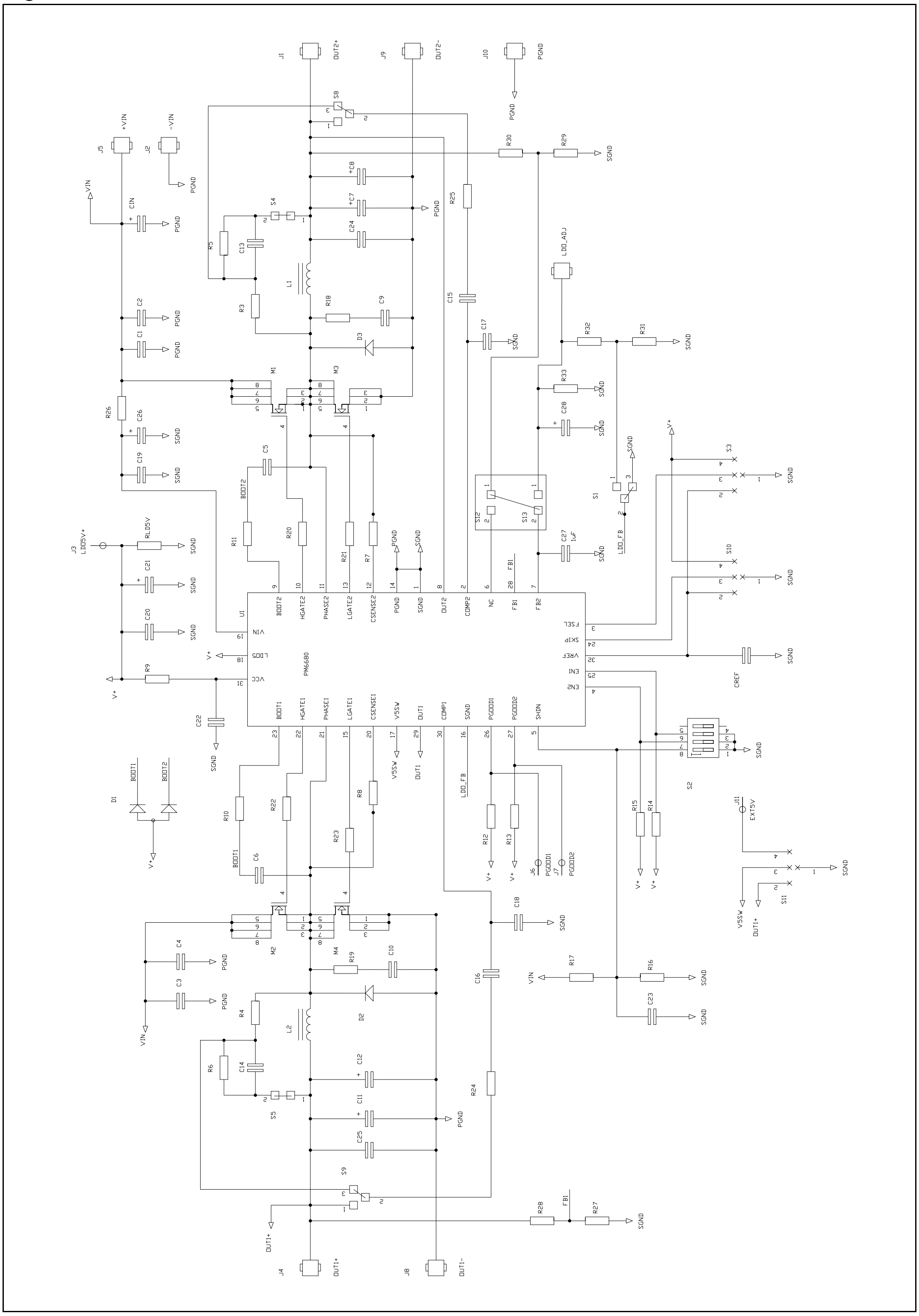
1 Main features

- Constant on-time control allows very fast load transients
- 6 V to 28 V input voltage range
- 5 V auxiliary output voltage
- Adjustable switching outputs
- Lossless current sensing using low side MOSFET $R_{DS(on)}$
- Negative current limit
- Soft-start internally fixed at 2.8 ms
- Soft-end for output discharge
- 200 kHz / 300 kHz, 300 kHz / 400 kHz, 400 kHz / 500 kHz (5 V / 3 V selectable switching frequency)
- Selectable pulse skip and no-audible skip modes at light loads
- Independent power good signals

2 Evaluation kit schematic

Figure 2. Evaluation kit schematic



3 Component list

Table 1. Component list

Name	Description	Size	Value	Supplier	Part number
C1, C2, C3	Ceramic capacitor 50 V	1210	10 µF	Taiyo Yuden	UMK325BJ106KM
C4	Ceramic capacitor 50 V	1210	Not installed		
C5, C6	Ceramic capacitor	0805	0,1 µF	Standard	
C7	Low ESR capacitor	D case	Not installed	Standard	
C8	Low ESR capacitor 4 V, 12 mΩ ESR	D case	330 µF	POSCAP - Sanyo	4TPD33OM
C11	Low ESR capacitor	D case	Not installed	Standard	
C12	Low ESR capacitor 4 V, 12 mΩ ESR	D case	330 µF	POSCAP - Sanyo	4TPD33OM
C13, C14	Ceramic capacitor	0805	5.6 nF	Standard	
C15, C16	Ceramic capacitor	0603	1 nF	Standard	
C17, C18	Ceramic capacitor	0603	47 pF	Standard	
C19	Ceramic capacitor 50 V	0805	0.1 µF	Standard	B37941K5104K62
C26	Tantalum capacitor 35 V	C case	4.7 µF	AVX TPS	TPSC475*035#0600
C20	Ceramic capacitor	0603	1 µF	Standard	
C21	Tantalum capacitor package A, 16 V	B case	4.7 µF	AVX THJ	THJB475*016#JN
C22	Ceramic capacitor	0805	220 nF	Standard	
C9, C10	Ceramic capacitor	0805	Not installed	Standard	
C23	Ceramic capacitor	0603	10 pF	Standard	
CIN	Electrolytic capacitor 39 µF, 25 V	D 10 mm	Not installed	Sanyo	25SVPD39M
CREF	Ceramic capacitor	0603	100 nF	Standard	
C24,C25	Ceramic capacitor	0805	10 µF	Standard	
C27	Ceramic capacitor	0805	Not installed	Standard	
C28	Tantalum capacitor	3216	Not installed	Standard	
D1	Dual Schottky diode	SOT23		STMicroelectronics	BAT54A
D2,D3	Diode 1 A, 30 V	DO216-AA		STMicroelectronics	STPS1L30M
IC1	PM6680 device	VFQFPN-32 5 mm x 5 mm		STMicroelectronics	PM6680

Table 1. Component list (continued)

Name	Description	Size	Value	Supplier	Part number
L1	1.5 µH inductor, 12 A sat.	13 mm x 13 mm	1.5 µH	Coilcraft	MLC1538-152ML
L2	2.5 µH inductor, 8 A sat.	13 mm x 13 mm	2.5 µH	Coilcraft	MLC1550-252ML
M1	MOSFET control FET SO-8	SO-8		STMicroelectronics	STS12NH3LL
M2	MOSFET control FET SO-8	SO-8		STMicroelectronics	STS12NH3LL
M3	MOSFET Sync FET SO-8	SO-8		STMicroelectronics	STS12NH3LL
M4	MOSFET Sync FET SO-8	SO-8		STMicroelectronics	STS12NH3LL
R7,R8	Resistor	0805	680 Ω	Standard	
R3	Resistor	0805	22 kΩ	Standard	
R4	Resistor	0805	36 kΩ	Standard	
R5	Resistor	0805	3.3 kΩ	Standard	
R6	Resistor	0805	3 kΩ	Standard	
R24	Resistor	0805	1.1 kΩ	Standard	
R25	Resistor	0805	820 Ω	Standard	
R9	Resistor	0805	47 Ω	Standard	
R10,R11	Resistor	0805	10 Ω	Standard	
R12,R13, R14,R15	Resistor	0603	100 kΩ	Standard	
R16	Resistor	0603	150 kΩ	Standard	
R18,R19	Resistor	0603	Not installed		
R17	Resistor	0603	560 kΩ	Standard	
R26	Resistor	1206	3.9 Ω	Standard	
R20, R21, R22, R23	Resistor	0805	0 Ω	Standard	
R27	Resistor	0805	10 kΩ	Standard	
R28	Resistor	0805	6.8 kΩ	Standard	
R29	Resistor	0805	11 kΩ	Standard	
R30	Resistor	0805	1.8 kΩ	Standard	
R31	Resistor	0805	Not installed	Standard	
R32	Resistor	0805	Not installed	Standard	
RLD5V, RLD3V	Resistor	0805	Not installed	Standard	

4 Evaluation board layout

Figure 3. PM6680 evaluation board layout - top layer (PGND plain and component side)

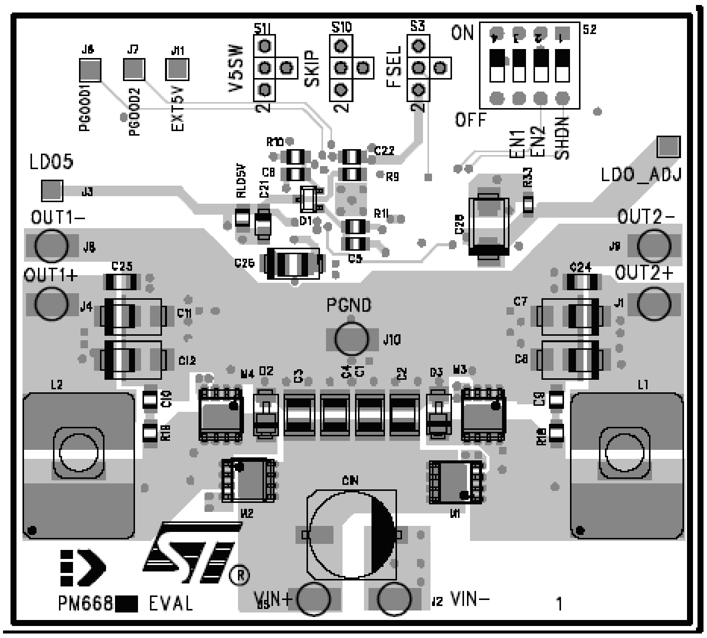


Figure 4. PM6680 evaluation board layout - inner layer 1 (SGND layer and V_{IN} plane)

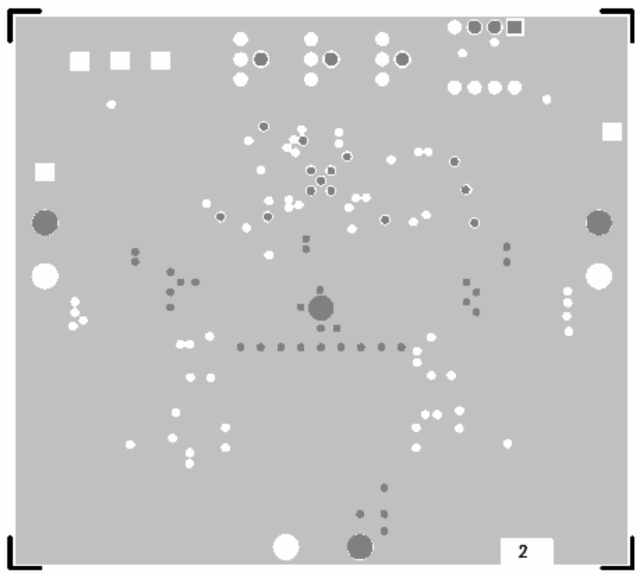


Figure 5. PM6680 evaluation board layout - inner layer 2 (SGND layer and signals)

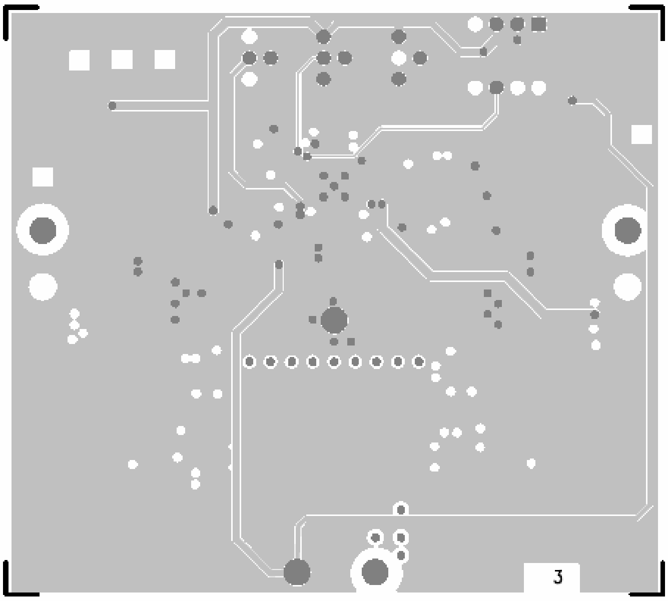
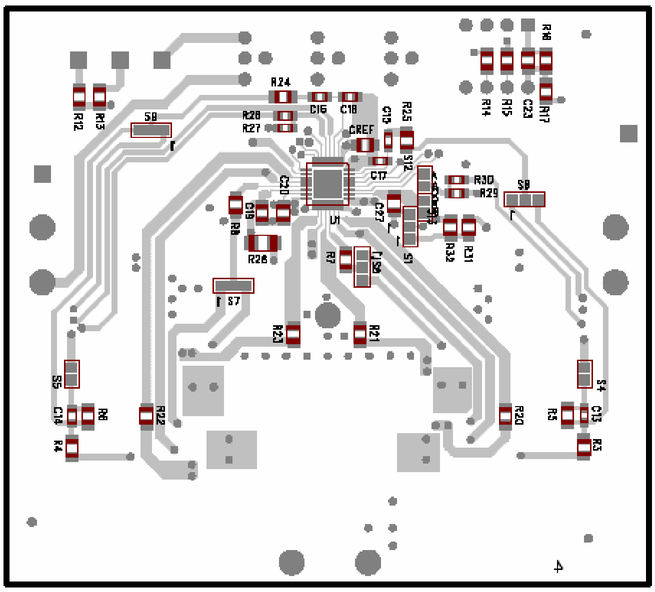


Figure 6. PM6680 evaluation board layout - bottom layer (PM6680 and component side)



5 I/O interface

The evaluation board has the following test points.

Table 2. The test points of the evaluation board

Test point	Description
V_{IN}+	Input voltage
V_{IN}-	Input voltage ground
LDO5	5 V linear regulator output
LDO_ADJ	Not used for this device
EXT5V	5 V external input
OUT1+	OUT1 switching section output
OUT1-	OUT1 switching section output ground
PGOOD1	OUT1 switching section power good
OUT2+	OUT2 switching section output
OUT2+	OUT2 switching section output ground
PGOOD2	OUT2 switching section power good
J10	Junction pin between PGND and SGND planes

6 Recommended equipment

- 6 V to 28 V power supply, notebook computer battery or AC adapter
- Active loads
- Digital multimeter
- 500 MHz four-trace oscilloscope

7 Quick start

1. Connect the V_{IN}+ and V_{IN}- test points of the evaluation board to an external power supply.
2. Ensure that all DIP switches (S2) are in the "OFF" position. In this condition all outputs are disabled (shutdown mode).
3. Turn $S2_1$ to the “ON” position (SHDN pin high). This turns on the LDO5 output (standby-mode).
4. Turn $S2_2$ to the “ON” position (EN1 pin high). The 1.5 V switching controller begins regulation of the output. PGOOD1 pin goes high after soft-start.
5. Turn $S2_3$ to the “ON” position (EN2 pin high). The 1.05 V switching controller begins regulation of the output. PGOOD2 pin goes high after soft-start.
6. In order to load the switching outputs, the loads must be connected between the "+" and the "-" output test points, respectively.
7. In order to load the linear outputs, the loads must be connected between J10 and LDO5 or alternative RLD5V resistors can be used on the evaluation board.

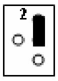
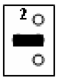
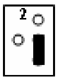
8 Jumper settings

It is possible to select different working conditions by using the jumpers on the board.

Note: Jumpers S1,S6, S7, S12 and S13 are already soldered on the evaluation board and it is not necessary to change them. Please refer to the schematic to verify their proper connection.

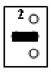
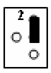
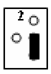
The external bypass connections for the linear regulator LDO5 are set by connecting the V5SW pin to jumper S11 as indicated in *Table 3* below.

Table 3. Jumper S11 - V5SW pin connections

Position	LDO5 working conditions
OUT5V 	When the main output voltage is greater than the boostrap-switchover threshold, an internal 3 Ω (max) P-channel MOSFET switch connects the V5SW pin to the LDO5 pin shutting down the LDO5 internal linear regulator. If not used, it must be tied to ground.
SGND 	The internal linear regulator LDO5 is always on. In this case LDO5 supplies all gate drivers and the internal circuitry. It can provide an output peak current of 100 mA.
EXT5V 	The internal linear regulator LDO5 remains off if an alternative 5V external voltage is applied to the EXT5V test-point. An internal 3 Ω (max) P-channel MOSFET switch connects V5SW pin to LDO5 output. The gate drivers and internal circuitry are supplied by the same 5 V external voltage applied.

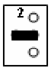
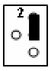
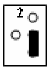
The FSEL pin is connected to jumper S3 to select the SMPS frequency. The jumper positions and corresponding frequencies are shown in *Table 4* below.

Table 4. Jumper S3 - FSEL pin connections

Position	SMPS OUT1	SMPS OUT2
SGND 	200 kHz	300 kHz
VREF 	300 kHz	400 kHz
LDO5 	400 kHz	500 kHz

To select the switching operation mode of the SMPS, connect the SKIP pin to jumper S10 as described in *Table 5.*

Table 5. Jumper S10 - SKIP pin connections

Position	Switching operating mode
GND 	If the SKIP pin is tied to ground, a pulse skip mode takes place at light loads. A zero crossing comparator prevents the inductor current from going negative.
VREF 	if the SKIP pin is tied to VREF pin enables a pulse skip mode with a minimum switching frequency about 25 kHz (ultrasonic mode).
LDO5 	If the SKIP pin is tied to 5 V, The fixed PWM mode takes place. The switching output is in a position to sink and source current from the load.

9 Feedback output connections

Table 6 and *Table 7* below illustrate jumper settings for a loop compensation network for very low output voltage ripple.

Table 6. Jumper S4, S5

Position	Output ripple compensation
Short	Virtual ESR output ripple is generated by using a compensation network connected between the output and PHASE pin of the switching section.

Table 7. Jumper S8, S9

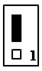
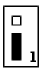
Position	Feedback connection
	Controller feedback signal connected to the compensation network

Table 8 and *Table 9* describe the settings for a loop compensation network for high output voltage ripple.

Table 8. Jumper S4, S5

Position	Output ripple compensation
Open	ESR output ripple is used.

Table 9. Jumper S8, S9

Position	Feedback connection
	Controller feedback signal connected directly to the output capacitor.

10 Test setup and performance summary

10.1 Test setup

The PM6680 evaluation board has the following input/output connections:

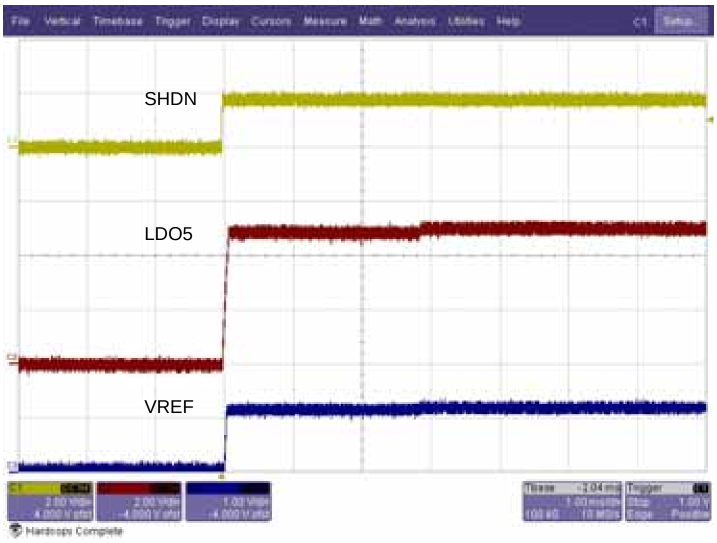
- 12 V input through J5-J2 (V_{IN}+ and V_{IN}-)
- 1.5 V SMPS output through J4-J13 (OUT1+ and OUT1-)
- 1.05 V SMPS output through J1-J12 (OUT2+ and OUT2-)
- 5 V linear regulator output through J3 (LDO5)

A power supply capable of supplying at least 6 A should be connected to V_{IN}+, V_{IN}- and two active loads should be connected respectively to OUT1+, OUT1- and OUT2+, OUT2-.

10.2 Power-up

As shown in *Figure 7*, the power-up starts when the input voltage is applied and the voltage on the SHDN pin is above the device “on” threshold. First, the LDO5 goes up with a masking time of about 4 ms.

Figure 7. REF and LDO5 power-up



10.3 Soft-start and shutdown waveforms

Figure 8 and *9* show the soft-start waveforms.

Figure 10 and *11* show the shut down waveforms.

The PM6680 has an independent internal digital soft-start for each switching section. During the soft-start phase the internal current limit increases from 25% to 100%, in increments of 25%, to avoid the inductor current reaching too high a value.

Figure 8. Section 1 soft-start waveforms

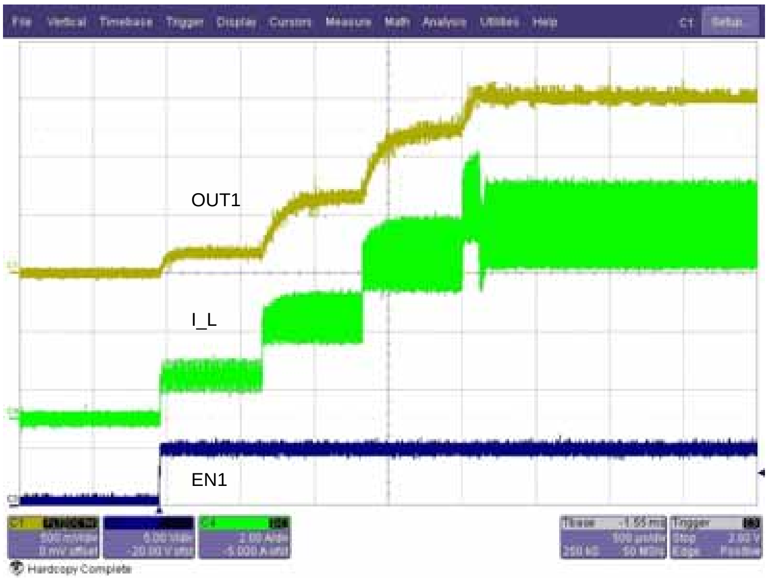
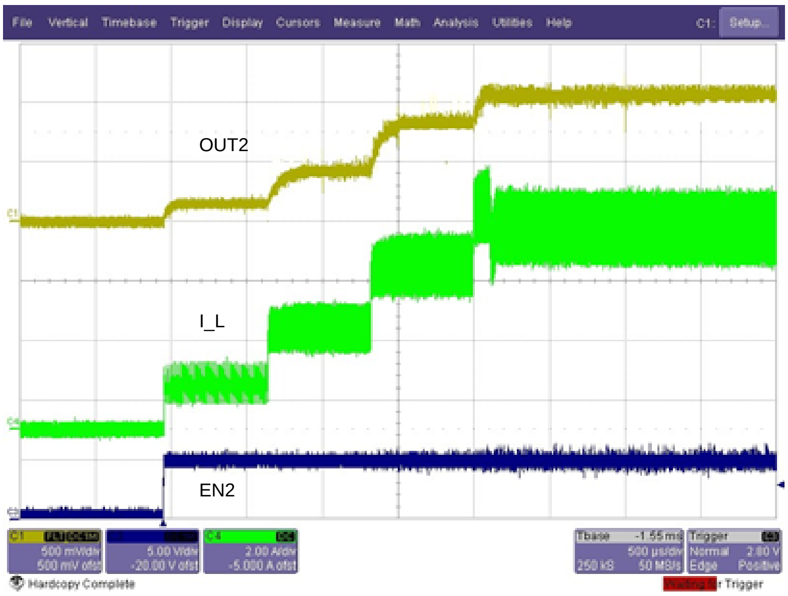


Figure 9. Section 2 soft-start waveforms



Driving the SHDN pin below the SHDN device “off” threshold will cause the device to enter shutdown mode. In this case the switching outputs are connected to ground through an internal 12 Ω power MOSFET and are discharged softly, (discharge mode). When the output voltages reach 0.3 V, the low side MOSFETs are turned on, quickly discharging them to ground.

Figure 10. Section 1 shutdown waveforms

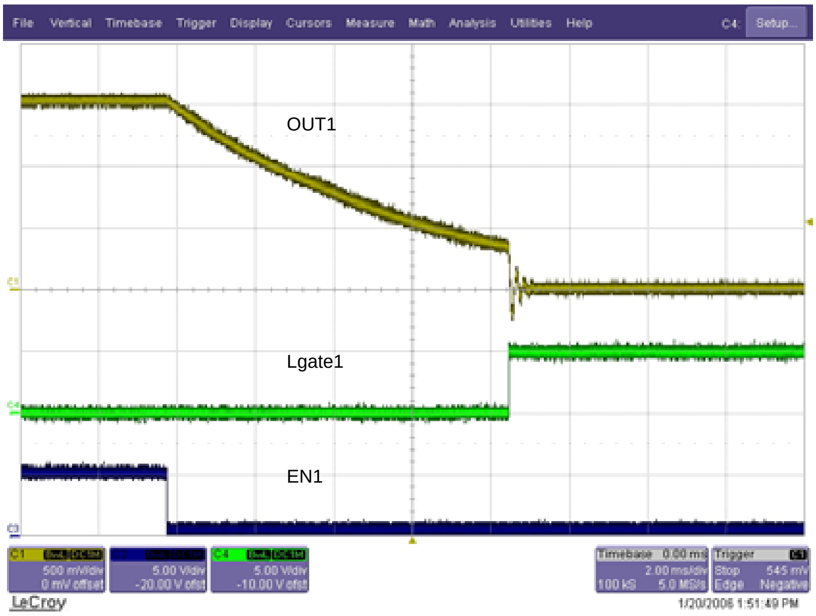


Figure 11. Section 2 shutdown waveforms

10.4 1.5 V and 1.05 V output efficiency vs. load current

Figure 12 and *Figure 13* show the efficiency versus load current for different input voltage values in PWM mode, skip mode and no-audible skip mode.

Figure 12. 1.5 V SMPS efficiency

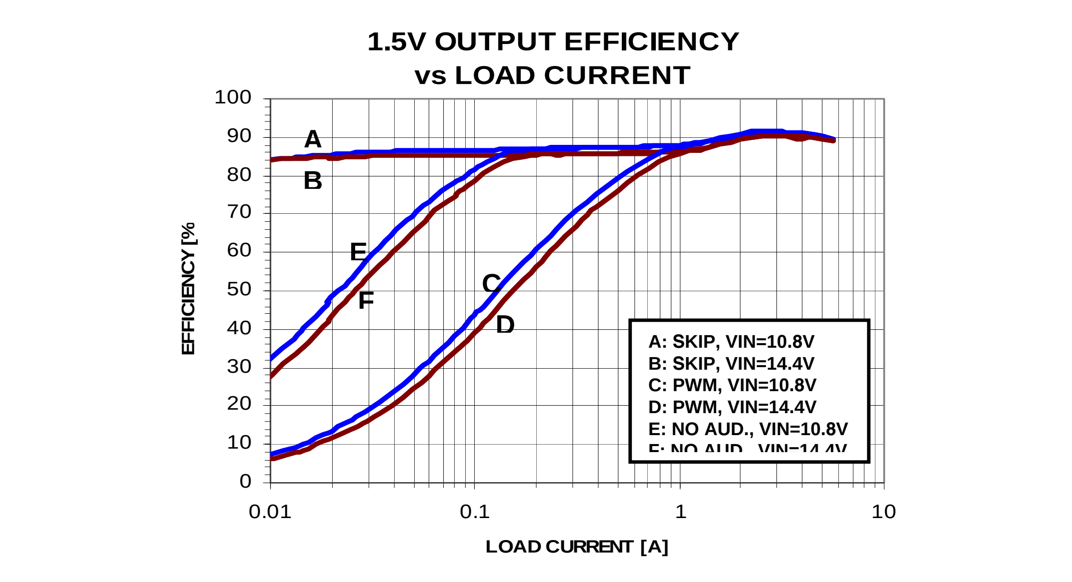
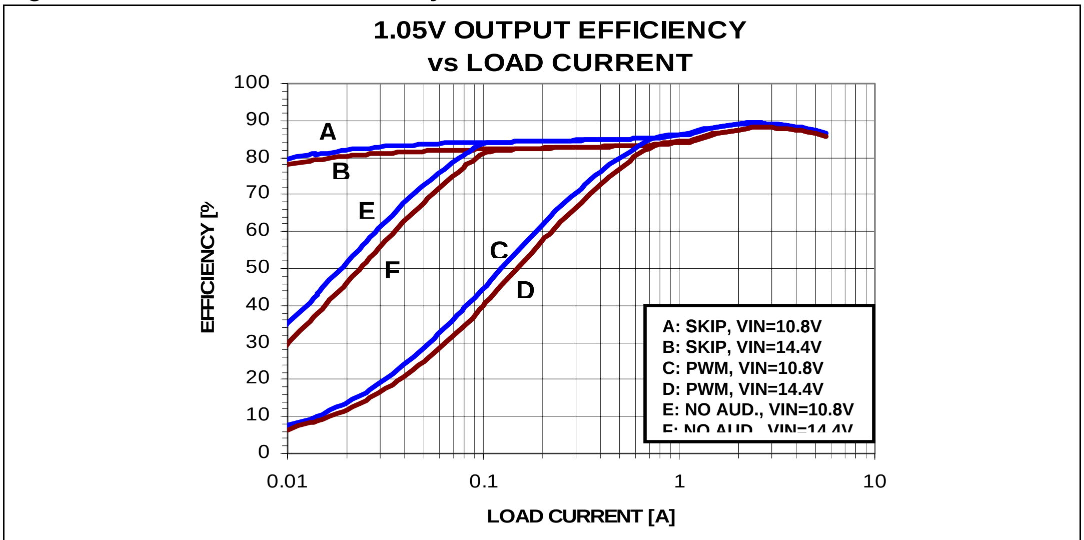


Figure 13. 1.05 V SMPS efficiency



10.5 Power consumption analysis

To measure the device consumption under real working conditions, an external power supply of +5 V is connected to EXT5V.

The two traces on figures that follow show the differentiation between the two input currents. Once the internal linear regulator is turned on, device consumption will increase as a consequence.

Figure 14 shows the input current consumption measured at V_{IN}+ (includes ISHDN) and the input device current consumption measured at the VCC pin. Both switching sections are working in forced PWM mode. No load is applied on the outputs.

Figure 14. Input current vs. input voltage

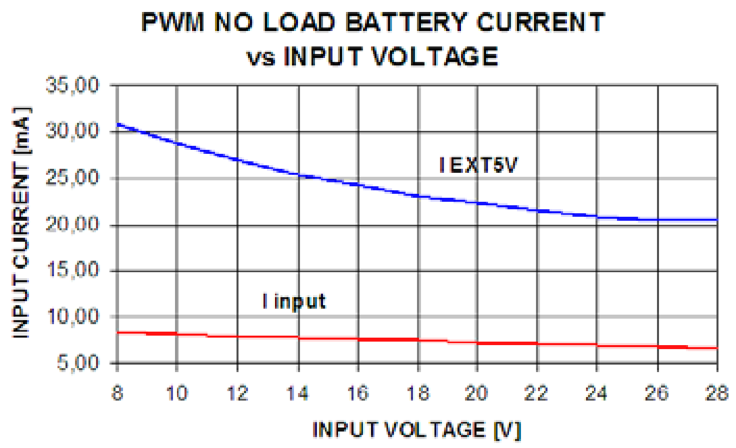


Figure 15 shows the input current consumption measured at V_{IN}+ (includes ISHDN) and the input device current consumption measured at the VCC pin(IEXT5V). Both switching sections are working in SKIP mode. No load is applied.

Figure 15. Input current vs. input voltage

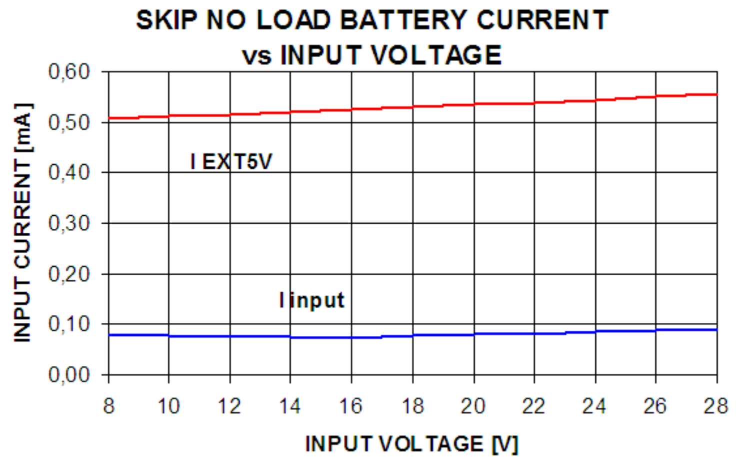
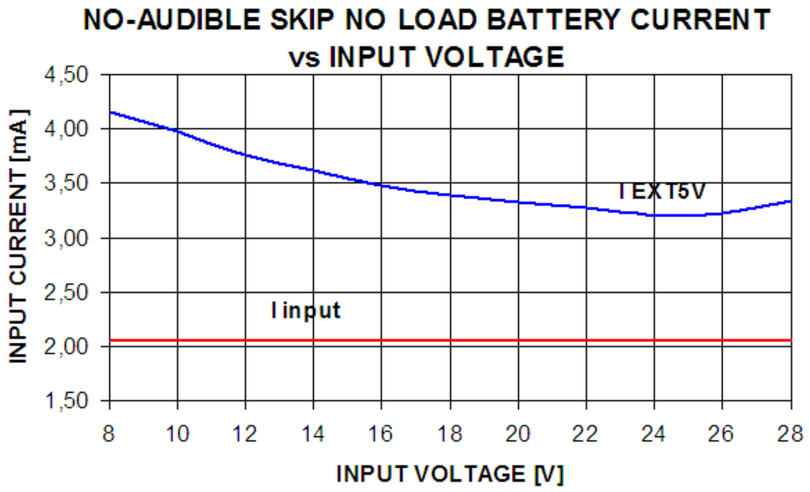


Figure 16 shows the input current consumption measured at V_{IN}+ (includes ISHDN) and the input device current consumption measured at the VCC pin(IEXT5V). Both switching sections are working in NO-AUDIBLE SKIP mode. No load is applied.

Figure 16. Input current vs. input voltage



In the following illustrations, the device current consumption is measured in shutdown mode and standby mode. In shutdown mode all outputs are off (SHDN pin low). In standby mode only the linear regulator output is on (V5SW = SGND, SHDN pin high, EN5 and EN3 pins low).

Figure 17. Device current consumption vs. input voltage

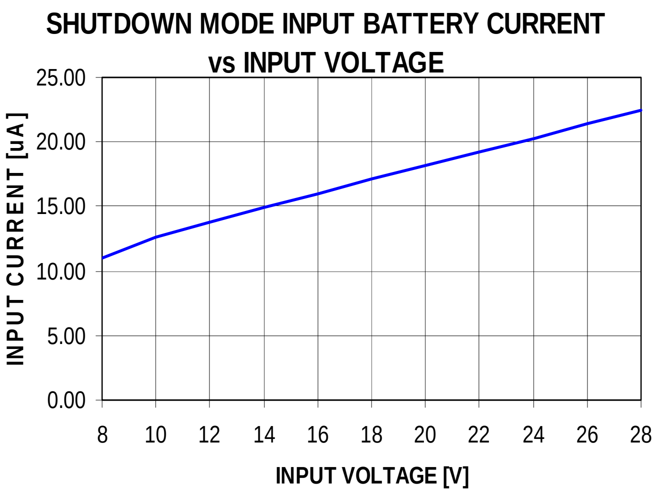
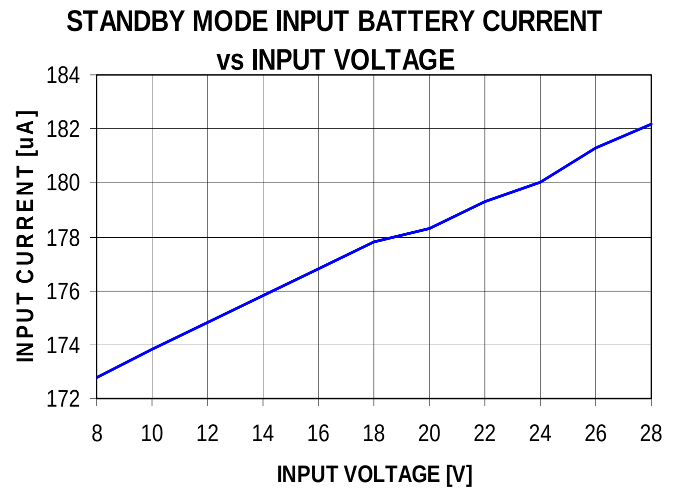


Figure 18. Device current consumption vs. input voltage



10.6 Switching frequency vs. load current

Figure 19 and *Figure 20* show the switching frequency variation with the load current in PWM mode, skip mode and no-audible skip mode. 12 V is applied at the V_{IN}+ and V_{IN}- test points.

Figure 19. 1.5 V output switching frequency vs. load current

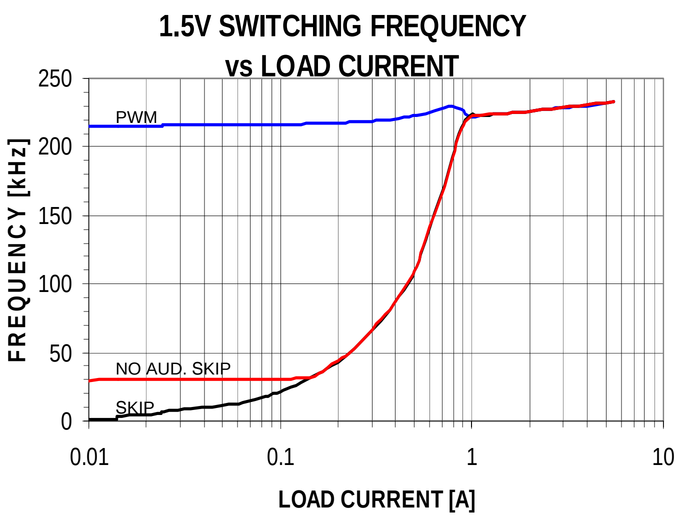
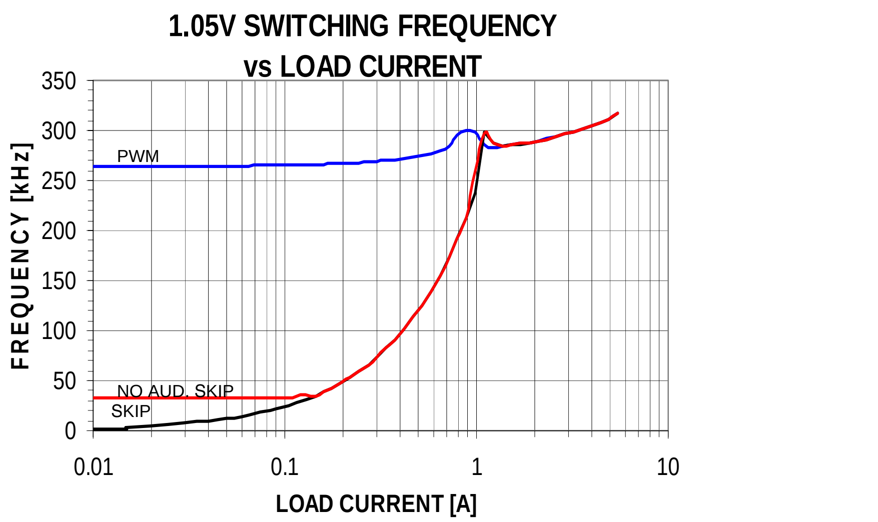


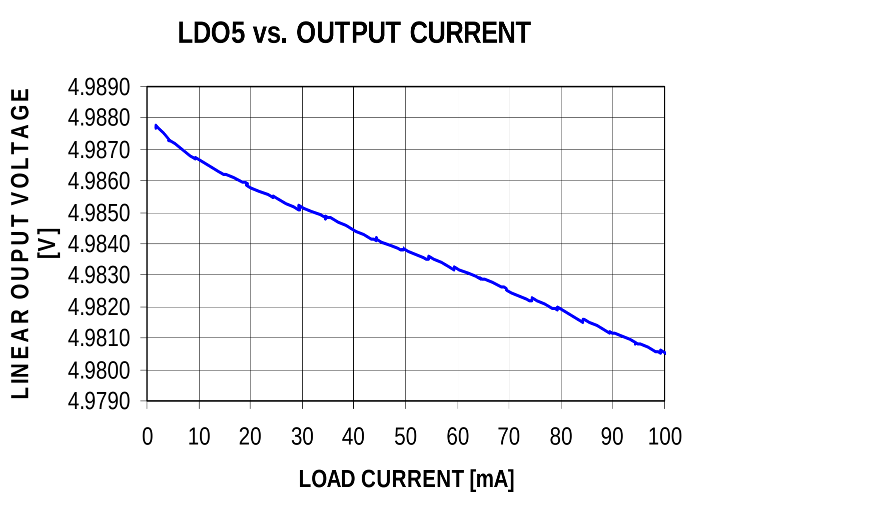
Figure 20. 1.05 V output switching frequency vs. load current



10.7 Linear regulator output voltages vs. output current

Figure 21 shows the load regulation for the internal linear regulator LDO5. Both switching sections are disabled and 12 V is applied at V_{IN}+ and V_{IN}- test points.

Figure 21. LDO5 output vs. load current



10.8 Load transient responses

The following figures show the load transient response from 1 A to 4 A for both switching outputs. In each of these cases the PM6680 works in forced PWM mode (the SKIP pin is high).

Figure 22. SMPS 1.5 V load transient response

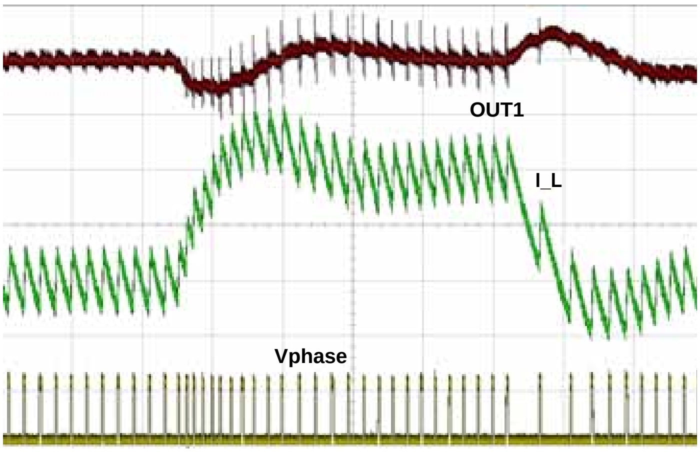
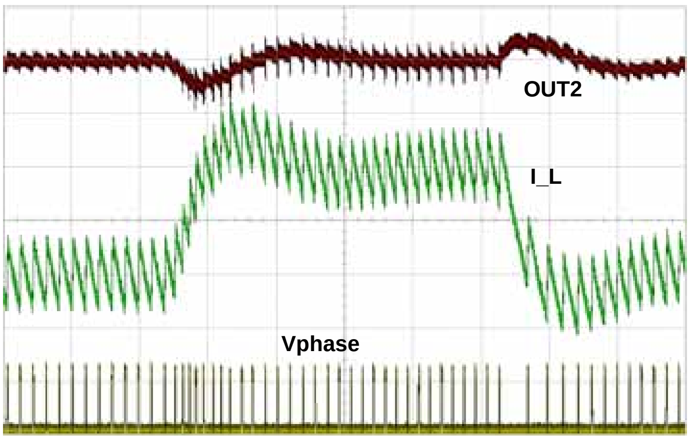


Figure 23. SMPS 1.05 V load transient response



11 Representatives waveforms

The following illustrations show the relevant waveforms of a switching section and are provided to underline the behavior of the device in pulse skip mode, no-audible skip mode and forced PWM mode working conditions.

Figure 24. SMPS pulse skip mode

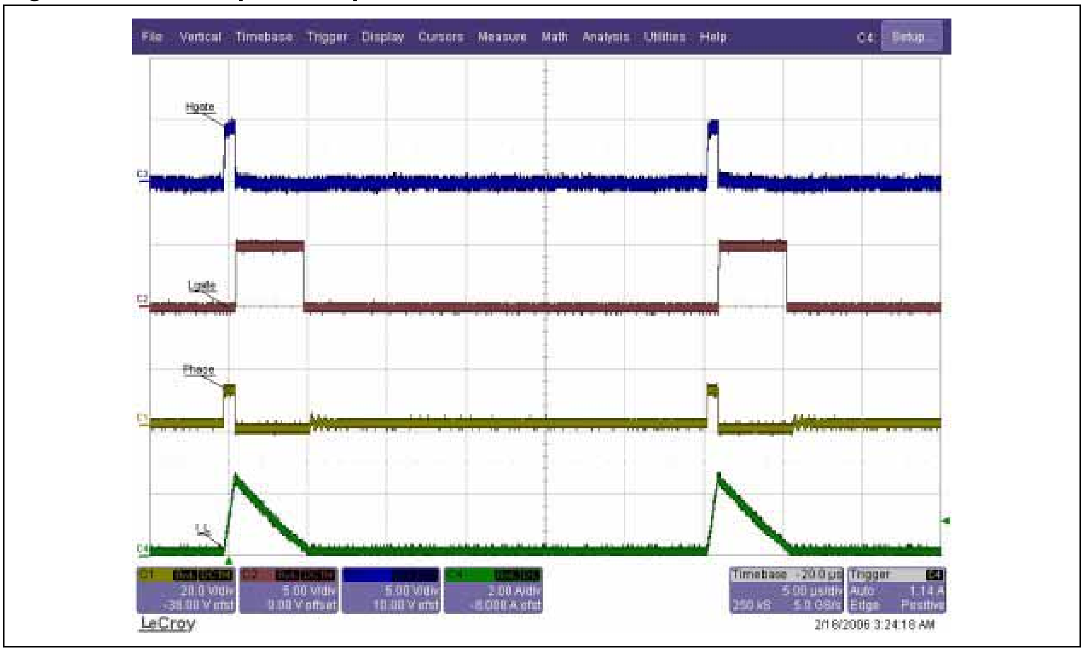


Figure 25. SMPS no-audible skip mode

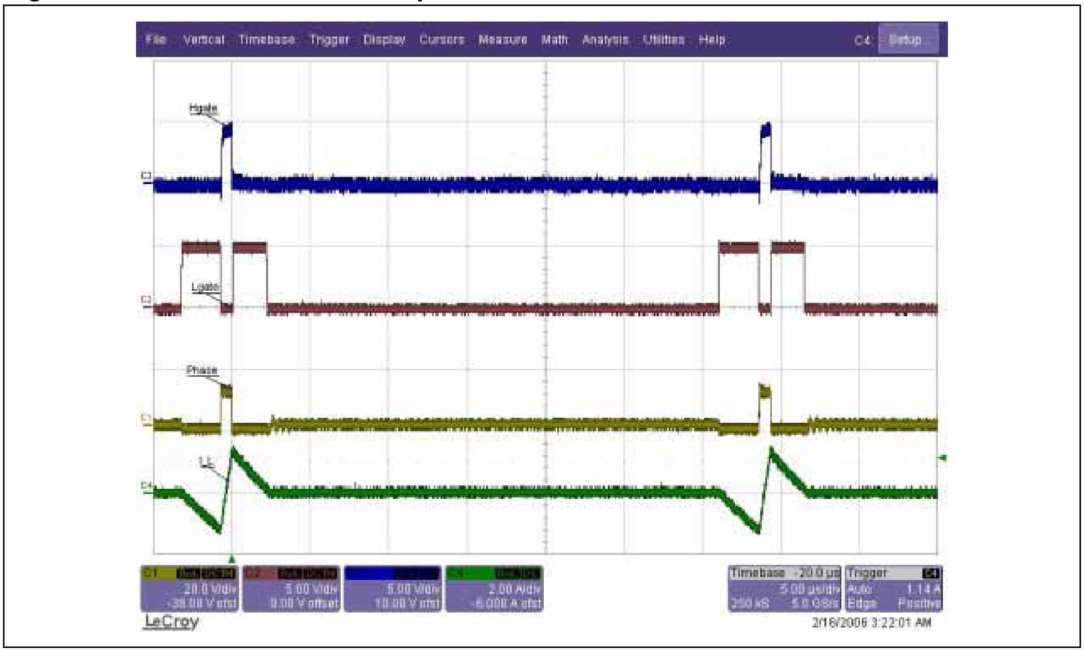
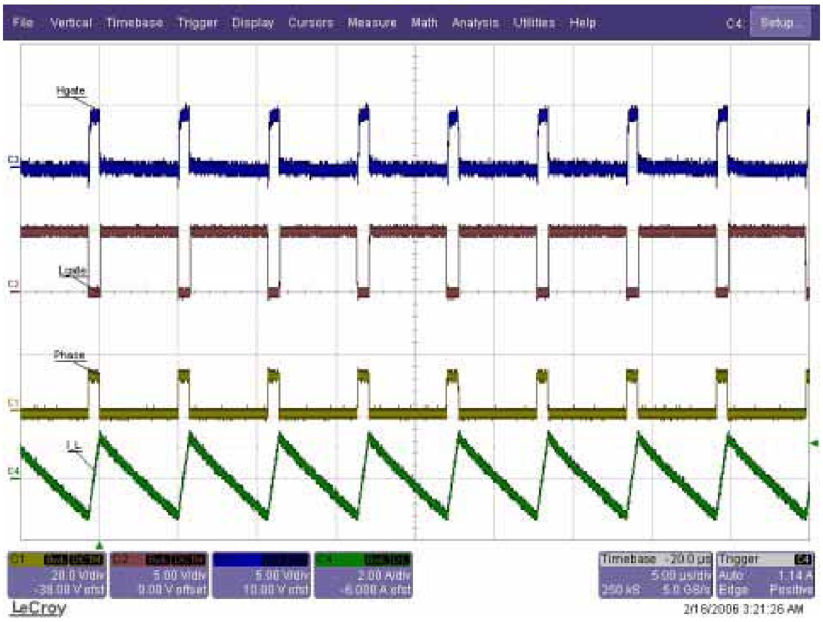


Figure 26. SMPS PWM mode



12 Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Aug-2007	1	Initial release
05-Mar-2008	2	– Changed: *Figure 1*, *2*, *3*, *14*, and *16* – Modified: *Table 1* – Minor text changes
07-Apr-2008	3	– Modified*: Introduction*