Defense Grade Platform Flash In-System Programmable Configuration PROM

DS541 (v3.0) August 5, 2015 **Product Specification**

Features

- In-System Programmable PROM for Configuration of Xilinx FPGAs
- Low-Power Advanced CMOS NOR FLASH Process
- Endurance of 20,000 Program/Erase Cycles
- Operation over Full Military Temperature Range (–55°C to +125°C)
- IEEE Standard 1149.1/1532 Boundary-Scan (JTAG) Support for Programming, Prototyping, and Testing
- JTAG Command Initiation of Standard FPGA Configuration
- Cascadable for Storing Longer or Multiple Bitstreams
- Dedicated Boundary-Scan (JTAG) I/O Power Supply (V_{CCJ})
- I/O Pins Compatible with Voltage Levels Ranging From 1.8V to 3.3V
- Design Support Using the Xilinx Alliance ISE™ and Foundation ISE Series Software Packages
- XQF32P
  - 1.8V Supply Voltage
  - Serial or Parallel FPGA Configuration Interface (up to 33 MHz)
  - Available in Small-Footprint VOG48 Package
  - Design Revision Technology Enables Storing and Accessing Multiple Design Revisions for Configuration
  - Built-In Data Decompressor Compatible with Xilinx Advanced Compression Technology

Table 1: **Xilinx Defense Grade Platform Flash PROM Features**

Device	Density	V_{CCINT}	V_{CCO} Range	V_{CCJ} Range	Packages	Program In-system via JTAG	Serial Config.	Parallel Config.	Design Revisioning	Compression
XQF32P	32 Mbit	1.8V	1.8V – 3.3V	2.5V – 3.3V	VOG48	✓	✓	✓	✓	✓

Description

This data sheet describes the defense-grade version of the Platform Flash series of in-system programmable configuration PROMs. Available in 32 Megabit (Mbit) density, this PROM provides an easy-to-use, cost-effective, and reprogrammable method for storing large Xilinx FPGA configuration bitstreams. The 32-Mbit PROM supports Master Serial, Slave Serial, Master SelectMAP, and Slave SelectMAP FPGA configuration modes (Figure 1).

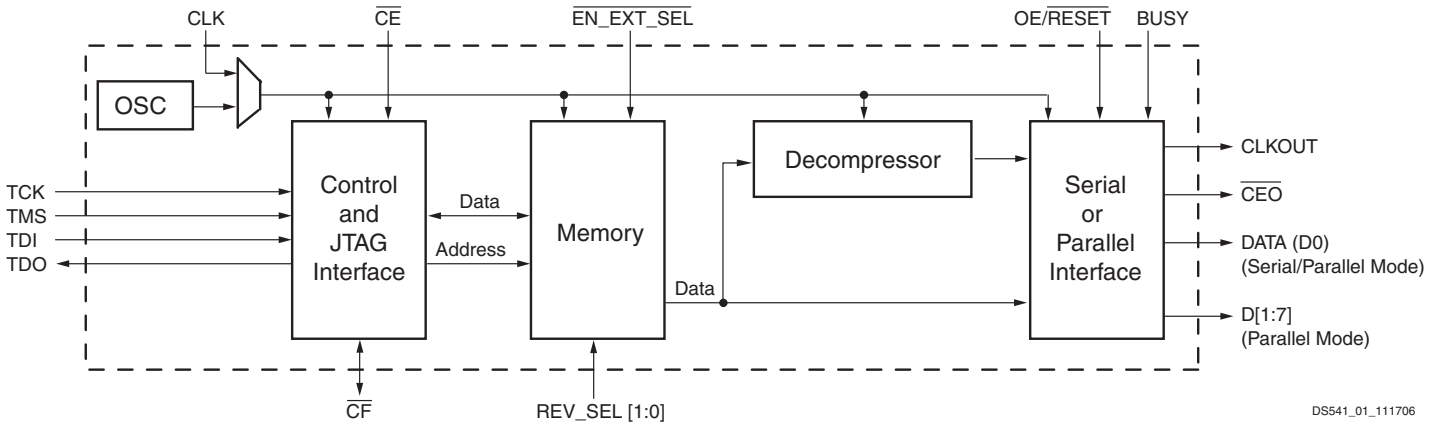


Figure 1: **XQF32P Platform Flash PROM Block Diagram**

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. With $\overline{CF}$ High, a short access time after $\overline{CE}$ and OE are enabled, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. New data is available a short access time after each rising clock edge. The FPGA generates the appropriate number of clock pulses to complete the configuration.

When the FPGA is in Slave Serial mode, the PROM and the FPGA are both clocked by an external clock source, or optionally, the PROM can be used to drive the FPGA's configuration clock.

The XQF32P defense-grade version of the Platform Flash PROM also supports Master SelectMAP and Slave SelectMAP (or Slave Parallel) FPGA configuration modes. When the FPGA is in Master SelectMAP mode, the FPGA generates a configuration clock that drives the PROM. When the FPGA is in Slave SelectMAP Mode, either an external oscillator generates the configuration clock that drives the PROM and the FPGA, or optionally, the XQF32P PROM can be used to drive the FPGA's configuration clock. With BUSY Low and $\overline{CF}$ High, after $\overline{CE}$ and OE are enabled, data is available on the PROM DATA (D0-D7) pins. New data is available a short access time after each rising clock edge. The data is clocked into the FPGA on the following rising edge of the CCLK. A free-running oscillator can be used in the Slave Parallel /Slave SelecMAP mode.

The XQF32P defense-grade version of the Platform Flash PROM provides additional advanced features. A built-in data decompressor supports utilizing compressed PROM files, and design revisioning allows multiple design revisions to be stored on a single PROM or stored across several PROMs. For design revisioning, external pins or internal control bits are used to select the active design revision.

Multiple Platform Flash PROM devices can be cascaded to support the larger configuration files required when targeting larger FPGA devices or targeting multiple FPGAs daisy chained together. When utilizing the advanced features for the XQF32P Platform Flash PROM, such as design revisioning, programming files which span cascaded PROM devices can only be created for cascaded chains containing only XQF32P PROMs.

The Platform Flash PROMs are compatible with all of the existing FPGA device families. The XQF32P Platform Flash PROM capacity is 33,554,432 configuration bits.

Programming

In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be daisy-chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 2. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The programming data sequence is delivered to the device using either Xilinx iMPACT software and a Xilinx download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format, including automatic test equipment. During in-system programming, the $\overline{CEO}$ output is driven High. All other outputs are held in a high-impedance state or held at clamp levels during in-system programming. In-system programming is fully supported across the recommended operating voltage and temperature ranges.

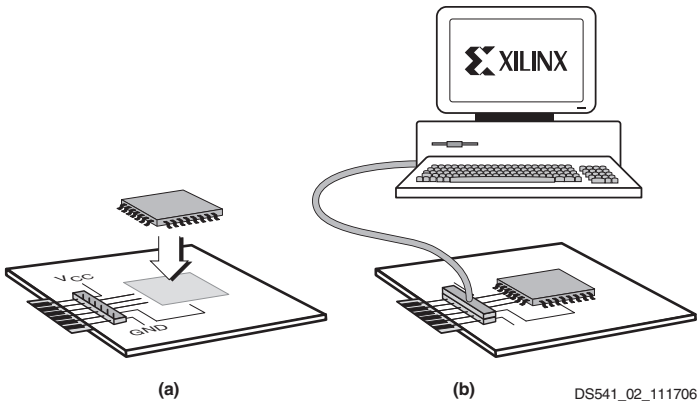


Figure 2: **JTAG In-System Programming Operation**
(a) Solder Device to PCB (b) Program Using Download Cable

External Programming

In traditional manufacturing environments, third-party device programmers can program Platform Flash PROMs with an initial memory image before the PROMs are assembled onto boards. Contact a preferred third-party programmer vendor for Platform Flash PROM support information. A sample list of third-party programmer vendors with Platform Flash PROM support is available on the Xilinx web page for *Third-Party Programmer Device Support*. See UG161, *Platform Flash PROM User Guide*, for the PROM data file format required for programmers.

Pre-programmed PROMs can be assembled onto boards using the typical soldering process guidelines in UG112, *Device Package User Guide*. A pre-programmed PROM's memory image can be updated after board assembly using an in-system programming solution.

Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 20,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

Design Security

The Xilinx in-system programmable Platform Flash PROM devices incorporate advanced data security features to fully protect the FPGA programming data against unauthorized reading via JTAG. The XQF32P PROMs can also be programmed to prevent inadvertent writing via JTAG. Table 2 shows the security settings available for the XQF32P PROM.

Read Protection

The read protect security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. Read protection does not prevent write operations. For the XQF32P PROM the read protect security bit can be set for individual design revisions, and resetting the read protect bit requires erasing the particular design revision.

Write Protection

The XQF32P PROM device also allows the user to write protect (or lock) a particular design revision to prevent inadvertent erase or program operations. Once set, the write protect security bit for an individual design revision must be reset (using the UNLOCK command followed by ISC_ERASE command) before an erase or program operation can be performed.

Table 2: **XQF32P Design Revision Data Security Options**

Read Protect	Write Protect	Read/Verify Inhibited	Program Inhibited	Erase Inhibited
Reset (default)	Reset (default)	–	–	–
Reset (default)	Set	–	✓	✓
Set	Reset (default)	✓	–	–
Set	Set	✓	✓	✓

IEEE 1149.1 Boundary-Scan (JTAG)

The Platform Flash PROM family is compatible with the IEEE 1149.1 boundary-scan standard and the IEEE 1532 in-system configuration standard. A Test Access Port (TAP) and registers are provided to support all required boundary scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the Platform Flash PROM device. Table 3 lists the required and optional boundary-scan instructions supported in the Platform Flash PROMs. Refer to the IEEE Std. 1149.1 specification for a complete description of boundary-scan architecture and the required and optional instructions.

Note: The XQF32P JTAG TAP pause states are not fully compliant with the JTAG 1149.1 specification. If a temporary pause of a JTAG shift operation is required, then stop the JTAG TCK clock and maintain the JTAG TAP within the JTAG Shift-IR or Shift-DR TAP state. Do not transition the XQF32P JTAG TAP through the JTAG Pause-IR or Pause-DR TAP state to temporarily pause a JTAG shift operation.

Table 3: **Platform Flash PROM Boundary Scan Instructions**

Boundary-Scan Command	XQF32P IR[15:0] (Hex)	Instruction Description
Required Instructions		
BYPASS	FFFF	Enables BYPASS.
SAMPLE/PRELOAD	0001	Enables boundary-scan SAMPLE/PRELOAD operation.
EXTEST	0000	Enables boundary-scan EXTEST operation.
Optional Instructions		
CLAMP	00FA	Enables boundary-scan CLAMP operation.
HIGHZ	00FC	Places all outputs in high-impedance state simultaneously.
IDCODE	00FE	Enables shifting out 32-bit IDCODE.
USERCODE	00FD	Enables shifting out 32-bit USERCODE.
Platform Flash PROM Specific Instructions		
CONFIG	00EE	Initiates FPGA configuration by pulsing $\overline{CF}$ pin Low once (for the XQF32P, this command also resets the selected design revision based on either the external REV_SEL[1:0] pins or on the internal design revision selection bits).(1)

Notes:

1. For more information see Initiating FPGA Configuration, page 9.

Instruction Register

The Instruction Register (IR) for the Platform Flash PROM is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI.

XQF32P Instruction Register (16 bits wide)

The Instruction Register (IR) for the XQF32P PROM is sixteen bits wide and is connected between TDI and TDO during an instruction scan sequence. The detailed composition of the instruction capture pattern is illustrated in Table 4.

The instruction capture pattern shifted out of the XQF32P device includes IR[15:0]. IR[15:9] are reserved bits and are set to a logic 0. The ISC Error field, IR[8:7], contains a `10` when an ISC operation is a success; otherwise a `01` when an In-System Configuration (ISC) operation fails. The Erase/Program (ER/PROG) Error field, IR[6:5], contains a `10` when an erase or program operation is a success; otherwise a `01` when an erase or program operation fails. The Erase/Program (ER/PROG) Status field, IR[4], contains a logic 0 when the device is busy performing an erase or programming operation; otherwise, it contains a logic 1. The ISC Status field, IR[3], contains logic 1 if the device is currently in In-System Configuration (ISC) mode; otherwise, it contains logic 0. The DONE field, IR[2], contains logic 1 if the sampled design revision has been successfully programmed; otherwise, a logic 0 indicates incomplete programming. The remaining bits IR[1:0] are set to `01` as defined by IEEE Std. 1149.1.

Table 4: **XQF32P Instruction Capture Values Loaded into IR as part of an Instruction Scan Sequence**

TDI →	**IR[15:9]**	**IR[8:7]**	**IR[6:5]**	**IR[4]**	**IR[3]**	**IR[2]**	**IR[1:0]**	**→ TDO**
	Reserved	ISC Error	ER/PROG Error	ER/PROG Status	ISC Status	DONE	0 1	

Boundary Scan Register

The boundary-scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output pin on the Platform Flash PROM has two register stages which contribute to the boundary-scan register, while each input pin has only one register stage. The bidirectional pins have a total of three register stages which contribute to the boundary-scan register. For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the High-Z enable state of the output pin. For each input pin, a single register stage controls and observes the input state of the pin. The bidirectional pin combines the three bits, the input stage bit is first, followed by the output stage bit and finally the output enable stage bit. The output enable stage bit is closest to TDO.

See the XQF32P Pin Names and Descriptions Tables in Pinouts and Pin Descriptions, page 23 for the boundary-scan bit order for all connected device pins, or see the appropriate BSDL file for the complete boundary-scan bit order description under the *attribute BOUNDARY_REGISTER section* in the BSDL file. The bit assigned to boundary-scan cell 0 is the LSB in the boundary-scan register, and is the register bit closest to TDO.

Identification Registers

IDCODE Register

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32 bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG.

The IDCODE register has the following binary format:

`vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1`

where:

`v` = the die version number
`f` = the PROM family code
`a` = the specific Platform Flash PROM product ID
`c` = the Xilinx manufacturer's ID

The LSB of the IDCODE register is always read as logic 1 as defined by IEEE Std. 1149.1. The IDCODE register value for the XQ32PPlatform Flash PROM is `<v>5059093`.

Note: The `<v>` in the IDCODE field represents the device's revision code (in hex) and can vary.

USERCODE Register

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the Platform Flash PROM. If the device is blank or was not loaded during programming, the USERCODE register contains `FFFFFFFFh`.

Customer Code Register

For the XQF32P Platform Flash PROM, in addition to the USERCODE, a unique 32-byte Customer Code can be assigned to each design revision enabled for the PROM. The Customer Code is set during programming, and is typically used to supply information about the design revision contents. A private JTAG instruction is required to read the Customer Code. If the PROM is blank, or the Customer Code for the selected design revision was not loaded during programming, or if the particular design revision is erased, the Customer Code contains all ones.

Platform Flash PROM TAP Characteristics

The Platform Flash PROM family performs both in-system programming and IEEE 1149.1 boundary-scan (JTAG) testing via a single 4-wire test access port (TAP). This simplifies system designs and allows standard automatic test equipment (ATE) to perform both functions. The AC characteristics of the Platform Flash PROM TAP are described as follows.

TAP Timing

Figure 3 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both boundary-scan and ISP operations.

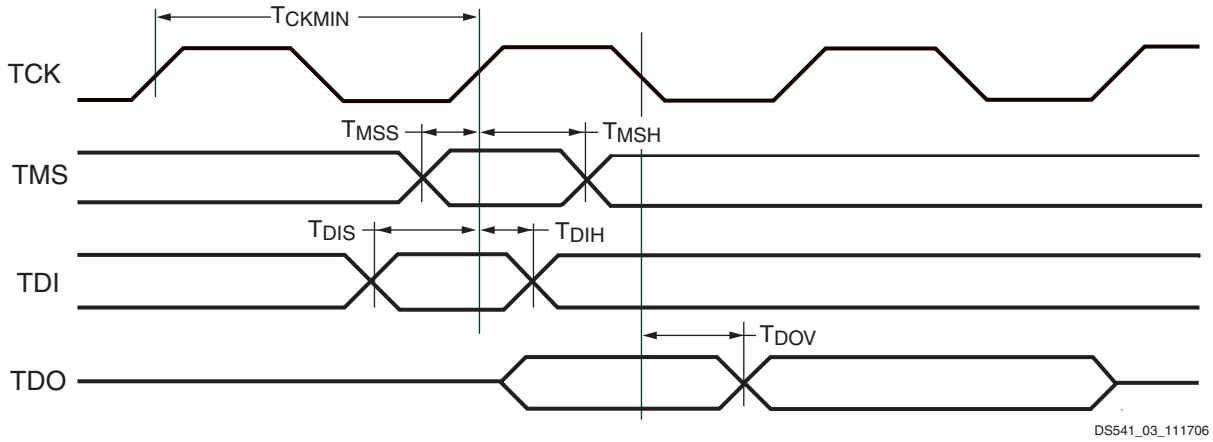


Figure 3: **Test Access Port Timing**

TAP AC Parameters

Table 5 shows the timing parameters for the TAP waveforms shown in Figure 3.

Table 5: **Test Access Port Timing Parameters**

Symbol	Description	Min	Max	Units
T_{CKMIN}	TCK minimum clock period when V_{CCJ} = 2.5V or 3.3V	100	–	ns
T_{MSS}	TMS setup time when V_{CCJ} = 2.5V or 3.3V	10	–	ns
T_{MSH}	TMS hold time when V_{CCJ} = 2.5V or 3.3V	25	–	ns
T_{DIS}	TDI setup time when V_{CCJ} = 2.5V or 3.3V	10	–	ns
T_{DIH}	TDI hold time when V_{CCJ} = 2.5V or 3.3V	25	–	ns
T_{DOV}	TDO valid delay when V_{CCJ} = 2.5V or 3.3V	–	30	ns

Additional Features for the XQF32P

Internal Oscillator

The 32-Mbit XQF32P Platform Flash PROMs include an optional internal oscillator which can be used to drive the CLKOUT and DATA pins on FPGA configuration interface. The internal oscillator can be enabled when programming the PROM, and the oscillator can be set to either the default frequency or to a slower frequency (XQF32P PROM as Configuration Master with Internal Oscillator as Clock Source, page 19).

CLKOUT

The 32-Mbit XQF32P Platform Flash PROMs include the programmable option to enable the CLKOUT signal which allows the PROM to provide a source synchronous clock aligned to the data on the configuration interface. The CLKOUT signal is derived from one of two clock sources: the CLK input pin or the internal oscillator. The input clock source is selected during the PROM programming sequence. Output data is available on the rising edge of CLKOUT.

The CLKOUT signal is enabled during programming, and is active when $\overline{CE}$ is Low and OE/$\overline{RESET}$ is High. On $\overline{CE}$ rising edge transition, if OE/$\overline{RESET}$ is High and the PROM terminal count has not been reached, then CLKOUT remains active for an additional eights clock cycles before being disabled. On a OE/$\overline{RESET}$ falling edge transition, CLKOUT is immediately disabled. When disabled, the CLKOUT pin is put into a high-impedance state and should be pulled High externally to provide a known state.

When cascading Platform Flash PROMs with CLKOUT enabled, after completing it's data transfer, the first PROM disables CLKOUT and drives the $\overline{CEO}$ pin enabling the next PROM in the PROM chain. The next PROM begins driving the CLKOUT signal once that PROM is enabled and data is available for transfer.

During high-speed parallel configuration without compression, the FPGA drives the BUSY signal on the configuration interface. When BUSY is asserted High, the PROMs internal address counter stops incrementing, and the current data value is held on the data outputs. While BUSY is High, the PROM continues driving the CLKOUT signal to the FPGA, clocking the FPGA’s configuration logic. When the FPGA deasserts BUSY, indicating that it is ready to receive additional configuration data, the PROM begins driving new data onto the configuration interface.

Decompression

The 32-Mbit XQF32P Platform Flash PROMs include a built-in data decompressor compatible with Xilinx advanced compression technology. Compressed Platform Flash PROM files are created from the target FPGA bitstream(s) using the iMPACT software. Only Slave Serial and Slave SelectMAP (parallel) configuration modes are supported for FPGA configuration when using a XQF32P PROM programmed with a compressed bitstream. Compression rates vary depending on several factors, including the target device family and the target design contents.

The decompression option is enabled during the PROM programming sequence. The PROM decompresses the stored data before driving both clock and data onto the FPGA's configuration interface. If Decompression is enabled, then the Platform Flash clock output pin (CLKOUT) must be used as the clock signal for the configuration interface, driving the target FPGA's configuration clock input pin (CCLK). Either the PROM's CLK input pin or the internal oscillator must be selected as the source for CLKOUT. Any target FPGA connected to the PROM must operate as slave in the configuration chain, with the configuration mode set to Slave Serial mode or Slave SelectMap (parallel) mode.

When decompression is enabled, the CLKOUT signal becomes a controlled clock output with a reduced maximum frequency. When decompressed data is not ready, the CLKOUT pin is put into a high-Z state and must be pulled High externally to provide a known state.

The BUSY input is automatically disabled when decompression is enabled.

Design Revisioning

Design Revisioning allows the user to create up to four unique design revisions on a single PROM or stored across multiple cascaded PROMs. Design Revisioning is supported for the XQF32P Platform Flash PROM in both serial and parallel modes. Design Revisioning can be used with compressed PROM files, and also when the CLKOUT feature is enabled. The PROM programming files along with the revision information files (`.cfi`) are created using the iMPACT software. The `.cfi` file is required to enable design revision programming in iMPACT.

A single design revision is composed of from 1 to *n* 8-Mbit memory blocks. If a single design revision contains less than 8 Mbits of data, then the remaining space is padded with all ones. A larger design revision can span several 8-Mbit memory blocks, and any space remaining in the last 8-Mbit memory block is padded with all ones.

- A single 32-Mbit PROM contains four 8-Mbit memory blocks, and can therefore store up to four separate design revisions: one 32-Mbit design revision, two 16-Mbit design revisions, three 8-Mbit design revisions, four 8-Mbit design revisions, and so on.
- Because of the 8-Mbit minimum size requirement for each revision, a single 16-Mbit PROM can only store up to two separate design revisions: one 16-Mbit design revision, one 8-Mbit design revision, or two 8-Mbit design revisions.
- A single 8-Mbit PROM can store only one 8-Mbit design revision.

Larger design revisions can be split over several cascaded PROMs. For example, two 32-Mbit PROMs can store up to four separate design revisions: one 64-Mbit design revision, two 32-Mbit design revisions, three 16-Mbit design revisions, four 16-Mbit design revisions, and so on.

See Figure 4 for a few basic examples of how multiple revisions can be stored. The design revision partitioning is handled automatically during file generation in iMPACT.

During the PROM file creation, each design revision is assigned a revision number:

Revision 0 = `00`
Revision 1 = `01`
Revision 2 = `10`
Revision 3 = `11`

After programming the Platform Flash PROM with a set of design revisions, a particular design revision can be selected using the external REV_SEL[1:0] pins or using the internal programmable design revision control bits. The $\overline{\text{EN\_EXT\_SEL}}$ pin determines if the external pins or internal bits are used to select the design revision. When $\overline{\text{EN\_EXT\_SEL}}$ is Low, design revision selection is controlled by the external Revision Select pins, REV_SEL[1:0]. When $\overline{\text{EN\_EXT\_SEL}}$ is High, design revision selection is controlled by the internal programmable Revision Select control bits. During power up, the design revision selection inputs (pins or control bits) are sampled internally. After power up, the design revision selection inputs are sampled again when any of the following events occur:

- On the rising edge of $\overline{\text{CE}}$
- On the falling edge of OE/$\overline{\text{RESET}}$ (when $\overline{\text{CE}}$ is Low)
- On the rising edge of $\overline{\text{CF}}$ (when $\overline{\text{CE}}$ is Low)
- When reconfiguration is initiated by using the JTAG CONFIG instruction.

The data from the selected design revision is then presented on the FPGA configuration interface.

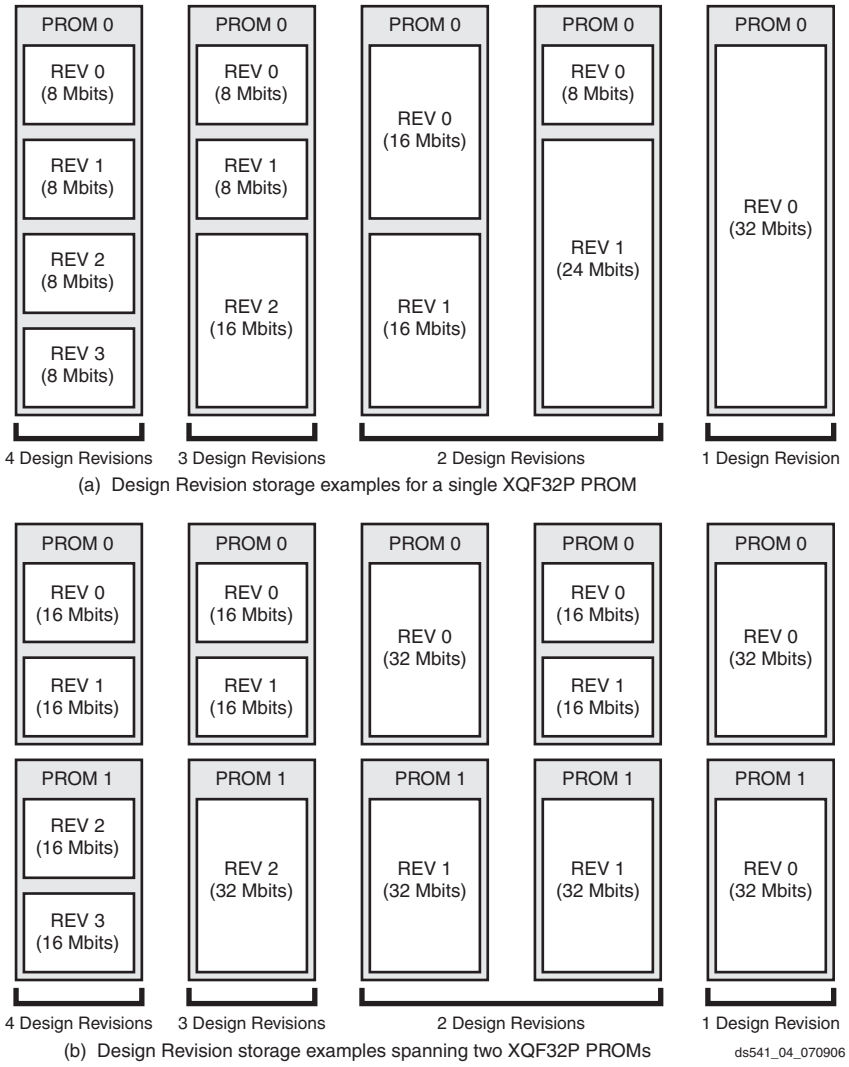


Figure 4: **Design Revision Storage Examples**

Initiating FPGA Configuration

The options for initiating FPGA configuration via the Platform Flash PROM include:

- Automatic configuration on power up
- Applying an external PROG_B (or $\overline{\text{PROGRAM}}$) pulse
- Applying the JTAG CONFIG instruction

Following the FPGA's power-on sequence or the assertion of the PROG_B (or $\overline{\text{PROGRAM}}$) pin the FPGA's configuration memory is cleared, the configuration mode is selected, and the FPGA is ready to accept a new configuration bitstream. The FPGA's PROG_B pin can be controlled by an external source, or alternatively, the Platform Flash PROMs incorporate a $\overline{\text{CF}}$ pin that can be tied to the FPGA's PROG_B pin. Executing the CONFIG instruction through JTAG pulses the $\overline{\text{CF}}$ output Low once for 300-500 ns, resetting the FPGA and initiating configuration. The iMPACT software can issue the JTAG CONFIG command to initiate FPGA configuration by setting the Load FPGA option.

When using the XQF32P Platform Flash PROM with design revisioning enabled, the $\overline{\text{CF}}$ pin should always be connected to the PROG_B (or $\overline{\text{PROGRAM}}$) pin on the FPGA to ensure that the current design revision selection is sampled when the FPGA is reset. The XQF32P PROM samples the current design revision selection from the external REV_SEL pins or the internal programmable Revision Select bits on the rising edge of $\overline{\text{CF}}$. When the JTAG CONFIG command is executed, the XQF32P samples the new design revision selection before initiating the FPGA configuration sequence. When using the XQF32P Platform Flash PROM without design revisioning, if the $\overline{\text{CF}}$ pin is not connected to the FPGA PROG_B (or $\overline{\text{PROGRAM}}$) pin, then the XQF32P $\overline{\text{CF}}$ pin must be tied High.

Reset and Power-On Reset Activation

At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified V_{CCINT} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on reset properly. During the power-up sequence, OE/$\overline{\text{RESET}}$ is held Low by the PROM. Once the required supplies have reached their respective POR (Power On Reset) thresholds, the OE/$\overline{\text{RESET}}$ release is delayed (T_{OER} minimum) to allow more margin for the power supplies to stabilize before initiating configuration. The OE/$\overline{\text{RESET}}$ pin is connected to an external 4.7 kΩ pull-up resistor and also to the target FPGA's INIT pin. For systems utilizing slow-rising power supplies, an additional power monitoring circuit can be used to delay the target configuration until the system power reaches minimum operating voltages by holding the OE/$\overline{\text{RESET}}$ pin Low. When OE/$\overline{\text{RESET}}$ is released, the FPGA's INIT pin is pulled High allowing the FPGA's configuration sequence to begin. If the power drops below the power-down threshold (V_{CCPD}), the PROM resets and OE/$\overline{\text{RESET}}$ is again held Low until the after the POR threshold is reached. OE/$\overline{\text{RESET}}$ polarity is not programmable. These power-up requirements are shown graphically in Figure 5.

For a fully powered Platform Flash PROM, a reset occurs whenever OE/$\overline{\text{RESET}}$ is asserted (Low) or $\overline{\text{CE}}$ is deasserted (High). The address counter is reset, $\overline{\text{CEO}}$ is driven High, and the remaining outputs are placed in a high-impedance state.

Note: The XQF32P PROM requires both V_{CCINT} to rise above its POR threshold and for V_{CCO} to reach the recommended operating voltage level before releasing OE/$\overline{\text{RESET}}$.

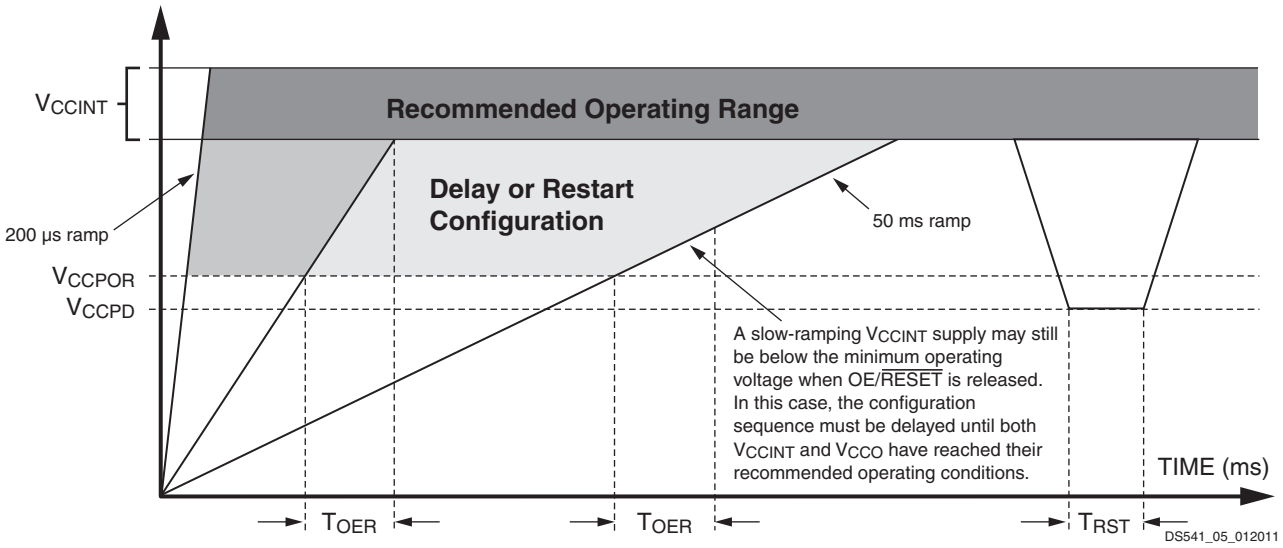


Figure 5: **Platform Flash PROM Power-Up Requirements**

I/O Input Voltage Tolerance and Power Sequencing

The I/Os on each re-programmable Platform Flash PROM are fully 3.3V tolerant. This allows 3V CMOS signals to connect directly to the inputs without damage. The core power supply (V_{CCINT}), JTAG pin power supply (V_{CCJ}), output power supply (V_{CCO}), and external 3V CMOS I/O signals can be applied in any order.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{\text{CE}}$ is deasserted (High). In standby mode, the address counter is reset, $\overline{\text{CEO}}$ is driven High, and the remaining outputs are placed in a high-impedance state regardless of the state of the OE/$\overline{\text{RESET}}$ input. For the device to remain in the low-power standby mode, the JTAG pins TMS, TDI, and TDO must not be pulled Low, and TCK must be stopped (High or Low).

When using the FPGA DONE signal to drive the PROM $\overline{\text{CE}}$ pin High to reduce standby power after configuration, an external pull-up resistor should be used. Typically a 330Ω pull-up resistor is used, but refer to the appropriate FPGA data sheet for the recommended DONE pin pull-up value. If the DONE circuit is connected to an LED to indicate FPGA configuration is complete, and is also connected to the PROM $\overline{\text{CE}}$ pin to enable low-power standby mode, then an external buffer should be used to drive the LED circuit to ensure valid transitions on the PROM's $\overline{\text{CE}}$ pin. If low-power standby mode is not required for the PROM, then the $\overline{\text{CE}}$ pin should be connected to ground.

Table 6 shows the truth table of the XQF32P PROM inputs and outputs.

Table 6: **Truth Table for XQF32P PROM Control Inputs**

Control Inputs				Internal Address	Outputs			
OE/$\overline{\text{RESET}}$	**$\overline{\text{CE}}$**	**$\overline{\text{CF}}$**	**BUSY(5)**		**DATA**	**$\overline{\text{CEO}}$**	**CLKOUT**	**ICC**
High	Low	High	Low	If address < TC(2) and address < EA(3) : increment	Active	High	Active	Active
				If address < TC(2) and address = EA(3) : don't change	High-Z	High	High-Z	Reduced
				Else If address = TC(2) : don't change	High-Z	Low	High-Z	Reduced
High	Low	High	High	Unchanged	Active and Unchanged	High	Active	Active
High	Low	↑	X(1)	Reset(4)	Active	High	Active	Active
Low	Low	X(1)	X(1)	Held reset(4)	High-Z	High	High-Z	Active
X(1)	High	X(1)	X(1)	Held reset(4)	High-Z	High	High-Z	Standby

Notes:

1. X = don't care.
2. TC = Terminal Count = highest address value.
3. For the XQF32P with Design Revisioning enabled, EA = end address (last address in the selected design revision).
4. For the XQF32P with Design Revisioning enabled, Reset = address reset to the beginning address of the selected bank. If Design Revisioning is not enabled, then Reset = address reset to address 0.
5. The BUSY input is only enabled when the XQF32P is programmed for parallel data output and decompression is not enabled.

DC Electrical Characteristics

Absolute Maximum Ratings

Table 7: **Absolute Maximum Ratings**

Symbol	Description	XQF32P	Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to +2.7	V
V_{CCO}	I/O supply voltage relative to GND	–0.5 to +4.0	V
V_{CCJ}	JTAG I/O supply voltage relative to GND	–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to +3.6	V
V_{TS}	Voltage applied to High-Z output	–0.5 to +3.6	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_J	Junction temperature	+125	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins can undershoot to –2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
3. For soldering guidelines, see UG112, Device Packaging and Thermal Characteristics as well as other information at www.xilinx.com.

Supply Voltage Requirements for Power-On Reset and Power-Down

Table 8: **Supply Voltage Requirements for Power-On Reset and Power-Down**

Symbol	Description	XQF32P		Units
		Min	Max	
T_{VCC}	V_{CCINT} rise time from 0V to nominal voltage(2)	0.2	50	ms
V_{CCPOR}	POR threshold for the V_{CCINT} supply	0.5	–	V
T_{OER}	OE/$\overline{\text{RESET}}$ release delay following POR(3)	0.5	30	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply	–	0.5	V
T_{RST}	Time required to trigger a device reset when the VCCINT supply drops below the maximum V_{CCPD} threshold	10	–	ms

Notes:

1. V_{CCINT}, V_{CCO}, and V_{CCJ} supplies can be applied in any order.
2. At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified T_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 5, page 10.
3. If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the OE/$\overline{\text{RESET}}$ pin is released, then the configuration data from the PROM is not be available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.

Recommended Operating Conditions

Table 9: **Recommended Operating Conditions**

Symbol	Description		XQF32P			Units
			Min	Typ	Max	
V_{CCINT}	Internal voltage supply		1.65	1.8	2.0	V
V_{CCO}	Supply voltage for output drivers	3.3V Operation	3.0	3.3	3.6	V
		2.5V Operation	2.3	2.5	2.7	V
		1.8V Operation	1.7	1.8	1.9	V
V_{CCJ}	Supply voltage for JTAG output drivers	3.3V Operation	3.0	3.3	3.6	V
		2.5V Operation	2.3	2.5	2.7	V
V_{IL}	Low-level input voltage	3.3V Operation	0	–	0.8	V
		2.5V Operation	0	–	0.7	V
		1.8V Operation	–	–	20% V_{CCO}	V
V_{IH}	High-level input voltage	3.3V Operation	2.0	–	3.6	V
		2.5V Operation	1.7	–	3.6	V
		1.8V Operation	70% V_{CCO}	–	3.6	V
T_{IN}	Input signal transition time(1)		–	–	500	ns
V_O	Output voltage		0	–	V_{CCO}	V
T_A	Operating ambient temperature		–55		125	°C

Notes:

1. Input signal transition time measured between 10% V_{CCO} and 90% V_{CCO}.

Quality and Reliability Characteristics

Table 10: **Quality and Reliability Characteristics**

Symbol	Description	Min	Max	Units
T_{DR}	Data retention	20	–	Years
N_{PE}	Program/erase cycles (Endurance)	20,000	–	Cycles
V_{ESD}	Electrostatic discharge (ESD)	2,000	–	V

DC Characteristics Over Operating Conditions

Table 11: **DC Characteristics Over Operating Conditions**

Symbol	Description	XQF32P			Units
		Test Conditions	Min	Max	
V_{OH}	High-level output voltage for 3.3V outputs	I_{OH} = –4 mA	2.4	–	V
	High-level output voltage for 2.5V outputs	I_{OH} = –500 µA	V_{CCO} – 0.4	–	V
	High-level output voltage for 1.8V outputs	I_{OH} = –50 µA	V_{CCO} – 0.4	–	V
V_{OL}	Low-level output voltage for 3.3V outputs	I_{OL} = 4 mA	–	0.4	V
	Low-level output voltage for 2.5V outputs	I_{OL} = 500 µA	–	0.4	V
	Low-level output voltage for 1.8V outputs	I_{OL} = 50 µA	–	0.4	V
I_{CCINT}	Internal voltage supply current, active mode	33 MHz	–	10	mA
I_{CCO} (1)	Output driver supply current, active serial mode	33 MHz	–	10	mA
	Output driver supply current, active parallel mode	33 MHz	–	40	mA
I_{CCJ}	JTAG supply current, active mode	Note (2)	–	5	mA
I_{CCINTS}	Internal voltage supply current, standby mode	Note (3)	–	1	mA
I_{CCOS}	Output driver supply current, standby mode	Note (3)	–	1	mA
I_{CCJS}	JTAG supply current, standby mode	Note (3)	–	1	mA
I_{ILJ}	JTAG pins TMS, TDI, and TDO pull-up current	V_{CCJ} = Max V_{IN} = GND	–	100	µA
I_{IL}	Input leakage current	V_{CCINT} = Max V_{CCO} = Max V_{IN} = GND or V_{CCO}	–10	10	µA
I_{IH}	Input and output High-Z leakage current	V_{CCINT} = Max V_{CCO} = Max V_{IN} = GND or V_{CCO}	–10	10	µA
I_{ILP}	Source current through internal pull-ups on $\overline{EN\_EXT\_SEL}$, REV_SEL0, REV_SEL1	V_{CCINT} = Max V_{CCO} = Max V_{IN} = GND or V_{CCO}	–	100	µA
I_{IHP}	Sink current through internal pull-down on BUSY	V_{CCINT} = Max V_{CCO} = Max V_{IN} = GND or V_{CCO}	–100	–	µA
C_{IN}	Input capacitance	V_{IN} = GND f = 1.0 MHz	–	8	pF
C_{OUT}	Output capacitance	V_{IN} = GND f = 1.0 MHz	–	14	pF

Notes:

1. Output driver supply current specification based on no-load conditions.
2. TDI/TMS/TCK non-static (active).
3. $\overline{CE}$ High, OE Low, and TMS/TDI/TCK static.

AC Electrical Characteristics

AC Characteristics Over Operating Conditions

XQF32P PROM as Configuration Slave with CLK Input Pin as Clock Source

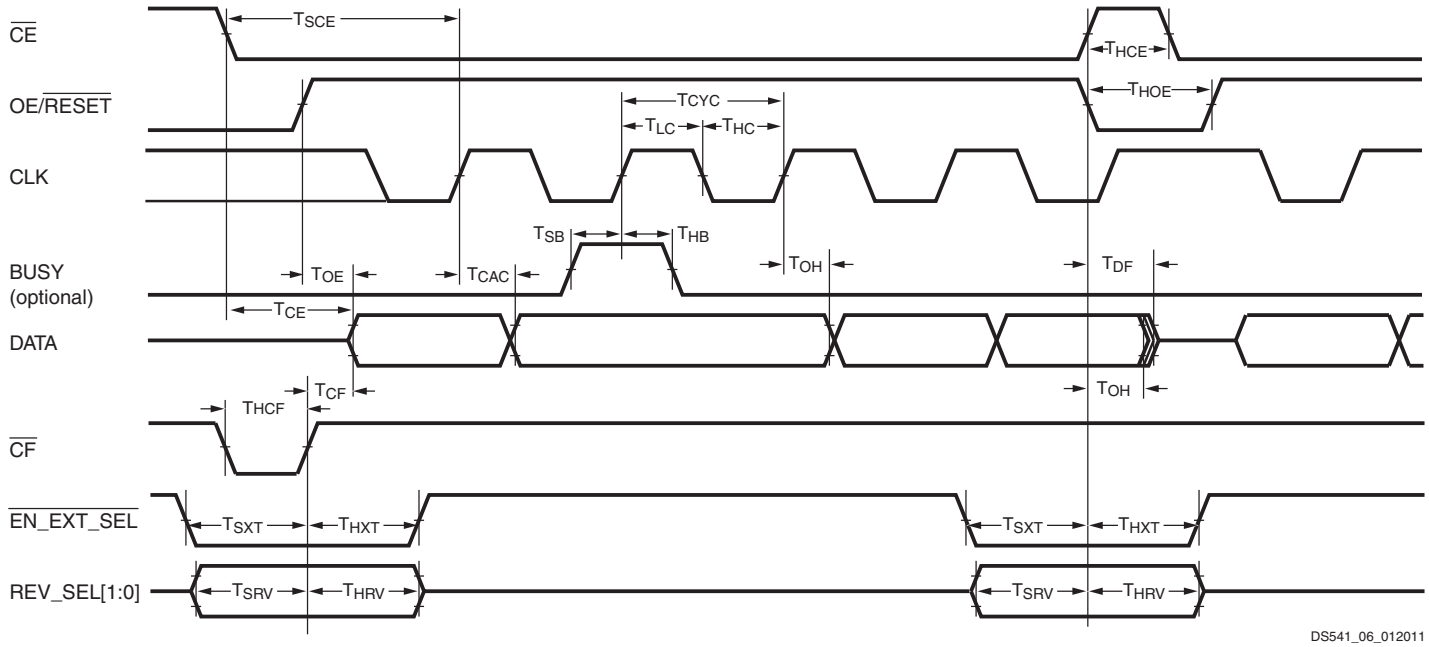


Figure 6: **XQF32P PROM as Configuration Slave with CLK Input Pin as Clock Source**

Table 12: **XQF32P PROM as Configuration Slave with CLK Input Pin as Clock Source**

Symbol	Description	XQF32P		Units
		Min	Max	
T_{HCF}	$\overline{CF}$ hold time to guarantee design revision selection is sampled when V_{CCO} = 3.3V or 2.5V(9)	300	–	ns
	$\overline{CF}$ hold time to guarantee design revision selection is sampled when V_{CCO} = 1.8V(9)	300	–	ns
T_{CF}	$\overline{CF}$ to data delay when VCCO = 3.3V or 2.5V(8)	–	25	ns
	$\overline{CF}$ to data delay when VCCO = 1.8V(8)	–	25	ns
T_{OE}	OE/$\overline{RESET}$ to data delay(5) when V_{CCO} = 3.3V or 2.5V	–	30	ns
	OE/$\overline{RESET}$ to data delay(5) when V_{CCO} = 1.8V	–	30	ns
T_{CE}	$\overline{CE}$ to data delay(4) when V_{CCO} = 3.3V or 2.5V	–	30	ns
	$\overline{CE}$ to data delay(4) when V_{CCO} = 1.8V	–	30	ns
T_{CAC}	CLK to data delay(7) when V_{CCO} = 3.3V or 2.5V	–	30	ns
	CLK to data delay(7) when V_{CCO} = 1.8V	–	30	ns
T_{OH}	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, CLK, or $\overline{CF}$ when V_{CCO} = 3.3V or 2.5V(8)	5	–	ns
	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, CLK, or $\overline{CF}$ when V_{CCO} = 1.8V(8)	5	–	ns
T_{DF}	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay(2) when V_{CCO} = 3.3V or 2.5V	–	45	ns
	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay(2) when V_{CCO} = 1.8V	–	45	ns

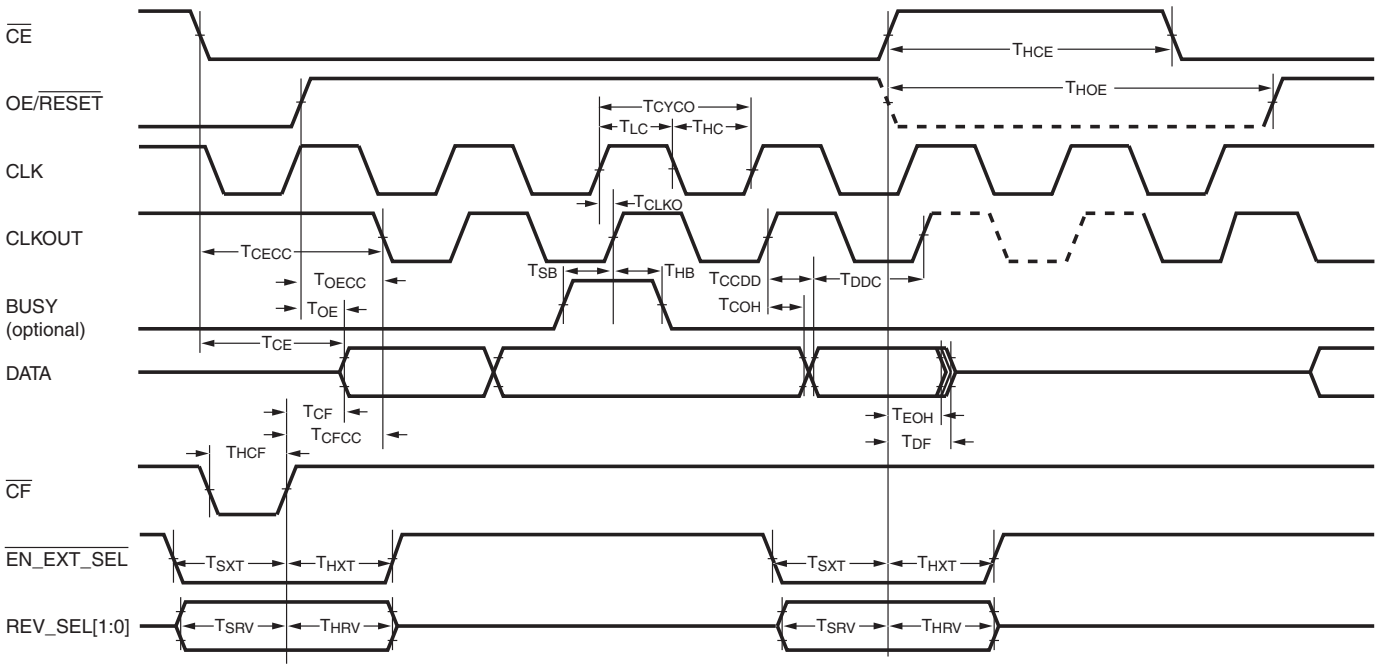
Table 12: **XQF32P PROM as Configuration Slave with CLK Input Pin as Clock Source *(Cont'd)***

Symbol	Description	XQF32P		Units
		Min	Max	
T_{CYC}	Clock period(6) (serial mode) when V_{CCO} = 3.3V or 2.5V	30	–	ns
	Clock period(6) (serial mode) when V_{CCO} = 1.8V	30	–	ns
	Clock period(6) (parallel mode) when V_{CCO} = 3.3V or 2.5V	35	–	ns
	Clock period(6) (parallel mode) when V_{CCO} = 1.8V	35	–	ns
T_{LC}	CLK Low time(3) when V_{CCO} = 3.3V or 2.5V	12	–	ns
	CLK Low time(3) when V_{CCO} = 1.8V	12	–	ns
T_{HC}	CLK High time(3) when V_{CCO} = 3.3V or 2.5V	12	–	ns
	CLK High time(3) when V_{CCO} = 1.8V	12	–	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (guarantees proper counting)(3) when V_{CCO} = 3.3V or 2.5V	30	–	ns
	$\overline{CE}$ setup time to CLK (guarantees proper counting)(3) when V_{CCO} = 1.8V	30	–	ns
T_{HCE}	$\overline{CE}$ hold time (guarantees counters are reset)(4) when V_{CCO} = 3.3V or 2.5V	2000	–	ns
	$\overline{CE}$ hold time (guarantees counters are reset)(4) when V_{CCO} = 1.8V	2000	–	ns
T_{HOE}	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 3.3V or 2.5V	2000	–	ns
	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 1.8V	2000	–	ns
T_{SB}	BUSY setup time to CLK when V_{CCO} = 3.3V or 2.5V(8)	12	–	ns
	BUSY setup time to CLK when V_{CCO} = 1.8V(8)	12	–	ns
T_{HB}	BUSY hold time to CLK when V_{CCO} = 3.3V or 2.5V(8)	8	–	ns
	BUSY hold time to CLK when V_{CCO} = 1.8V(8)	8	–	ns
T_{SXT}	$\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V(8)	300	–	ns
	$\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 1.8V(8)	300	–	ns
T_{HXT}	$\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V(8)	300	–	ns
	$\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 1.8V(8)	300	–	ns
T_{SRV}	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V(8)	300	–	ns
	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 1.8V(8)	300	–	ns
T_{HRV}	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V(8)	300	–	ns
	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 1.8V(8)	300	–	ns

Notes:

1. AC test load = 30 pF for XQF32P.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady-state active levels.
3. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
4. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
5. If T_{HOE} Low < 2 µs, T_{OE} = 2 µs.
6. This is the minimum possible T_{CYC}. Actual T_{CYC} = T_{CAC} + FPGA Data setup time. Example: With the XCF32P in serial mode with V_{CCO} at 3.3V, if FPGA data setup time = 15 ns, then the actual T_{CYC} = 25 ns +15 ns = 40 ns.
7. Guaranteed by design; not tested.
8. CF, EN_EXT_SEL, REV_SEL[1:0], and BUSY are inputs.
9. When JTAG CONFIG command is issued, PROM drives CF Low for at least the T_{HCF} minimum.

XQF32P PROM as Configuration Master with CLK Input Pin as Clock Source



Note: 8 CLKOUT cycles are output after $\overline{CE}$ rising edge, before CLKOUT is 3-stated, if OE/$\overline{RESET}$ remains High, and terminal count has not been reached.

Figure 7: **XQF32P PROM as Configuration Master with CLK Input Pin as Clock Source**

Table 13: **XQF32P PROM as Configuration Master with CLK Input Pin as Clock Source**

Symbol	Description	XQF32P		Units
		Min	Max	
T_{HCF}	$\overline{CF}$ hold time to guarantee design revision selection is sampled when V_{CCO} = 3.3V or 2.5V(11)	300	–	ns
	$\overline{CF}$ hold time to guarantee design revision selection is sampled when V_{CCO} = 1.8V(11)	300	–	ns
T_{CF}	$\overline{CF}$ to data delay when V_{CCO} = 3.3V or 2.5V	–	25	ns
	$\overline{CF}$ to data delay when V_{CCO} = 1.8V	–	25	ns
T_{OE}	OE/$\overline{RESET}$ to data delay(6) when V_{CCO} = 3.3V or 2.5V	–	30	ns
	OE/$\overline{RESET}$ to data delay(6) when V_{CCO} = 1.8V	–	30	ns
T_{CE}	$\overline{CE}$ to data delay(5) when V_{CCO} = 3.3V or 2.5V	–	30	ns
	$\overline{CE}$ to data delay(5) when V_{CCO} = 1.8V	–	30	ns
T_{EOH}	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, or $\overline{CF}$ when V_{CCO} = 3.3V or 2.5V	5	–	ns
	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, or $\overline{CF}$ when V_{CCO} = 1.8V	5	–	ns
T_{DF}	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay(2) when V_{CCO} = 3.3V or 2.5V	–	45	ns
	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay(2) when V_{CCO} = 1.8V	–	45	ns
T_{CYCO}	Clock period(7) (serial mode) when V_{CCO} = 3.3V or 2.5V	30	–	ns
	Clock period(7) (serial mode) when V_{CCO} = 1.8V	30	–	ns
	Clock period(7) (parallel mode) when V_{CCO} = 3.3V or 2.5V	35	–	ns
	Clock period(7) (parallel mode) when V_{CCO} = 1.8V	35	–	ns

Table 13: **XQF32P PROM as Configuration Master with CLK Input Pin as Clock Source *(Cont'd)***

Symbol	Description	XQF32P		Units
		Min	Max	
T_{LC}	CLK Low time(3) when V_{CCO} = 3.3V or 2.5V	12	–	ns
	CLK Low time(3) when V_{CCO} = 1.8V	12	–	ns
T_{HC}	CLK High time(3) when V_{CCO} = 3.3V or 2.5V	12	–	ns
	CLK High time(3) when V_{CCO} = 1.8V	12	–	ns
T_{HCE}	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 3.3V or 2.5V	2000	–	ns
	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 1.8V	2000	–	ns
T_{HOE}	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 3.3V or 2.5V	2000	–	ns
	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 1.8V	2000	–	ns
T_{SB}	BUSY setup time to CLKOUT when V_{CCO} = 3.3V or 2.5V	12	–	ns
	BUSY setup time to CLKOUT when V_{CCO} = 1.8V	12	–	ns
T_{HB}	BUSY hold time to CLKOUT when V_{CCO} = 3.3V or 2.5V	8	–	ns
	BUSY hold time to CLKOUT when V_{CCO} = 1.8V	8	–	ns
T_{CLKO}	CLK input to CLKOUT output delay when V_{CCO} = 3.3V or 2.5V	–	35	ns
	CLK input to CLKOUT output delay when V_{CCO} = 1.8V	–	35	ns
	CLK input to CLKOUT output delay when V_{CCO} = 3.3V or 2.5V with decompression(10)	–	35	ns
	CLK input to CLKOUT output delay when V_{CCO} = 1.8V with decompression(10)	–	35	ns
T_{CECC}	$\overline{CE}$ to CLKOUT delay(8) when V_{CCO} = 3.3V or 2.5V	0	2 CLK cycles	–
	$\overline{CE}$ to CLKOUT delay(8) when V_{CCO} = 1.8V	0	2 CLK cycles	–
T_{OECC}	OE/$\overline{RESET}$ to CLKOUT delay(8) when V_{CCO} = 3.3V or 2.5V	0	2 CLK cycles	–
	OE/$\overline{RESET}$ to CLKOUT delay(8) when V_{CCO} = 1.8V	0	2 CLK cycles	–
T_{CFCC}	$\overline{CF}$ to CLKOUT delay(8) when V_{CCO} = 3.3V or 2.5V	0	–	ns
	$\overline{CF}$ to CLKOUT delay(8) when V_{CCO} = 1.8V	0	–	ns
T_{CCDD}	CLKOUT to data delay when V_{CCO} = 3.3V or 2.5V(9)	–	32	ns
	CLKOUT to data delay when V_{CCO} = 1.8V(9)	–	32	ns
T_{DDC}	Data setup time to CLKOUT when V_{CCO} = 3.3V or 2.5V with decompression(9)(10)	5	–	ns
	Data setup time to CLKOUT when V_{CCO} = 1.8V with decompression(9)(10)	5	–	ns
T_{COH}	Data hold from CLKOUT when V_{CCO} = 3.3V or 2.5V	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 1.8V	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 3.3V or 2.5V with decompression(10)	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 1.8V with decompression(10)	3	–	ns
T_{SXT}	$\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	$\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
T_{HXT}	$\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	$\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
T_{SRV}	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns

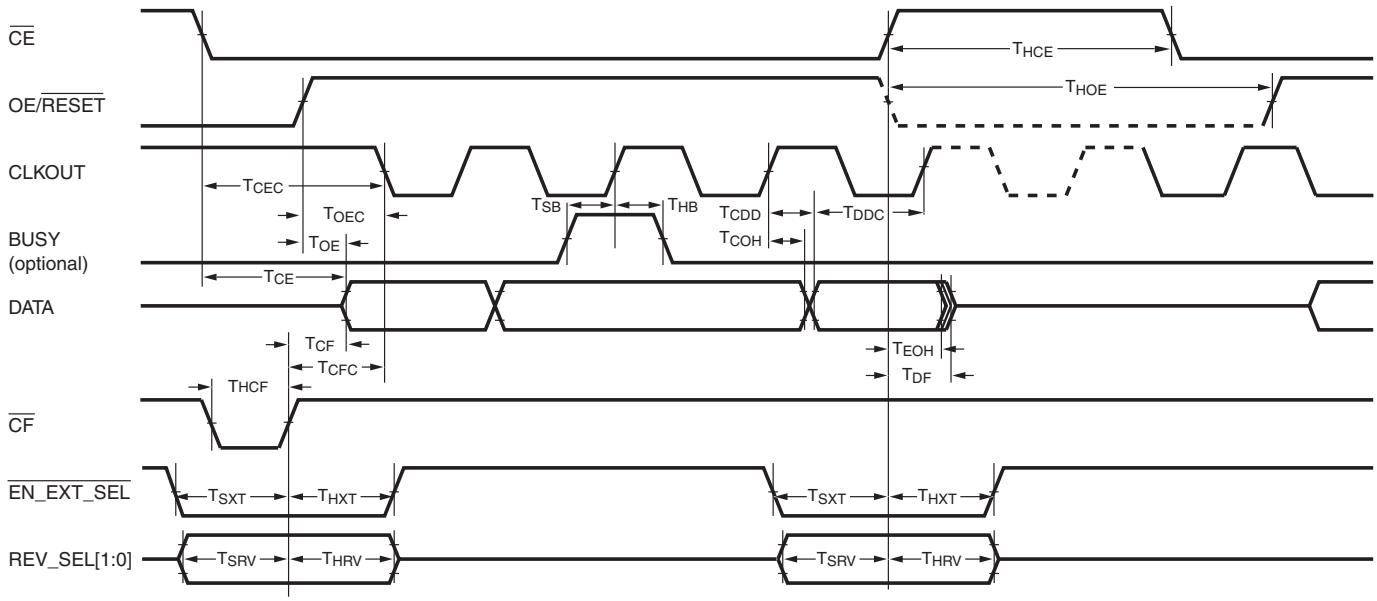
Table 13: **XQF32P PROM as Configuration Master with CLK Input Pin as Clock Source *(Cont'd)***

Symbol	Description	XQF32P		Units
		Min	Max	
T_{HRV}	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns

Notes:

1. AC test load = 30 pF for XQF32P.
2. Float delays are measured with 5 pF AC loads.Transition is measured at ±200 mV from steady-state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
6. If T_{HOE} Low < 2 µs, T_{OE} = 2 µs.
7. This is the minimum possible T_{CYCO}. Actual $T_{CYCO} = T_{CCDD}$ + FPGA Data setup time. *Example:* With the XQF32P in serial mode with V_{CCO} at 3.3V, if FPGA Data setup time = 15 ns, then the actual T_{CYCO} = 25 ns +15 ns = 40 ns.
8. The delay before the enabled CLKOUT signal begins clocking data out of the device is dependent on the clocking configuration. The delay before CLKOUT is enabled increases if decompression is enabled.
9. Slower CLK frequency option can be required to meet the FPGA data sheet setup time.
10. When decompression is enabled, the CLKOUT signal becomes a controlled clock output. When decompressed data is available, CLKOUT toggles at ½ the source clock frequency (either ½ the selected internal clock frequency or ½ the external CLK input frequency). When decompressed data is not available, the CLKOUT pin is parked High. If CLKOUT is used, then it must be pulled High externally using a 4.7kΩ pull-up to V_{CCO}.
11. When JTAG CONFIG command is issued, PROM drives $\overline{CF}$ Low for at least the T_{HCF} minimum.

XQF32P PROM as Configuration Master with Internal Oscillator as Clock Source



Note: 8 CLKOUT cycles are output after $\overline{CE}$ rising edge, before CLKOUT is 3-stated, if OE/$\overline{RESET}$ remains High, and terminal count has not been reached.

DS541_08_020811

Figure 8: **XQF32P PROM as Configuration Master with Internal Oscillator as Clock Source**

Table 14: **XQF32P PROM as Configuration Master with Internal Oscillator as Clock Source**

Symbol	Description	XQF32P		Units
		Min	Max	
T_{HCF}	$\overline{CF}$ hold time to guarantee design revision selection is sampled when V_{CCO} = 3.3V or 2.5V(12)	300	–	ns
	$\overline{CF}$ hold time to guarantee design revision selection is sampled when V_{CCO} = 1.8V(12)	300	–	ns
T_{CF}	$\overline{CF}$ to data delay when V_{CCO} = 3.3V or 2.5V	–	25	ns
	$\overline{CF}$ to data delay when V_{CCO} = 1.8V	–	25	ns
T_{OE}	OE/$\overline{RESET}$ to data delay(6) when V_{CCO} = 3.3V or 2.5V	–	30	ns
	OE/$\overline{RESET}$ to data delay(6) when V_{CCO} = 1.8V	–	30	ns
T_{CE}	$\overline{CE}$ to data delay(5) when V_{CCO} = 3.3V or 2.5V	–	30	ns
	$\overline{CE}$ to data delay(5) when V_{CCO} = 1.8V	–	30	ns
T_{EOH}	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, or $\overline{CF}$ when V_{CCO} = 3.3V or 2.5V	5	–	ns
	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, or $\overline{CF}$ when V_{CCO} = 1.8V	5	–	ns
T_{DF}	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay(2) when V_{CCO} = 3.3V or 2.5V	–	45	ns
	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay(2) when V_{CCO} = 1.8V	–	45	ns
T_{HCE}	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 3.3V or 2.5V	2000	–	ns
	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 1.8V	2000	–	ns
T_{HOE}	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 3.3V or 2.5V	2000	–	ns
	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 1.8V	2000	–	ns
T_{SB}	BUSY setup time to CLKOUT when V_{CCO} = 3.3V or 2.5V	12	–	ns
	BUSY setup time to CLKOUT when V_{CCO} = 1.8V	12	–	ns
T_{HB}	BUSY hold time to CLKOUT when V_{CCO} = 3.3V or 2.5V	8	–	ns
	BUSY hold time to CLKOUT when V_{CCO} = 1.8V	8	–	ns
T_{CEC}	$\overline{CE}$ to CLKOUT delay(7) when V_{CCO} = 3.3V or 2.5V	0	1	µs
	$\overline{CE}$ to CLKOUT delay(7) when V_{CCO} = 1.8V	0	1	µs
T_{OEC}	OE/$\overline{RESET}$ to CLKOUT delay(7) when V_{CCO} = 3.3V or 2.5V	0	1	µs
	OE/$\overline{RESET}$ to CLKOUT delay(7) when V_{CCO} = 1.8V	0	1	µs
T_{CFC}	$\overline{CF}$ to CLKOUT delay(7) when V_{CCO} = 3.3V or 2.5V	0	–	ns
	$\overline{CF}$ to CLKOUT delay(7) when V_{CCO} = 1.8V	0	–	ns
T_{CDD}	CLKOUT to data delay when V_{CCO} = 3.3V or 2.5V(8)	–	30	ns
	CLKOUT to data delay when V_{CCO} = 1.8V(8)	–	30	ns
T_{DDC}	Data setup time to CLKOUT when V_{CCO} = 3.3V or 2.5V with decompression(8)(11)	5	–	ns
	Data setup time to CLKOUT when V_{CCO} = 1.8V with decompression(8)(11)	5	–	ns
T_{COH}	Data hold from CLKOUT when V_{CCO} = 3.3V or 2.5V	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 1.8V	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 3.3V or 2.5V with decompression(11)	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 1.8V with decompression(11)	3	–	ns
T_{SXT}	$\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	$\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
T_{HXT}	$\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	$\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns

Table 14: **XQF32P PROM as Configuration Master with Internal Oscillator as Clock Source *(Cont'd)***

Symbol	Description	XQF32P		Units
		Min	Max	
T_{SRV}	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
T_{HRV}	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
FF	CLKOUT default (fast) frequency(9)	25	50	MHz
	CLKOUT default (fast) frequency with decompression(11)	12.5	25	MHz
FS	CLKOUT alternate (slower) frequency(10)	12.5	25	MHz
	CLKOUT alternate (slower) frequency with decompression(11)	6	12.5	MHz

Notes:

1. AC test load = 30 pF for XQF32P.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady-state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
6. If T_{HOE} Low < 2 µs, T_{OE} = 2 µs.
7. The delay before the enabled CLKOUT signal begins clocking data out of the device is dependent on the clocking configuration. The delay before CLKOUT is enabled increases if decompression is enabled.
8. Slower CLK frequency option can be required to meet the FPGA data sheet setup time.
9. Typical CLKOUT default (fast) period = 25 ns (40 MHz)
10. Typical CLKOUT alternate (slower) period = 50 ns (20 MHz)
11. When decompression is enabled, the CLKOUT signal becomes a controlled clock output. When decompressed data is available, CLKOUT toggles at ½ the source clock frequency (either ½ the selected internal clock frequency or ½ the external CLK input frequency). When decompressed data is not available, the CLKOUT pin is parked High. If CLKOUT is used, then it must be pulled High externally using a 4.7kΩ pull-up to V_{CCO}.
12. When JTAG CONFIG command is issued, PROM drives CF Low for at least the THCF minimum.

AC Characteristics Over Operating Conditions When Cascading

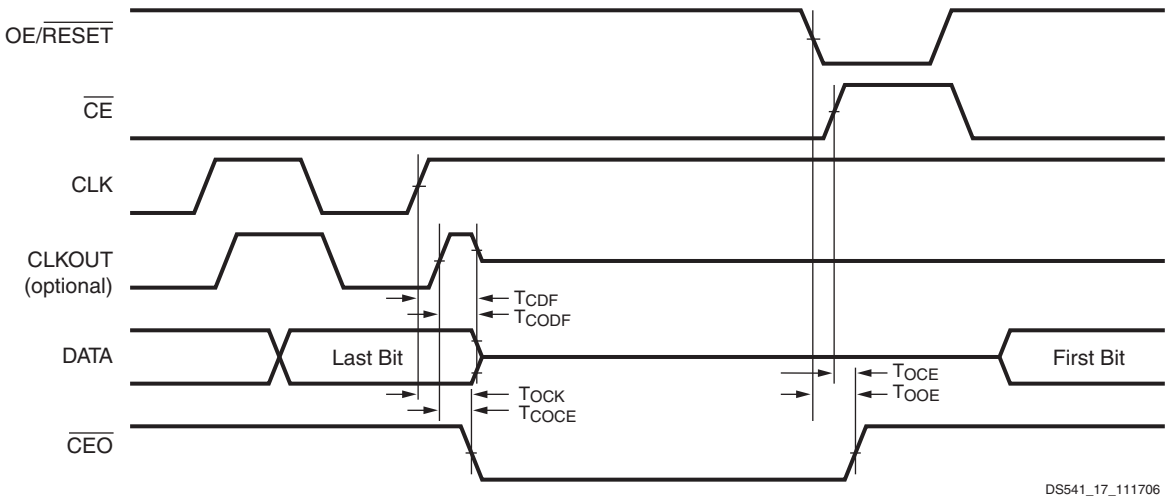


Figure 9: **AC Characteristics Over Operating Conditions When Cascading**

Table 15: **AC Characteristics Over Operating Conditions When Cascading**

Symbol	Description	XQF32P		Units
		Min	Max	
T_{CDF}	CLK to output float delay(2)(3) when V_{CCO} = 2.5V or 3.3V	–	25	ns
	CLK to output float delay(2)(3) when V_{CCO} = 1.8V	–	25	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)(5) when V_{CCO} = 2.5V or 3.3V	–	20	ns
	CLK to $\overline{CEO}$ delay(3)(5) when V_{CCO} = 1.8V	–	20	ns
T_{OCE}	$\overline{CE}$ to $\overline{CEO}$ delay(3)(6) when V_{CCO} = 2.5V or 3.3V	–	80	ns
	$\overline{CE}$ to $\overline{CEO}$ delay(3)(6) when V_{CCO} = 1.8V	–	80	ns
T_{OOE}	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 2.5V or 3.3V	–	80	ns
	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 1.8V	–	80	ns
T_{COCE}	CLKOUT to $\overline{CEO}$ delay when V_{CCO} = 2.5V or 3.3V	–	25	ns
	CLKOUT to $\overline{CEO}$ delay when V_{CCO} = 1.8V	–	25	ns
T_{CODF}	CLKOUT to output float delay when V_{CCO} = 2.5V or 3.3V	–	30	ns
	CLKOUT to output float delay when V_{CCO} = 1.8V	–	30	ns

Notes:

1. AC test load = 30 pF for XQF32P.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. For cascaded PROMs, if the FPGA's dual-purpose configuration data pins are set to persist as configuration pins, the minimum period is increased based on the CLK to $\overline{CEO}$ and $\overline{CE}$ to data propagation delays:
   - T_{CYC} minimum = T_{OCK} + T_{CE} + FPGA Data setup time.
   - T_{CAC} maximum = T_{OCK} + T_{CE}
6. For cascaded PROMs, if the FPGA's dual-purpose configuration data pins become general I/O pins after configuration; to allow for the disable to propagate to the cascaded PROMs and to avoid contention on the data lines following configuration, the minimum period is increased based on the $\overline{CE}$ to $\overline{CEO}$ and $\overline{CE}$ to data propagation delays:
   - T_{CYC} minimum = T_{OCE} + T_{CE}
   - T_{CAC} maximum = T_{OCK} + T_{CE}

Pinouts and Pin Descriptions

XQF32P VOG48 Pin Names and Descriptions

The XQF32P Platform Flash PROM is available in the VOG48 package. Table 16 provides a list of the pin names and descriptions for the XQF32P 48-pin VOG48 plastic, thin, small outline package (TSOP).

Table 16: **XQF32P Pin Names and Descriptions (VOG48)**

Pin Name	Boundary Scan Order	Boundary Scan Function	Pin Description	48-pin TSOP VOG48
D0	28	Data Out	D0 is the DATA output pin to provide data for configuring an FPGA in serial mode. D0-D7 are the DATA output pins to provide parallel data for configuring a Xilinx FPGA in SelectMap (parallel) mode. The D0 output is set to a high-impedance state during ISPEN (when not clamped). The D1-D7 outputs are set to a high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. The D1-D7 pins can be left unconnected when the PROM is used in serial mode.	28
	27	Output Enable		
D1	26	Data Out		29
	25	Output Enable		
D2	24	Data Out		32
	23	Output Enable		
D3	22	Data Out		33
	21	Output Enable		
D4	20	Data Out		43
	19	Output Enable		
D5	18	Data Out		44
	17	Output Enable		
D6	16	Data Out		47
	15	Output Enable		
D7	14	Data Out		48
	13	Output Enable		
CLK	01	Data In	Configuration Clock Input. An internal programmable control bit selects between the internal oscillator and the CLK input pin as the clock source to control the configuration sequence. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected, $\overline{CE}$ is Low, OE/$\overline{RESET}$ is High, BUSY is Low (parallel mode only), and $\overline{CF}$ is High.	12
OE/$\overline{RESET}$	04	Data In	Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable.	11
	03	Data Out		
	02	Output Enable		
$\overline{CE}$	00	Data In	Chip Enable Input. When $\overline{CE}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high-impedance state.	13
$\overline{CF}$	11	Data In	Configuration Pulse (Open-Drain I/O). As an output, this pin allows the JTAG CONFIG instruction to initiate FPGA configuration without powering down the FPGA. This is an open-drain signal that is pulsed Low by the JTAG CONFIG command. As an input, on the rising edge of $\overline{CF}$, the current design revision selection is sampled and the internal address counter is reset to the start address for the selected revision. If unused, the $\overline{CF}$ pin must be pulled High using an external 4.7 KΩ pull-up to V_{CCO}.	6
	10	Data Out		
	09	Output Enable		

Table 16: **XQF32P Pin Names and Descriptions (VOG48) *(Cont'd)***

Pin Name	Boundary Scan Order	Boundary Scan Function	Pin Description	48-pin TSOP VOG48
$\overline{CEO}$	06	Data Out	Chip Enable Output. Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. $\overline{CEO}$ returns to High when OE/$\overline{RESET}$ goes Low or $\overline{CE}$ goes High.	10
	05	Output Enable		
$\overline{EN\_EXT\_SEL}$	31	Data In	Enable External Selection Input. When this pin is Low, design revision selection is controlled by the Revision Select pins. When this pin is High, design revision selection is controlled by the internal programmable Revision Select control bits. $\overline{EN\_EXT\_SEL}$ has an internal 50KΩ resistive pull-up to V_{CCO} to provide a logic 1 to the device if the pin is not driven.	25
REV_SEL0	30	Data In	Revision Select[1:0] Inputs. When the $\overline{EN\_EXT\_SEL}$ is Low, the Revision Select pins are used to select the design revision to be enabled, overriding the internal programmable Revision Select control bits. The Revision Select[1:0] inputs have an internal 50 KΩ resistive pull-up to V_{CCO} to provide a logic 1 to the device if the pins are not driven.	26
REV_SEL1	29	Data In		27
BUSY	12	Data In	Busy Input. The BUSY input is enabled when parallel mode is selected for configuration. When BUSY is High, the internal address counter stops incrementing and the current data remains on the data pins. On the first rising edge of CLK after BUSY transitions from High to Low, the data for the next address is driven on the data pins. When serial mode or decompression is enabled during device programming, the BUSY input is disabled. BUSY has an internal 50 KΩ resistive pull-down to GND to provide a logic 0 to the device if the pin is not driven.	5
CLKOUT	08	Data Out	Configuration Clock Output. An internal Programmable control bit enables the CLKOUT signal, which is sourced from either the internal oscillator or the CLK input pin. Each rising edge of the selected clock source increments the internal address counter if data is available, $\overline{CE}$ is Low, and OE/$\overline{RESET}$ is High. Output data is available on the rising edge of CLKOUT. CLKOUT is disabled if $\overline{CE}$ is High or OE/$\overline{RESET}$ is Low. If decompression is enabled, CLKOUT is parked High when decompressed data is not ready. When CLKOUT is disabled, the CLKOUT pin is put into a high-Z state. If CLKOUT is used, then it must be pulled High externally using a 4.7 KΩ pull-up to V_{CCO}.	9
	07	Output Enable		
TMS		Mode Select	JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50 KΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the device if the pin is not driven.	21
TCK		Clock	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	20
TDI		Data In	JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50 KΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the device if the pin is not driven.	19
TDO		Data Out	JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50KΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the system if the pin is not driven.	22
VCCINT			+1.8V Supply. Positive 1.8V supply voltage for internal logic.	4, 15, 34
VCCO			+3.3V, 2.5V, or 1.8V I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the output voltage drivers and input buffers.	8, 30, 38, 45
VCCJ			+3.3V or 2.5V JTAG I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the TDO output voltage driver and TCK, TMS, and TDI input buffers.	24

Table 16: **XQF32P Pin Names and Descriptions (VOG48) *(Cont'd)***

Pin Name	Boundary Scan Order	Boundary Scan Function	Pin Description	48-pin TSOP VOG48
GND			Ground	2, 7, 17, 23, 31, 36, 46
DNC			Do Not Connect. (These pins must be left unconnected.)	1, 3, 14, 16, 18, 35, 37, 39, 40, 41, 42

XQF32P VOG48 Pinout Diagram

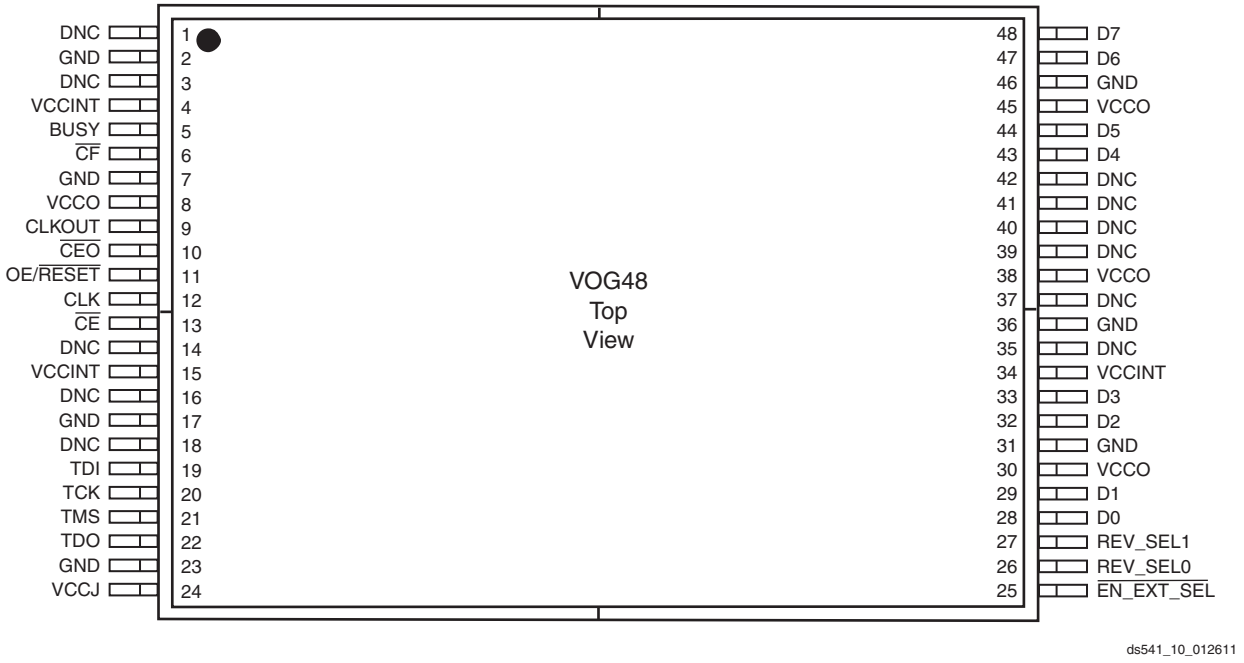


Figure 10: **VOG48 Pinout Diagram (Top View) with Pin Names**

Ordering Information

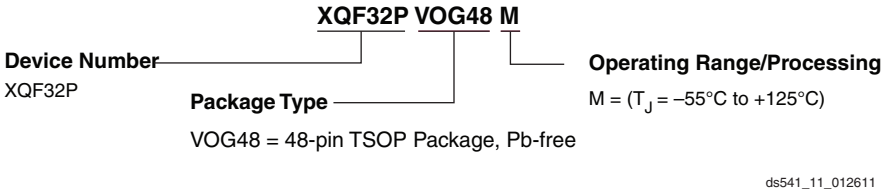


Figure 11: **Ordering information**

Valid Ordering Combinations

XQF32PVOG48M

Marking Information

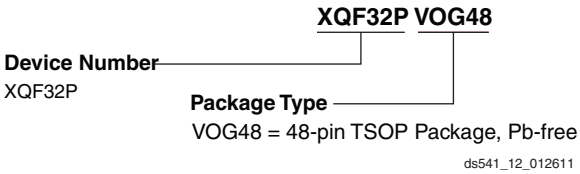


Figure 12: **Marking Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/27/2006	1.0	Xilinx Initial Release.
02/11/2011	2.0	Removed Table 2 from document as Platform Flash PROMs are compatible with all of the existing FPGA device families. Removed 1.5V V_{CCO} option from features list/table and from all specification tables. Replaced verbiage in section External Programming, page 3. Deleted former Figure 5 through Figure 12 (configuration mode schematics) and all associated text in former section *PROM to FPGA Configuration Mode and Connection Summary.* Clarified Table 8. Added row for T_A in specification table Recommended Operating Conditions, page 13. Removed the T_{OECF} and T_{CECF} specifications from Table 13 and Table 14 as well as and Figure 7 and Figure 8. Removed VO48 package per XCN09030: *Product Discontinuation Notice: VO48 Pin Package in Platform Flash PROM Devices.* Added VOG48 (Pb-free) package option as required throughout data sheet.
06/25/2014	2.1	Updated Valid Ordering Combinations. Updated Notice of Disclaimer.
08/05/2015	3.0	This product is obsolete/discontinued per XCN15008.

Notice of Disclaimer