

# BLP10H605

Broadband LDMOS driver transistor

Rev. 2 — 18 April 2014

Objective data sheet

## 1. Product profile

### 1.1 General description

A 5 W plastic LDMOS power transistor for broadcast transmitter and ISM applications at frequencies from HF to 1400 MHz.

Table 1. Application performance

Test signal	f	V <sub>DS</sub>	P <sub>L</sub>	G <sub>p</sub>	η <sub>D</sub>
	(MHz)	(V)	(W)	(dB)	(%)
CW	860	50	5	22.4	59.6

### 1.2 Features and benefits

- Easy power control
- Integrated dual side ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 1400 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

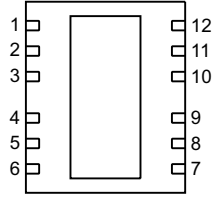
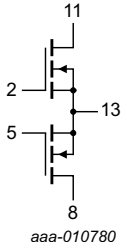
### 1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications



## 2. Pinning information

**Table 2. Pinning**

Pin	Description	Simplified outline	Graphic symbol
1, 3, 4, 6, 7, 9, 10, 12	n.c.	 <p>Transparent top view</p>	 <p>aaa-010780</p>
2	gate1		
5	gate2		
8	drain2		
11	drain1		
13	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BLP10H605	HVSON12	plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 5 × 6 × 0.85 mm	SOT1352-1

## 4. Limiting values

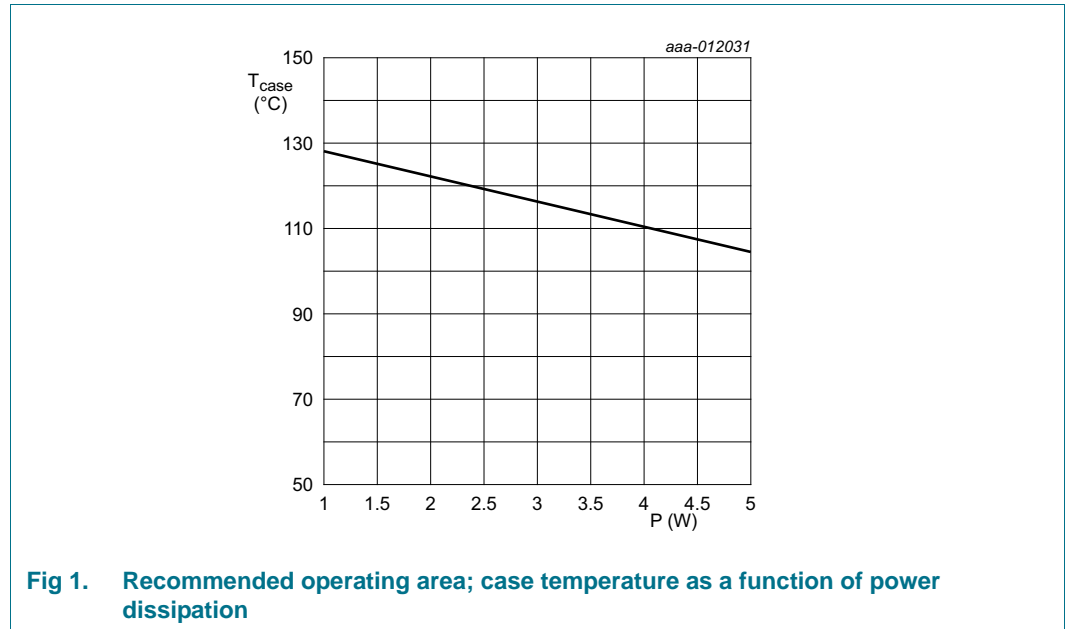
**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	104	V
$V_{GS}$	gate-source voltage		-6	+11	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	150	°C

## 5. Recommended operating conditions

See application note AN11520 for more details.



## 6. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
R <sub>th(j-c)</sub>	thermal resistance from junction to case	T <sub>case</sub> = 80 °C; P <sub>L</sub> = 5 W [1]	5.5	K/W

[1] R<sub>th(j-c)</sub> is measured under RF conditions

## 7. Characteristics

**Table 6. DC characteristics**

T<sub>j</sub> = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 0.03 mA	104	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 3 mA	<tbid>	1.8	<tbid>	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 50 V; I <sub>D</sub> = <tbid> mA	<tbid>	<tbid>	<tbid>	V
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V	-	-	0.6	μA
I <sub>DSX</sub>	drain cut-off current	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; V <sub>DS</sub> = 10 V	-	<tbid>	-	A
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	60	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; I <sub>D</sub> = <tbid> mA	-	<tbid>	-	mΩ

**Table 7. AC characteristics**  
*T<sub>j</sub> = 25 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C <sub>rs</sub>	feedback capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; f = 1 MHz	-	0.07	-	pF
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 0 V; f = 1 MHz	-	6.8	-	pF
C <sub>oss</sub>	output capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; f = 1 MHz	-	2.24	-	pF

**Table 8. RF characteristics**  
*Test signal: CW pulsed; t<sub>p</sub> = 50 μs; δ = 10 %; f = 860 MHz; RF performance at V<sub>DS</sub> = 50 V; I<sub>Dq</sub> = 30 mA; T<sub>case</sub> = 25 °C; unless otherwise specified, in a class-AB production test circuit.*

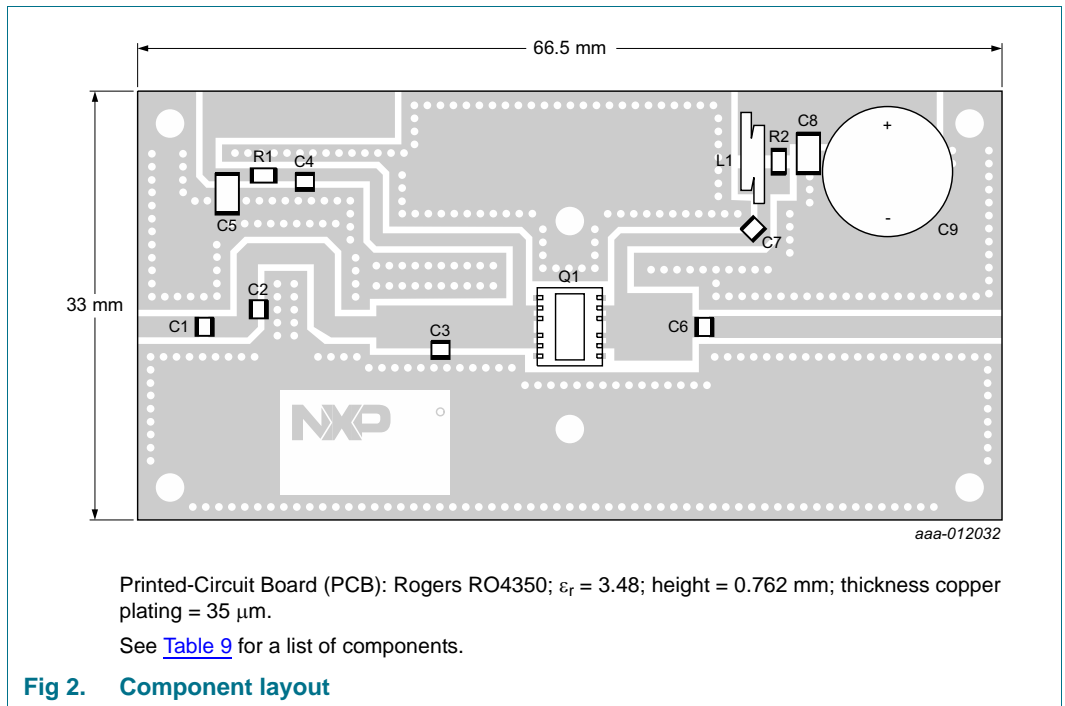
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G <sub>p</sub>	power gain	P <sub>L</sub> = 5 W	<td>	<td>	<td>	dB
η <sub>D</sub>	drain efficiency	P <sub>L</sub> = 5 W	<td>	<td>	-	%

## 8. Test information

### 8.1 Ruggedness in class-AB operation

The BLP10H605 is capable of withstanding a load mismatch corresponding to VSWR = 35 : 1 through all phases under the following conditions: V<sub>DS</sub> = 50 V; I<sub>Dq</sub> = 30 mA; P<sub>L</sub> = 5 W; f = 860 MHz.

### 8.2 Test circuit

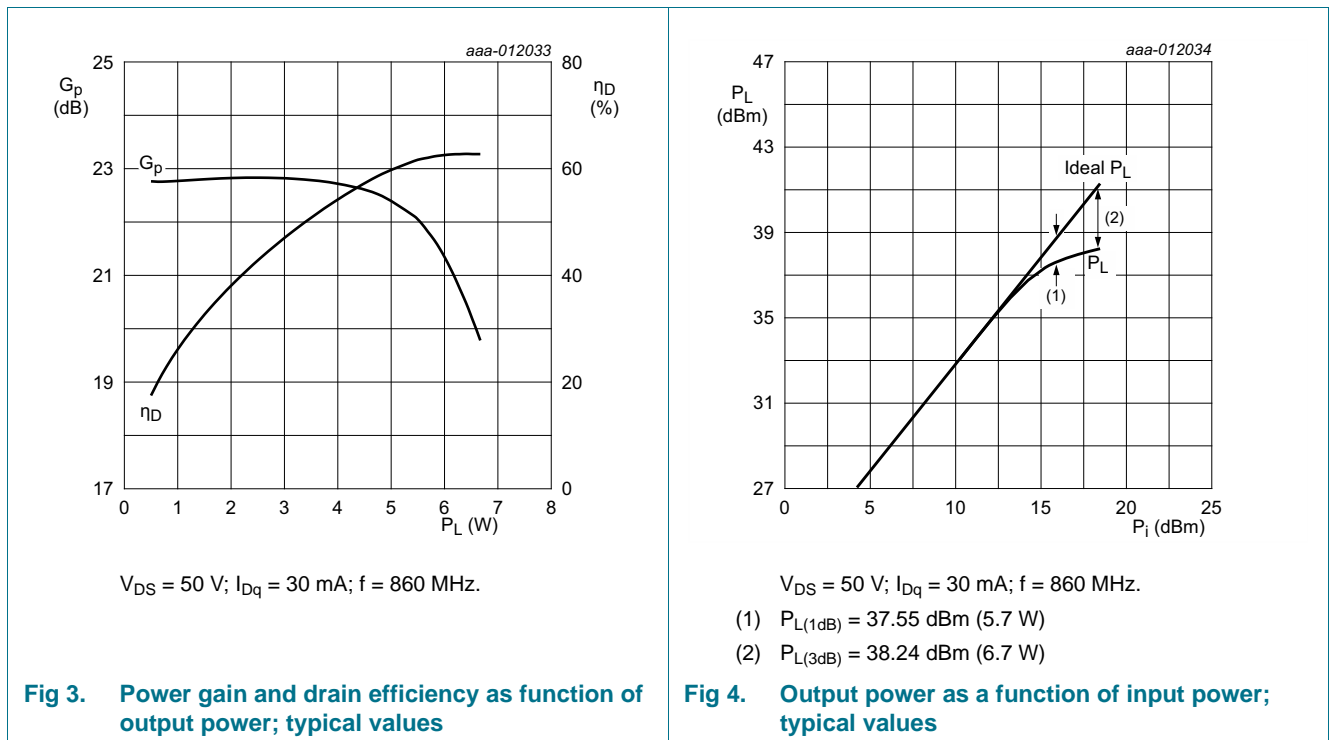


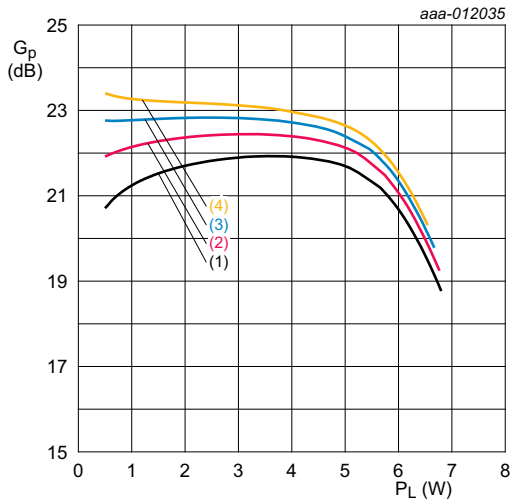
**Table 9. List of components**  
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C4, C7	multilayer ceramic chip capacitor	100 pF	[1]
C2	multilayer ceramic chip capacitor	8.2 pF	[1]
C3	multilayer ceramic chip capacitor	5.1 pF	[1]
C5	multilayer ceramic chip capacitor	1 $\mu$ F, 25 V	Murata GRM31MR71E105KA01L
C6	multilayer ceramic chip capacitor	2.2 pF	[1]
C8	multilayer ceramic chip capacitor	1 $\mu$ F, 50 V	Murata GRM32RR71H105KA01L
C9	electrolytic capacitor	220 $\mu$ F, 63 V	
L1	wire inductor, 0.8 mm copper wire	2 turn, D = 3 mm	
R1	resistor	0 $\Omega$	SMD 0805
R2	resistor	10 $\Omega$	SMD 0805
Q1	transistor	-	BLP10H605

[1] American Technical Ceramics type 100A or capacitor of same quality.

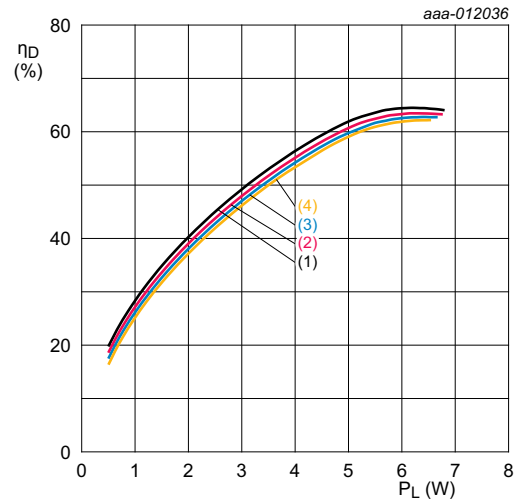
### 8.3 Graphical data





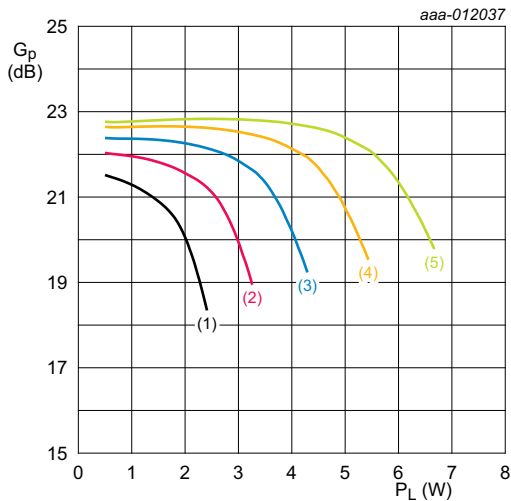
- $V_{DS} = 50\text{ V}; f = 860\text{ MHz}.$
- (1)  $I_{Dq} = 10\text{ mA}$
  - (2)  $I_{Dq} = 20\text{ mA}$
  - (3)  $I_{Dq} = 30\text{ mA}$
  - (4)  $I_{Dq} = 40\text{ mA}$

Fig 5. Power gain as a function of output power; typical values



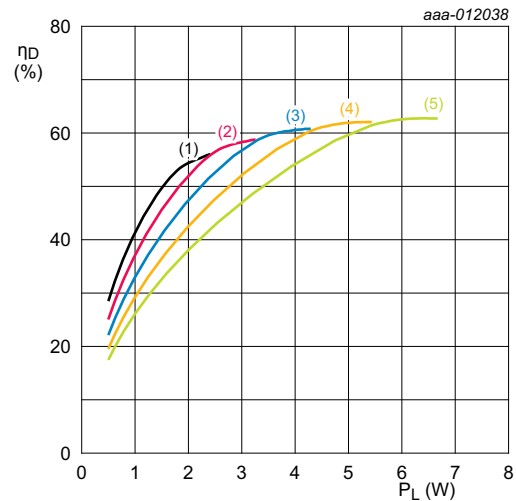
- $V_{DS} = 50\text{ V}; f = 860\text{ MHz}.$
- (1)  $I_{Dq} = 10\text{ mA}$
  - (2)  $I_{Dq} = 20\text{ mA}$
  - (3)  $I_{Dq} = 30\text{ mA}$
  - (4)  $I_{Dq} = 40\text{ mA}$

Fig 6. Drain efficiency as a function of output power; typical values



- $I_{Dq} = 30\text{ mA}; f = 860\text{ MHz}.$
- (1)  $V_{DS} = 30\text{ V}$
  - (2)  $V_{DS} = 35\text{ V}$
  - (3)  $V_{DS} = 40\text{ V}$
  - (4)  $V_{DS} = 45\text{ V}$
  - (5)  $V_{DS} = 50\text{ V}$

Fig 7. Power gain as a function of output power; typical values



- $I_{Dq} = 30\text{ mA}; f = 860\text{ MHz}.$
- (1)  $V_{DS} = 30\text{ V}$
  - (2)  $V_{DS} = 35\text{ V}$
  - (3)  $V_{DS} = 40\text{ V}$
  - (4)  $V_{DS} = 45\text{ V}$
  - (5)  $V_{DS} = 50\text{ V}$

Fig 8. Drain efficiency as a function of output power; typical values

9. Package outline

HVSON12: plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 5 x 6 x 0.85 mm

SOT1352-1

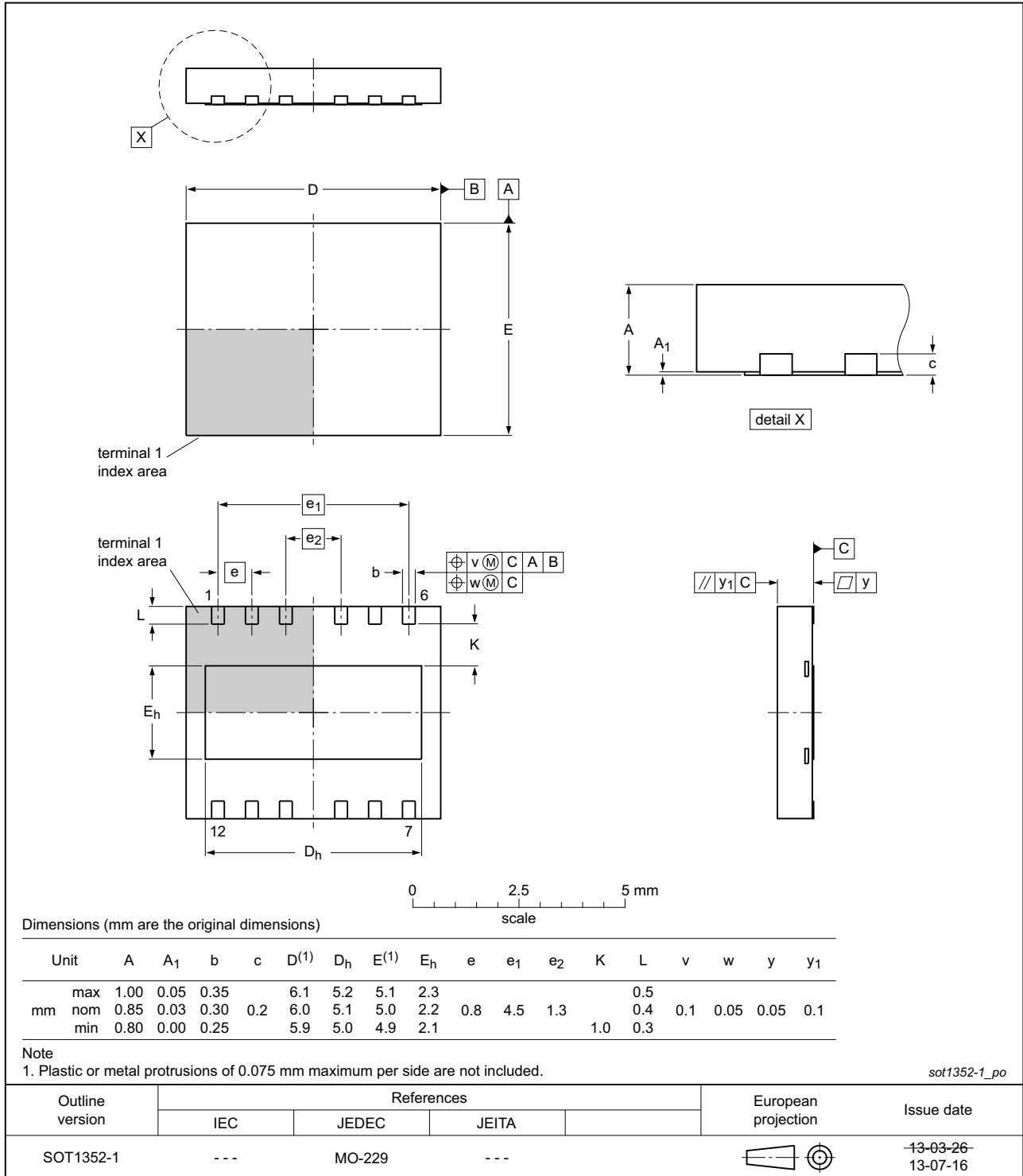


Fig 9. Package outline SOT1352-1 (HVSON12)

## 10. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 11. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
HF	High Frequency
ISM	Industrial, Scientific and Medical
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP10H605 v.2	20140418	Objective data sheet	-	BLP10H605 v.1
Modifications	<ul style="list-style-type: none"> <li><a href="#">Section 5 on page 3</a>: section added</li> <li><a href="#">Table 5 on page 3</a>: value <math>R_{th(j-c)}</math> added</li> <li><a href="#">Table 7 on page 4</a>: table updated</li> <li><a href="#">Section 8.2 on page 4</a>: section added</li> <li><a href="#">Section 8.3 on page 5</a>: section added</li> </ul>			
BLP10H605 v.1	20140221	Objective data sheet	-	-



## 13. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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