CA3127

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- *Gain-bandwidth product (f_T) > 1 GHz*
- *Power gain = 30 dB (typ.) at 100 MHz*
- *Noise figure = 3.5 dB (typ.) at 100 MHz*
- *Five independent transistors on a common substrate*

RCA-CA3127* consits of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127 useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

The CA3127 is supplied in the 16-lead dual-in-line plastic package (E suffix), 16-lead dual-in-line frit-seal ceramic package (F suffix), and is also available in clip form (H suffix). It operates over the full military temperature range of -55 to +125° C.

*Formerly RCA Dev. No. TA6206.

Applications:

- *VHF amplifiers*
- *Multifunction combinations - RF/mixer/oscillator*
- *Sense amplifiers*
- *Synchronous detectors*
- *VHF mixers*
- *IF converter*
- *IF amplifiers*
- *Synthesizers*
- *Cascade amplifiers*

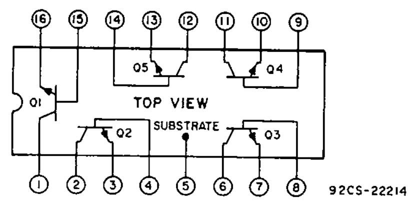

Fig. 1 — Schematic diagram of CA3127.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

POWER DISSIPATION, P_D:	
Any one transistor	85 mW
Total Package:	
For T_A up to 75° C	425 mW
For T_A > 75° C Derate Linearly at	6.67 mW/° C
AMBIENT TEMPERATURE RANGE:	
Operating	-55 to +125° C
Storage	-65 to +125° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265° C
The following ratings apply for each transistor in the device:	
Collector-to-Emitter Voltage, V_{CEO}	15 V
Collector-to-Base Voltage, V_{CBO}	20 V
Collector-to-Substrate Voltage, V_{CIO}*	20 V
Collector Current, I_C	20 mA

*The collector of each transistor of the CA3127 is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

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STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	TEST CONDITIONS		LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0$		20	32	–	V
Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$		15	24	–	V
Collector-to-Substrate Breakdown Voltage	$I_{C1} = 10\ \mu A$, $I_B = 0$, $I_E = 0$		20	60	–	V
Emitter-to-Base Breakdown Voltage*	$I_E = 10\ \mu A$, $I_C = 0$		4	5.7	–	V
Collector-Cutoff-Current	$V_{CE} = 10$ V, $I_B = 0$		–	–	0.5	μA
Collector-Cutoff-Current	$V_{CB} = 10$ V, $I_E = 0$		–	–	40	nA
DC Forward-Current Transfer Ratio	$V_{CE} = 6$ V	$I_C = 5$ mA	35	88	–	
		$I_C = 1$ mA	40	90	–	
		$I_C = 0.1$ mA	35	85	–	
Base-to-Emitter Voltage	$V_{CE} = 6$ V	$I_C = 5$ mA	0.71	0.81	0.91	V
		$I_C = 1$ mA	0.66	0.76	0.86	
		$I_C = 0.1$ mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		–	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched		–	0.5	5	mV
Magnitude of Difference in I_B	$V_{CE} = 6$ V, $I_C = 1$ mA		–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

DYNAMIC CHARACTERISTICS at $T_A = 25^\circ C$

CHARACTERISTICS	TEST CONDITIONS	LIMITS Min.	Typ.	Max.	UNITS
I/F Noise Figure	f = 100 kHz, $R_S = 500\ \Omega$, $I_C = 1$ mA	–	1.8	–	dB
Gain-Bandwidth Product	$V_{CE} = 6$ V, $I_C = 5$ mA	–	1.15	–	GHz
Collector-to-Base Capacitance	$V_{CB} = 6$ V, f = 1 MHz	–	See Fig. 5	–	pF
Collector-to-Substrate Capacitance	$V_{CI} = 6$ V, f = 1 MHz	–	See Fig. 5	–	pF
Emitter-to-Base Capacitance	$V_{BE} = 4$ V, f = 1 MHz	–	See Fig. 5	–	pF
Voltage Gain	$V_{CE} = 6$ V, f = 10 MHz $R_L = 1\ k\Omega$, $I_C = 1$ mA	–	28	–	dB
Power Gain	Cascode Configuration f = 100 MHz, $V^+ = 12$ V $I_C = 1$ mA	27	30	–	dB
Noise Figure		–	3.5	–	dB
Input Resistance	Common-Emitter Configuration $V_{CE} = 6$ V $I_C = 1$ mA f = 200 MHz	–	400	–	Ω
Output Resistance		–	4.6	–	kΩ
Input Capacitance		–	3.7	–	pF
Output Capacitance		–	2	–	pF
Magnitude of Forward Transadmittance		–	24	–	mmho

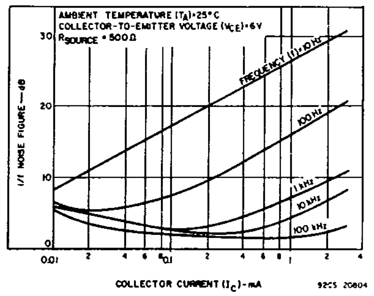

Fig. 2 — 1/f noise figure as a function of collector current at R_{SOURCE} = 500 Ω.

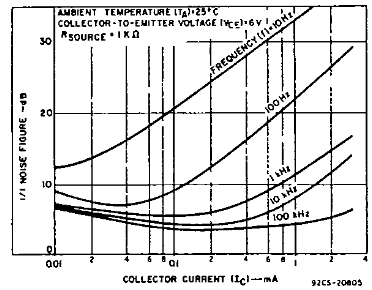

Fig. 3 — 1/f noise figure as a function of collector current at R_{SOURCE} = 1 kΩ.

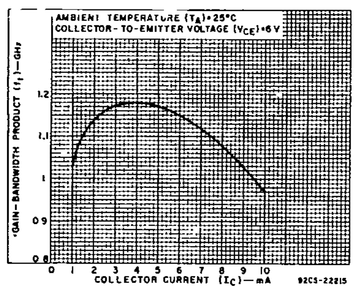

Fig. 4 — Gain-bandwidth product as a function of collector current.

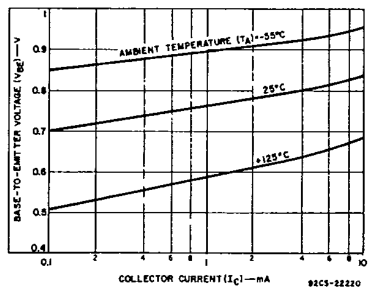

Fig. 5 — Base-to-emitter voltage as a function of collector current.

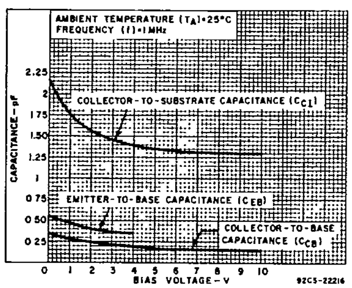

Fig. 6(a) — Capacitance as a function of bias voltage for Q_2.

Transistor	Capacitance (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	Pkg	Total	Pkg	Total	Pkg	Total	Pkg	Total
Bias Voltage	–	6 V	–	6 V	–	4 V	–	6 V
Q1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q2	0.015	0.170	0.225	0.265	0.130	0.360	0.085	1.35
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

Fig. 6(b) — Typical capacitance values at f = 1 MHz. Three terminal measurement. Guard all terminals except those under test.

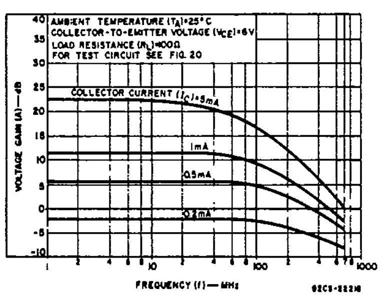

Fig. 7 — Voltage gain as a function of frequency at R_L = 100 Ω.

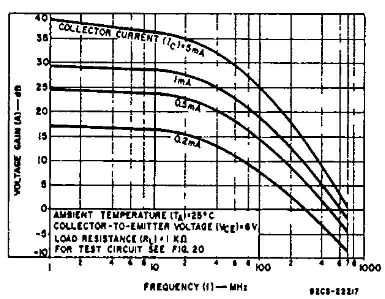

Fig. 8 — Voltage gain as a function of frequency at R_L = 1 kΩ.

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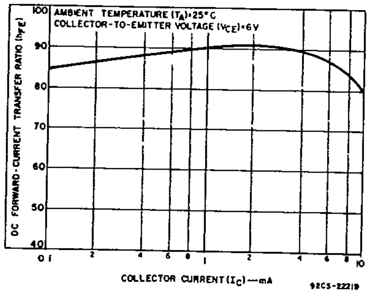


Fig. 9 – DC forward-current transfer ratio as a function of collector current.

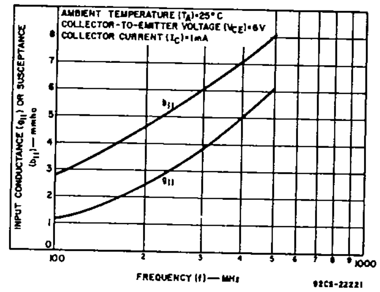


Fig. 10 – Input admittance (Y_{11}) as a function of frequency.

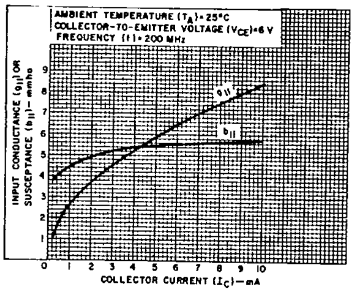


Fig. 11 – Input admittance (Y_{11}) as a function of collector current.

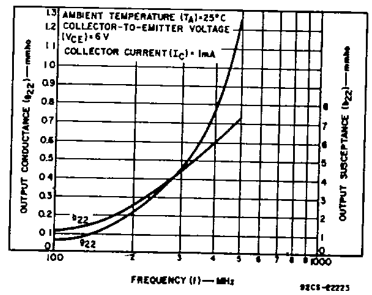


Fig. 12 – Output admittance (Y_{22}) as a function of frequency.

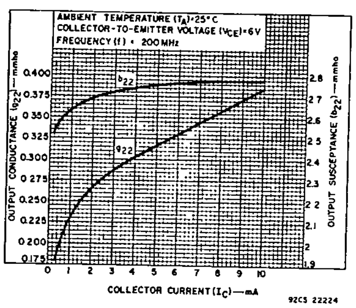


Fig. 13 – Output admittance (Y_{22}) as a function of collector current.

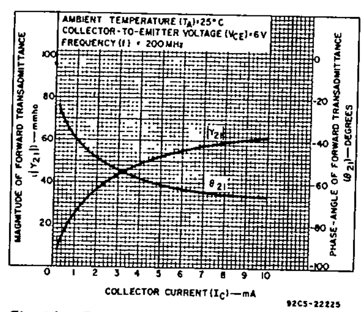


Fig. 14 – Forward transadmittance (Y_{21}) as a function of collector current.

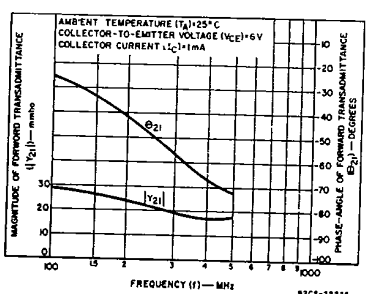


Fig. 15 – Forward transadmittance (Y_{21}) as a function of frequency.

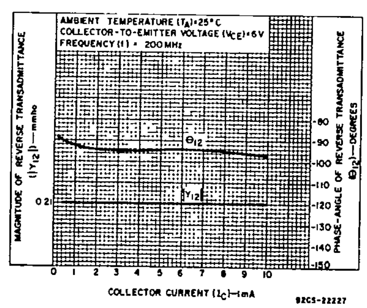


Fig. 16 – Reverse transadmittance (Y_{12}) as a function of collector current.

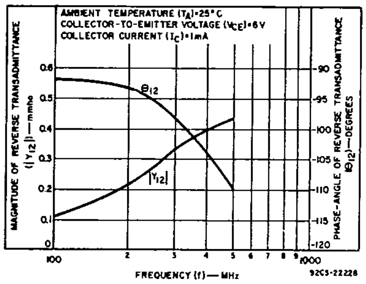


Fig. 17 – Reverse transadmittance (Y_{12}) as a function of frequency.

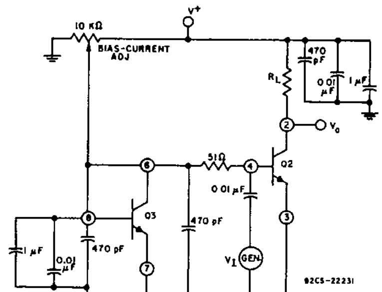
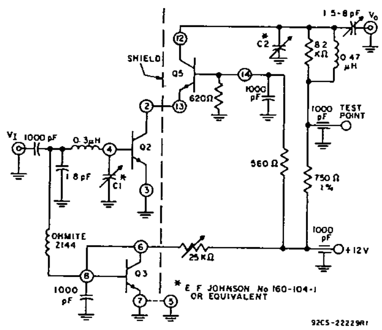


Fig. 18 – Voltage-gain test circuit using current-mirror biasing for Q_2.



This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

Fig. 19 – 100-MHz power-gain and noise-figure test circuit.

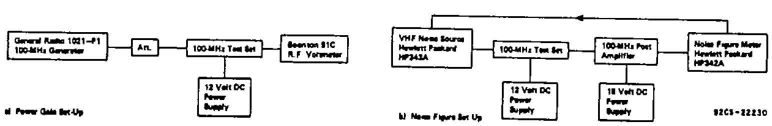


Fig. 20 – Block diagrams of power-gain and noise-figure test set-ups.