DM9102DEP Product Brief

Single Chip Fast Ethernet NIC Controller

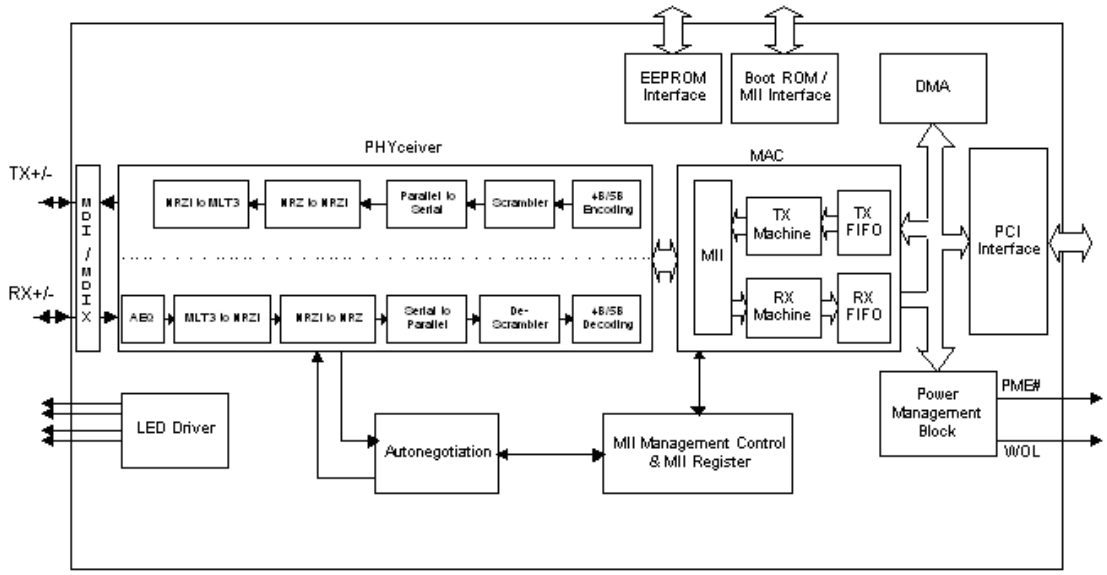
May. 2008 Rev.1.0

The DM9102D is a fully integrated and cost effective single chip Fast Ethernet NIC controller. It is designed with low power and high performance process. It is a 2.5/3.3V device with 5V tolerance.

The DM9102D provides direct interface to the PCI bus and supports bus master mode to achieve the high performance of the PCI bus. It fully complies with PCI 2.2. In the media side, the DM9102D interfaces to the UTP3, 4, 5 in 10Base-T and the UTP5 in 100Base-TX. It is fully compliant with the IEEE 802.3u Spec. The auto-negotiation and HP Auto-MDIX function can automatically configure the DM9102D to take the maximum advantage of its abilities. The DM9102D also supports IEEE 802.3x's full-duplex flow control to prevent the receive overflow of link partner. The IPv4 IP/TCP/UDP checksum generation and checking can reduce the system CPU utilization.

The DM9102D supports two types of power management mechanisms. The main mechanism is based on the OnNow architecture, which is required for PC99. The alternative mechanism is based upon the remote Wake-On-LAN mechanism.

Block Diagram



Specifications

- Integrated Fast Ethernet MAC, Physical Layer and transceiver in one chip.
- 128 pin LQFP with CMOS process.
- +2.5/3.3V Power supply with +5V tolerant I/O.
- Comply with PCI specification 2.2.
- PCI bus master architecture.
- PCI bus burst mode data transfer.
- Two large independent transmission and receipt FIFO.
- Up to 256K bytes Boot EPROM or Flash interface.
- EEPROM 93C46 interface automatically supports node ID load and configuration information.
- Comply with IEEE 802.3u 100Base-TX and 802.3 10Base-T.
- Comply with IEEE 802.3u auto-negotiation protocol for automatic link type selection.
- Support IEEE 802.3x Full Duplex Flow Control.
- VLAN frame length support.
- IP/TCP/UDP checksum generation and checking.
- Zero copy supporting.
- Comply with ACPI and PCI Bus Power Management.
- Support the MII (Media Independent Interface) for an external PHY.
- Support Wake-On-LAN function and remote wake-up (Magic packet, Link Change and Microsoft® wake-up frame).
- Support 4 Wake-On-LAN (WOL) signals (active high pulse, active low pulse, active high, active low.)
- High performance 100Mbps clock generator and data recovery circuit.
- Digital clock recovery circuit, using advanced digital algorithm to reduce jitter.
- Adaptive equalization circuit and Baseline wandering restoration circuit for 100Mbps receiver.
- Provides Loopback mode for easy system diagnostics.
- Support HP Auto-MDIX.
- Low power consumption modes:
  - Power reduced mode (cable detection)
  - Power down mode
  - Selectable TX drivers for 1:1 or 1.25:1 transformers for additional power reduction. (1.25:1 transformers for Non Auto-MDIX only).

Application

VoIP CPE (ATA, IP Phone, Video Phone)
IP STB, IPTV, IPC, Internet Radio
IP CAM, POS, DVR, Telecom

Ordering Information

Part Number	Pin Count	Package
DM9102DE	128	LQFP
DM9102DEP	128	LQFP(Pb-Free)

DAVICOM Semiconductor, Inc.
No.6, Li-Hsin Rd.VI, Science Park, Hsin-Chu, Taiwan, R.O.C.
TEL: 886-3-5798797
FAX: 886-3-5646929
E-mail: sales@davicom.com.tw