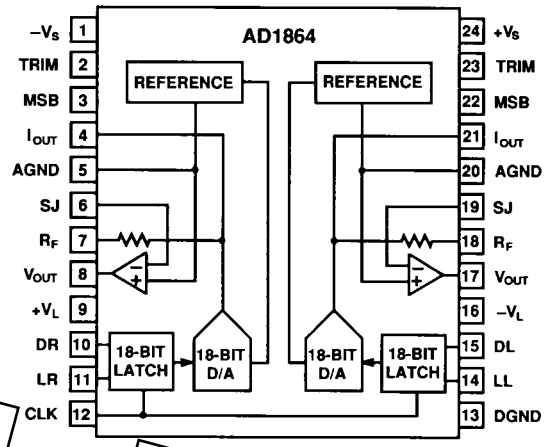
Complete Dual 18-Bit Audio DAC

AD1864*

FEATURES
Dual Serial Input, Voltage Output DACs
No External Components Required
Operates at 8 × Oversampling per Channel
±5 Volt to ±12 Volt Operation
Cophased Outputs
115 dB Channel Separation
±0.3% Interchannel Gain Matching
0.0017% THD+N

APPLICATIONS
Multichannel Audio Applications:
Compact Disc Players
Multi-Voice Keyboard Instruments
DAT Players and Recorders
Digital Mixing Consoles
Multimedia Workstations

DIP BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD1864 is a complete dual 18-bit DAC offering excellent THD+N, while requiring no external components. Two complete signal channels are included. This results in cophased voltage or current output signals and eliminates the need for output demultiplexing circuitry. The monolithic AD1864 chip includes CMOS logic elements, bipolar and MOS linear elements and laser-trimmed thin-film resistor elements, all fabricated on Analog Devices BiMOS II process.

The DACs on the AD1864 chip employ a partially-segmented architecture. The first four MSBs of each DAC are segmented into 15 elements. The 14 LSBs are produced using standard R-2R techniques. Segment and R-2R resistors are laser-trimmed to provide extremely low total harmonic distortion. This architecture minimizes errors at major code transitions resulting in low output glitch and eliminating the need for an external deglitcher. When used in the current output mode, the AD1864 provides two cophased ±1 mA output signals.

Each channel is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±3 V signals at load currents up to 8 mA. Each output amplifier is short-circuit protected and can withstand indefinite short circuits to ground.

The AD1864 was designed to balance two sets of opposing requirements, channel separation and DAC matching. High channel separation is the result of careful layout techniques. At the same time, both channels of the AD1864 have been designed to ensure matched gain and linearity as well as tracking over time and temperature. This assures optimum performance when used in stereo and multi-DAC per channel applications.

*Covered by U.S. Patents No: 4,855,618

A versatile digital interface allows the AD1864 to be directly connected to standard digital filter chips. This interface employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial input pins for the left and right DAC input registers. Input data bits are clocked into the input register on the rising edge of CLK. A low-going latch edge updates the respective DAC output. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together.

The AD1864 operates from ±5 V to ±12 V power supplies. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. The AD1864 typically dissipates only 225 mW, with a maximum power dissipation of 265 mW.

The AD1864 is packaged in both a 24-pin plastic DIP and a 28-pin PLCC. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 V to ±13.2 V.

PRODUCT HIGHLIGHTS

1. The AD1864 is a complete dual 18-bit audio DAC.
2. 108 dB signal-to-noise ratio for low noise operation.
3. THD+N is typically 0.0017%.
4. Interchannel gain and midscale matching.
5. Output voltages and currents are cophased.
6. Low glitch for improved sound quality.
7. Both channels are 100% tested at 8 × F_S.
8. Low Power — only 225 mW typ, 265 mW max.
9. 5-wire interface for individual DAC control.

REV. A

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AD1864—SPECIFICATIONS (T_A = +25°C, $\pm V_L = \pm V_S = \pm 5$ V, F_S = 352.8 kHz, without MSB adjustment)

	Min	Typ	Max	Units
RESOLUTION		18		Bits
DIGITAL INPUTS				
V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH} = +V_L$			**1.0**	μA
I_{IL}, V_{IL} = 0.4 V			**−10**	μA
Clock Input Frequency	**12.7**			MHz
ACCURACY				
Gain Error		0.4	**1.0**	% of FSR
Interchannel Gain Matching		0.3	**0.8**	% of FSR
Midscale Error		4		mV
Interchannel Midscale Matching		5		mV
Gain Linearity Error (0 dB to −90 dB)		<2		dB
DRIFT (0°C to +70°C)				
Gain Drift		±25		ppm of FSR/°C
Midscale Drift		±4		ppm of FSR/°C
TOTAL HARMONIC DISTORTION + NOISE*				
0 dB, 990.5 Hz AD1864N, P		0.004	**0.006**	%
AD1864N-J, P-J		0.003	**0.004**	%
AD1864N-K		0.0017	**0.0025**	%
−20 dB, 990.5 Hz AD1864N, P		0.010	**0.040**	%
AD1864N-J, P-J		0.010	**0.020**	%
AD1864N-K		0.010	**0.020**	%
−60 dB, 990.5 Hz AD1864N, P		1.0	**4.0**	%
AD1864N-J, P-J		1.0	**2.0**	%
AD1864N-K		1.0	**2.0**	%
CHANNEL SEPARATION*				
0 dB, 990.5 Hz	**110**	115		dB
SIGNAL-TO-NOISE RATIO*				
(20 Hz to 30 kHz) N, N-J, N-K	**102**	108		dB
P, P-J	**95**	108		
D-RANGE* (WITH A-WEIGHT FILTER)				
−60 dB, 990.5 Hz AD1864N, P	**88**	100		dB
AD1864N-J, P-J	**94**	100		dB
AD1864N-K	**94**	100		dB
OUTPUT				
Voltage Output Configuration				
Output Range (±3%)	**±2.88**	±3.0	**±3.12**	V
Output Impedance		0.1		Ω
Load Current	±8			mA
Short-Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Output Range (±30%)		±1		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
$+V_L$ and $+V_S$	4.75	**5.0**	13.2	V
$-V_L$ and $-V_S$	−13.2	**−5.0**	−4.75	V
+I, ($+V_L$ and $+V_S$ = +5 V)		22	**25**	mA
−I, ($-V_L$ and $-V_S$ = −5 V)		−23	**−28**	mA
POWER DISSIPATION, $\pm V_L = \pm V_S = \pm 5$ V		225	**265**	mW
TEMPERATURE RANGE				
Specification	0	**+25**	+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C
WARMUP TIME	1			min

NOTE
Specifications shown in **boldface** are tested on production units at final test without optional MSB adjustment.
*Tested in accordance with EIAJ Test Standard CP-307 with 18-bit data.
Specifications subject to change without notice.

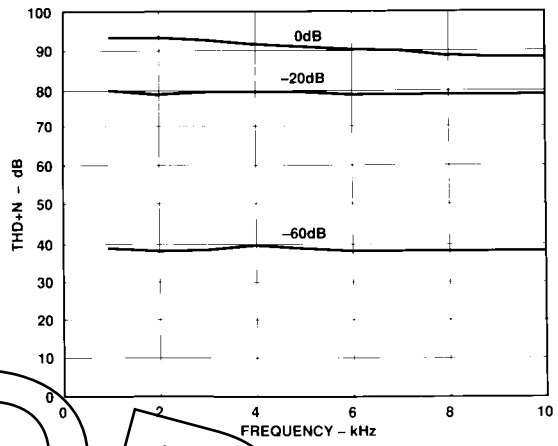


Figure 1. THD+N vs. Frequency

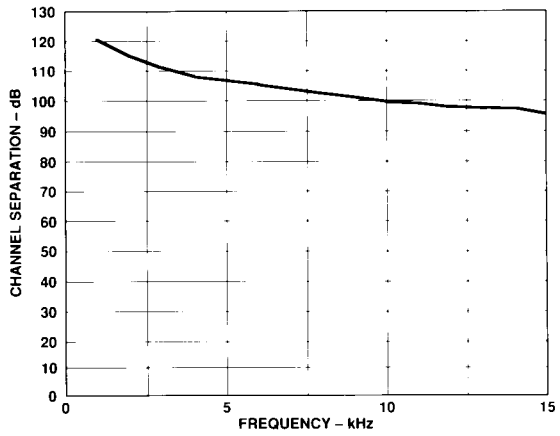


Figure 2. Channel Separation vs. Frequency

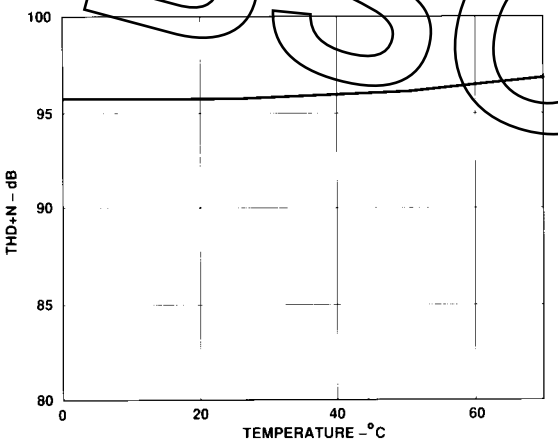


Figure 3. THD+N vs. Temperature

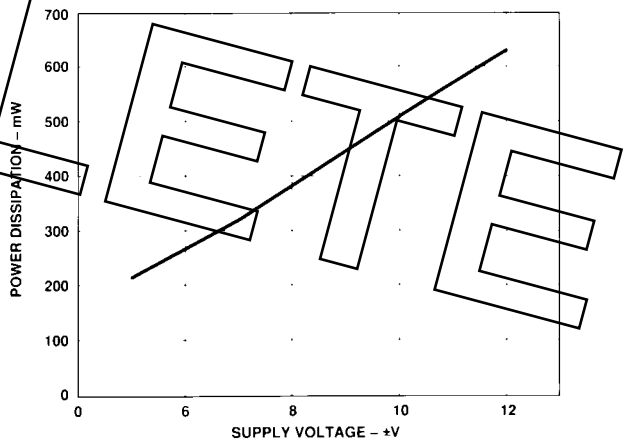


Figure 4. Power Dissipation vs. Supply Voltage

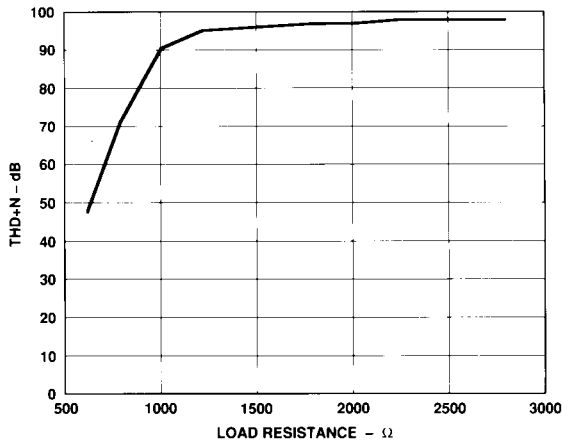


Figure 5. THD+N vs. Load Resistance

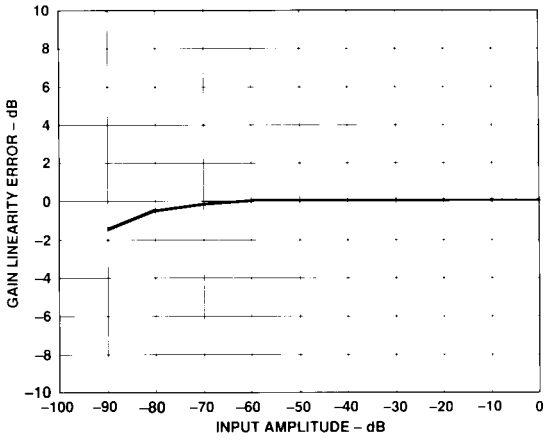


Figure 6. Gain Linearity Error vs. Input Amplitude

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 V to 13.2 V
V_S to AGND . . . . . 0 V to 13.2 V
$-V_L$ to DGND . . . . . −13.2 V to 0 V
$-V_S$ to AGND . . . . . −13.2 V to 0 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_L
Short-Circuit Protection . . . . . Indefinite Short to Ground
Soldering (10 sec) . . . . . +300°C

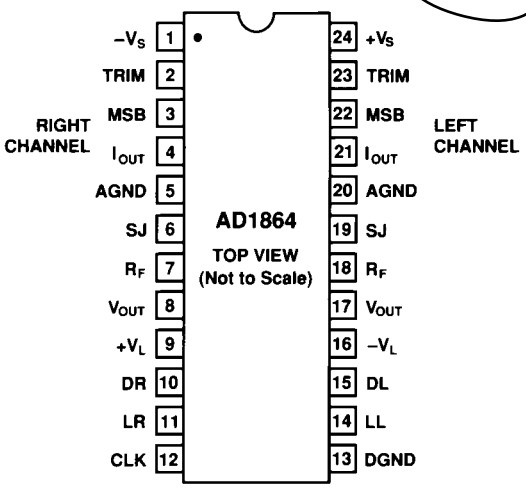
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

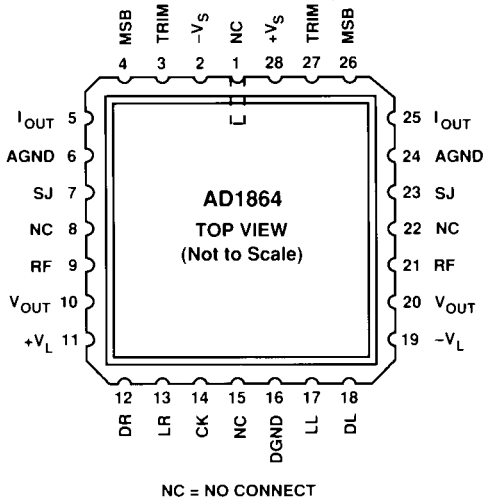
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP Package



PLCC Package



NC = NO CONNECT

PIN DESIGNATIONS

SIGNAL	DESCRIPTION
$-V_S$	Negative Analog Supply
TRIM	Right Channel Trim Network Connection
MSB	Right Channel Trim Potentiometer Connection
I_{OUT}	Right Channel Output Current
AGND	Right Channel Analog Common Pin
SJ	Right Channel Amplifier Summing Junction
R_F	Right Channel Feedback Resistor
V_{OUT}	Right Channel Output Voltage
$+V_L$	Positive Digital Supply
DR	Right Channel Data Input Pin
LR	Right Channel Latch Pin
CLK	Clock Input Pin
DGND	Digital Common Pin
LL	Left Channel Latch Pin
DL	Left Channel Data Input Pin
$-V_L$	Negative Digital Supply
V_{OUT}	Left Channel Output Voltage
RF	Left Channel Feedback Resistor
SJ	Left Channel Amplifier Summing Junction
AGND	Left Channel Analog Common Pin
I_{OUT}	Left Channel Output Current
MSB	Left Channel Trim Potentiometer Wiper Connection
TRIM	Left Channel Trim Network Connection
$+V_S$	Positive Analog Supply

ORDERING GUIDE

Model	THD+N @ FS	Package Option*
AD1864N	0.006%	N-24
AD1864N-J	0.004%	N-24
AD1864N-K	0.0025%	N-24
AD1864P	0.006%	P-28A
AD1864P-J	0.004%	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent.

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large (0 dB) and small (−20 dB, −60 dB) signal amplitudes. THD+N measurements for the AD1864 are made using the first 19 harmonics and noise out to 30 kHz.

SIGNAL-TO-NOISE RATIO

The Signal-to-Noise Ratio is defined as the ratio of the amplitude of the output when a full-scale code is entered to the amplitude of the output when a midscale code is entered. It is measured using a standard A-Weight filter. SNR for the AD1864 is measured for noise components up to 30 kHz.

CHANNEL SEPARATION

Channel separation is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of that same signal which couples onto the adjacent channel. It is usually expressed in dB. For the AD1864 channel separation is measured in accordance with EIAJ Standard CP-307, Section 5.5.

D-RANGE DISTORTION

D-Range distortion is equal to the value of the total harmonic distortion + noise (THD+N) plus 60 dB when a signal level of 60 dB below full-scale is reproduced. D-Range is tested with a 1 kHz input sine wave. This is measured with a standard A-Weight filter as specified by EIAJ Standard CP-307.

GAIN ERROR

The gain error specification indicates how closely the output of a given channel matches the ideal output for given input data. It is expressed in % of FSR and is measured with a full-scale output signal.

INTERCHANNEL GAIN MATCHING

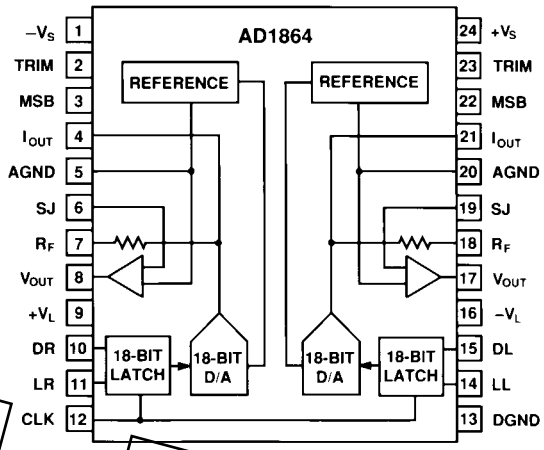
The gain matching specification indicates how closely the amplitudes of the output signals match when producing identical input data. It is expressed in % of FSR (Full-Scale Range = 6 V for the AD1864) and is measured with full-scale output signals.

MIDSCALE ERROR

Midscale error is the deviation of the actual analog output of a given channel from the ideal output (0 V) when the 2s complement input code representing half scale is loaded into the input register of the DAC. It is expressed in mV.

INTERCHANNEL MIDSCALE MATCHING

The midscale matching specification indicates how closely the amplitudes of the output signals of the two channels match when the 2s complement input code representing half scale is loaded into the input register of both channels. It is expressed in mV and is measured with half-scale output signals.



AD1864 DIP Block Diagram

FUNCTIONAL DESCRIPTION

The AD1864 is a complete, monolithic, dual 18-bit audio DAC. No external components are required for operation. As shown in the block diagram, each chip contains two voltage references, two output amplifiers, two 18-bit serial input registers and two 18-bit DACs.

The voltage reference section provides a reference voltage for each DAC circuit. These voltages are produced by low-noise bandgap circuits. Buffer amplifiers are also included. This combination of elements produces reference voltages that are unaffected by changes in temperature and time.

The output amplifiers use both MOS and bipolar devices and incorporate an all NPN output stage. This design technique produces higher slew rate and lower distortion than previous techniques. Frequency response is also improved. When combined with the appropriate on-chip feedback resistor, the output op amps convert the output current to output voltages.

The 18-bit D/A converters use a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser trimming of these resistors further reduces linearity errors resulting in low output distortion.

The input registers are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption, contributing to the low glitch and low power dissipation of the AD1864.

AD1864—Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1864 has three ground pins, two labeled AGND and one labeled DGND. AGND, the analog ground pins, are the "high quality" ground references for the device. To minimize distortion and reduce crosstalk between channels, the analog ground pins should be connected together only at the analog common point in the system. As shown in Figure 7, the AGND pins should *not* be connected at the chip.

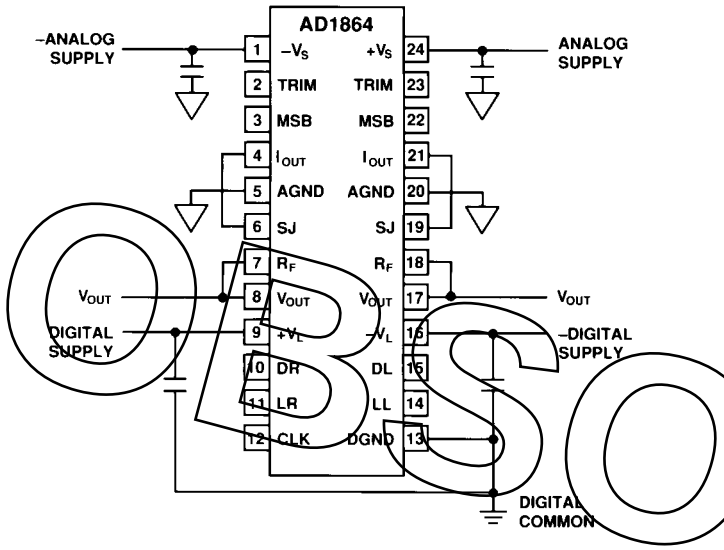


Figure 7. Recommended DIP Circuit Schematic

The digital ground pin returns ground current from the digital logic portions of the AD1864 circuitry. This pin should be connected to the digital common pin in the system. Other digital logic chips should also be referred to that point. The analog and digital grounds should be connected together at one point in the system, preferably at the power supply.

POWER SUPPLIES AND DECOUPLING

The AD1864 has four power supply pins. $\pm V_S$ provide the supply voltages which operate the analog portions of the DAC including the voltage references, output amplifiers and control amplifiers. The $\pm V_S$ supplies are designed to operate from ± 5 V to ± 12 V. These supplies should be decoupled to analog common using 0.1 μF capacitors. Good engineering practice suggests that the bypass capacitors be placed as close as possible to the package pins. This minimizes the parasitic inductive effects of printed circuit board traces.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift registers and the input latching circuitry. These supplies should be bypassed to digital common using 0.1 μF capacitors. $\pm V_L$ operates with ± 5 V to ± 12 V supplies. In order to assure proper operation of the AD1864, $-V_S$ must be the most negative power supply voltage at all times.

Though separate positive and negative power supply pins are provided for the analog and digital portions of the AD1864, it is also possible to use the AD1864 in systems featuring a single positive and a single negative power supply. In this case, the $+V_S$ and $+V_L$ input pins should be connected to the positive power supply. $-V_S$ and $-V_L$ should be connected to the single negative supply. This feature allows reduction of the cost and complexity of the system power supply.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well-regulated power supplies with less than 1% ripple be incorporated into the design of an audio system.

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD+N specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance. Figure 1 illustrates the typical THD+N performance of the AD1864 versus frequency. A load impedance of at least 1.5 kΩ is recommended for best THD+N performance.

Analog Devices tests and grades all AD1864s on the basis of THD+N performance. During the distortion test, a high-speed digital pattern generator transmits digital data to each channel of the device under test. Eighteen-bit data is latched into the DAC at 352.8 kHz (8 × Fs). The test waveform is a 990.5 kHz sine wave with 0 dB, −20 dB and −60 dB amplitudes. A 4096-point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, D-Range and channel separation. No deglitchers or MSB trims are used.

OPTIONAL MSB ADJUSTMENT

Use of optional adjust circuitry allows residual distortion error to be eliminated. This distortion is especially important when low-amplitude signals are being reproduced. The MSB-adjust circuitry is shown in Figure 8. The trim pot should be adjusted to produce the lowest distortion using an input signal with a −60 dB amplitude.

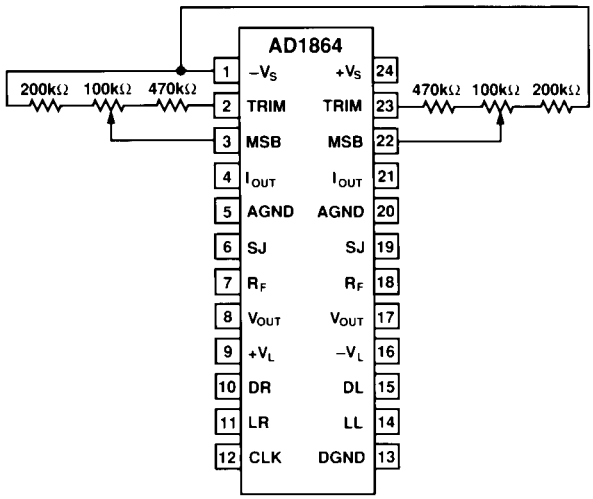


Figure 8. Optional DIP THD+N Adjust Circuitry

CURRENT OUTPUT MODE

One or both channels of the AD1864 can be operated in current output mode. I_{OUT} can be used to directly drive an external current-to-voltage (I-V) converter. The internal feedback resistor, R_F, can still be used in the feedback path of the external I-V converter, thus assuring that R_F tracks the DAC over time and temperature.

Of course, the AD1864 can also be used in voltage output mode utilizing the onboard I-V converter.

VOLTAGE OUTPUT MODES

As shown in the AD1864 block diagram, each channel of the AD1864 is complete with an I-V converter and a feedback resistor. These can be connected externally to provide direct voltage output from one or both AD1864 channels. Figure 7 shows these connections. I_{OUT} is connected to the summing junction, SJ. V_{OUT} is connected to the feedback resistor, R_F. This implementation results in the lowest possible component count and achieves the performance shown on the specifications page while operating at $8 \times F_S$.

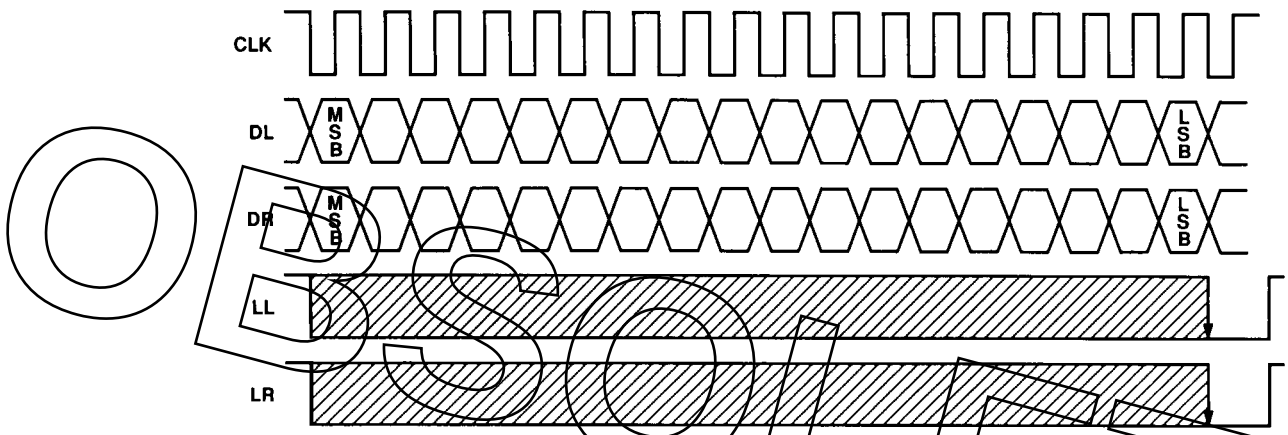


Figure 9. AD1864 Control Signals

INPUT DATA

Data is transmitted to the AD1864 in a bit stream composed of 18-bit words with a serial, 2s complement, MSB first format. Data Left (DL) and Data Right (DR) are the serial inputs for the left and right DACs, respectively. Similarly, Latch Left (LL) and Latch Right (LR) update the left and right DACs. The falling edges of LL and LR cause the last 18 bits which were clocked into the Serial Registers to be shifted into the DACs, thereby updating the DAC outputs. Left and Right channels share the Clock (CLK) signal. Data is clocked into the input registers on the rising edge of CLK.

Figure 9 illustrates the general signal requirements for data transfer for the AD1864.

TIMING

Figure 10 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1864 are both TTL and 5 V CMOS compatible.

The minimum clock rate of the AD1864 is at least 12.7 MHz. This clock rate allows data transfer rates of 2×, 4×, 8× and $16 \times F_S$ (where F_S equals 44.1 kHz). The applications section of this datasheet contains additional guidelines for using the AD1864.

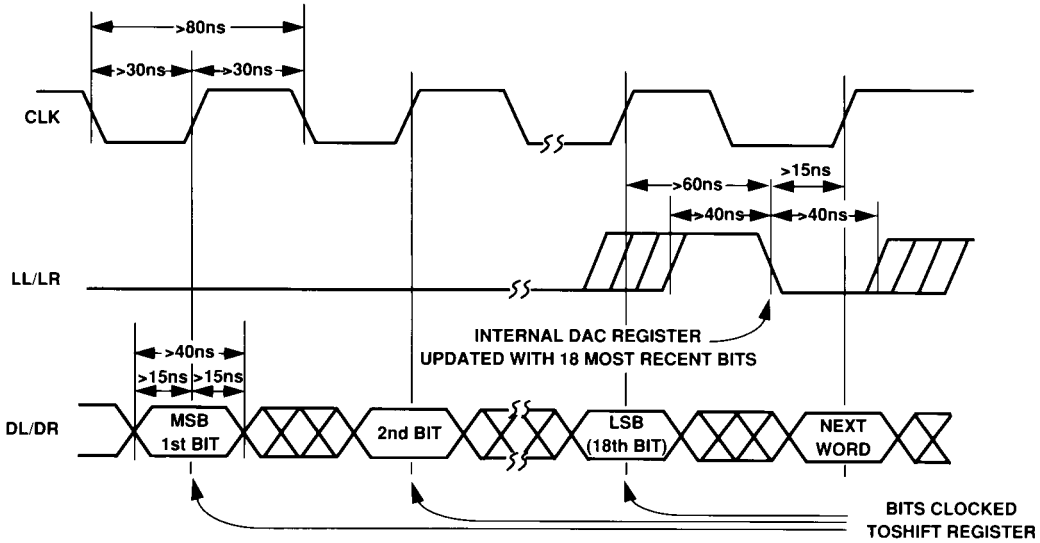


Figure 10. AD1864 Timing Diagram

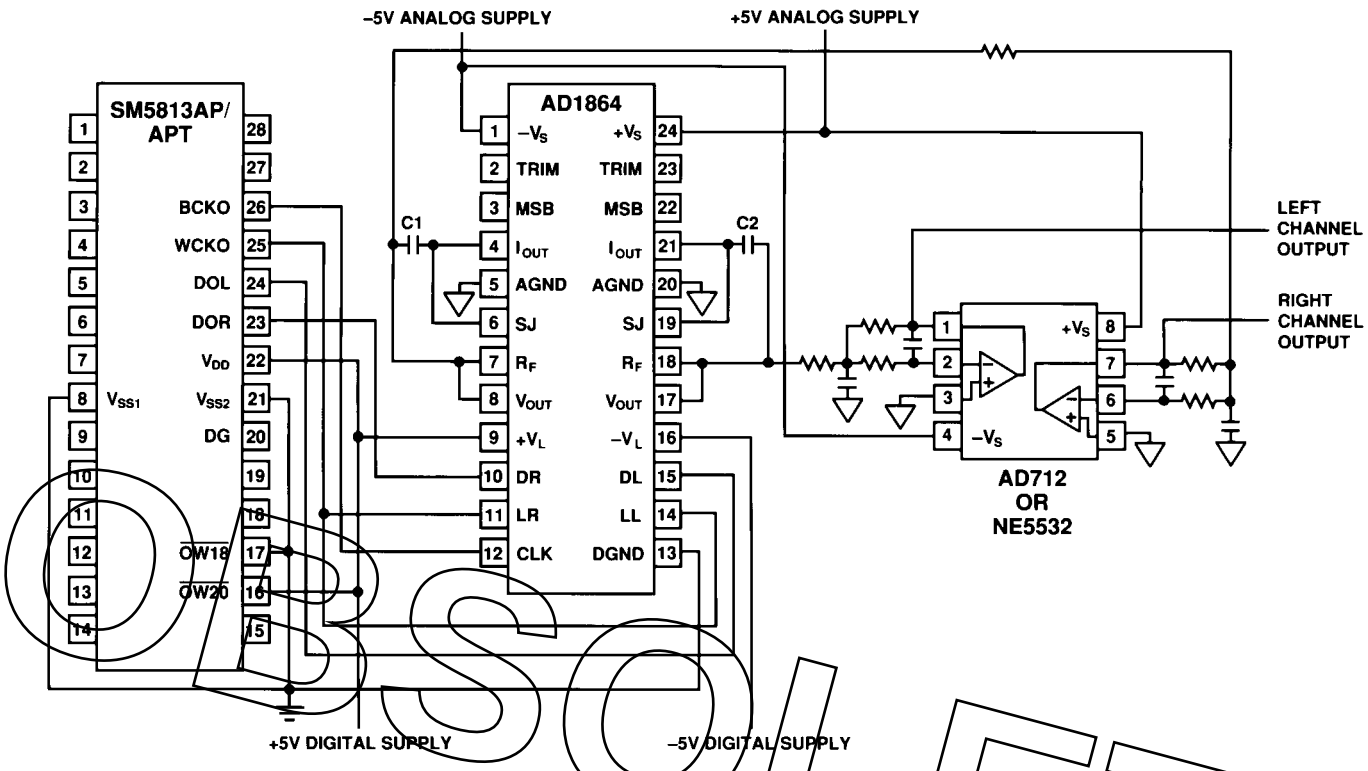


Figure 11. Complete 8 × F_S 18-Bit CD Player

18-BIT CD PLAYER DESIGN

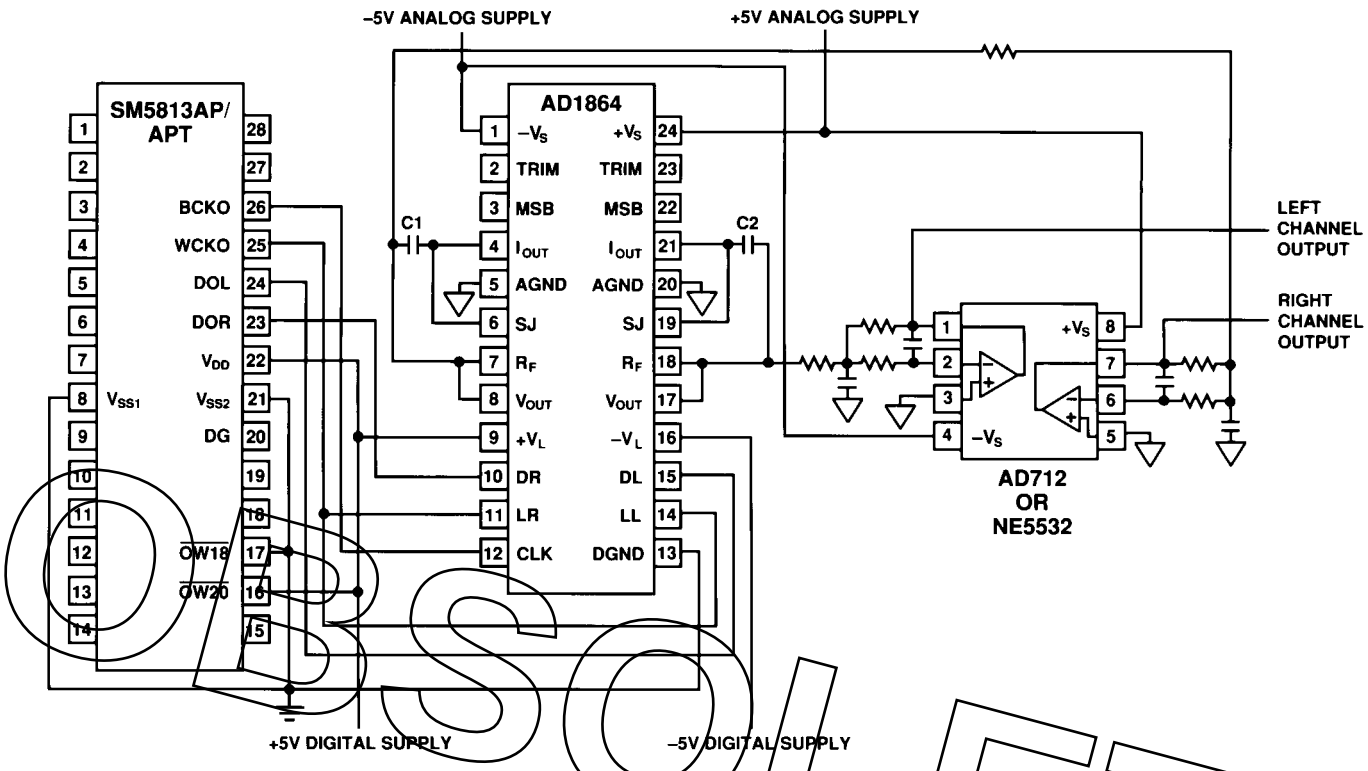
Figure 11 illustrates an 18-bit CD player design incorporating an AD1864 D/A converter, an AD712 or NE5532 dual op amp and the SM5813 digital filter chip manufactured by NPC. In this design, the SM5813 filter transmits left and right digital data to both channels of the AD1864. The left and right latch signals, LL and LR, are both provided by the word clock signal (WCKO) of the digital filter. The digital filter supplies data at an 8 × F_S oversample rate to each channel.

The digital data is converted to analog output voltages by the output amplifiers on the AD1864. Note that no external components are required by the AD1864. Also, no deglitching circuitry is required.

An AD712 or NE5532 dual op amp is used to provide the output antialias filters required for adequate image rejection. One 2-pole filter section is provided for each channel. An additional pole is created from the combination of the internal feedback resistors (R_F) and the external capacitors C1 and C2. For example, the nominal 3 kΩ R_F with a 360 pF capacitor for C1 and C2 will place a pole at approximately 147 kHz, effectively eliminating all high frequency noise components.

Close matching of the ac characteristics of the amplifiers on the AD712 as well as their low distortion make it an ideal choice for the task.

Low distortion, superior channel separation, low power consumption and a low component count are all realized by this simple design.



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Close matching of the ac characteristics of the amplifiers on the AD712 as well as their low distortion make it an ideal choice for the task.

Low distortion, superior channel separation, low power consumption and a low component count are all realized by this simple design.

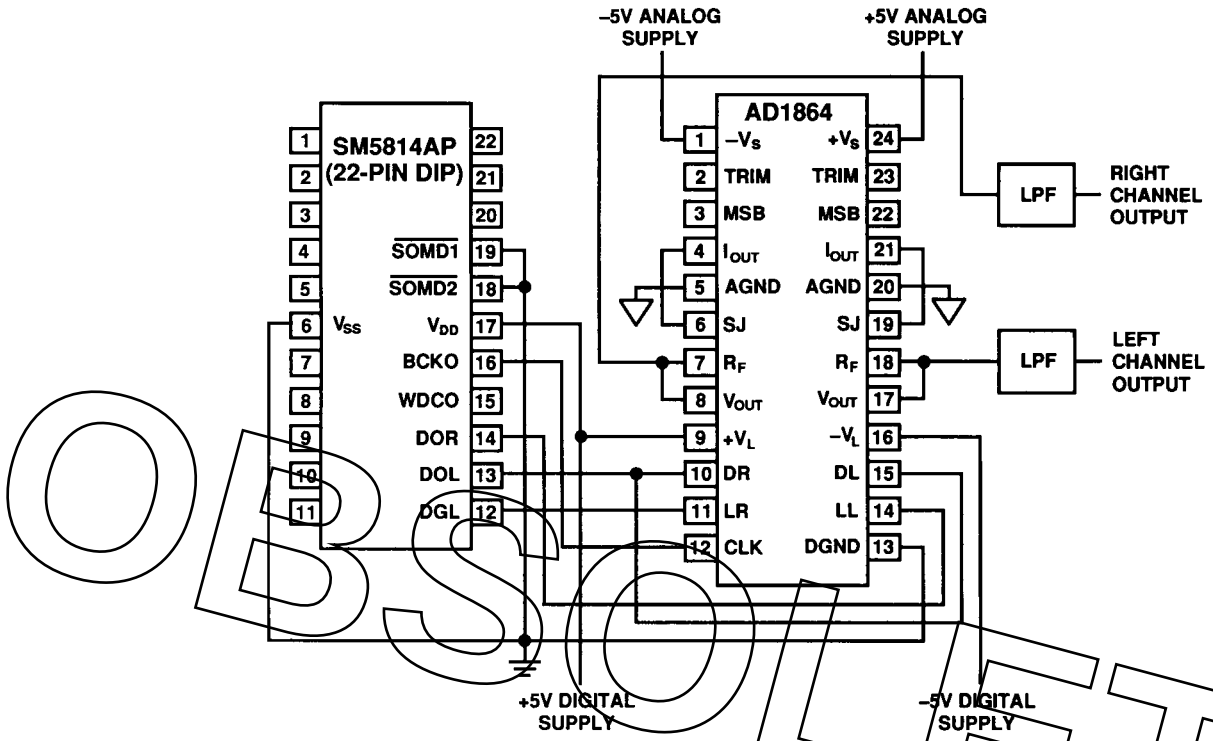


Figure 13. AD1864 with NPC SM5814AP Digital Filter

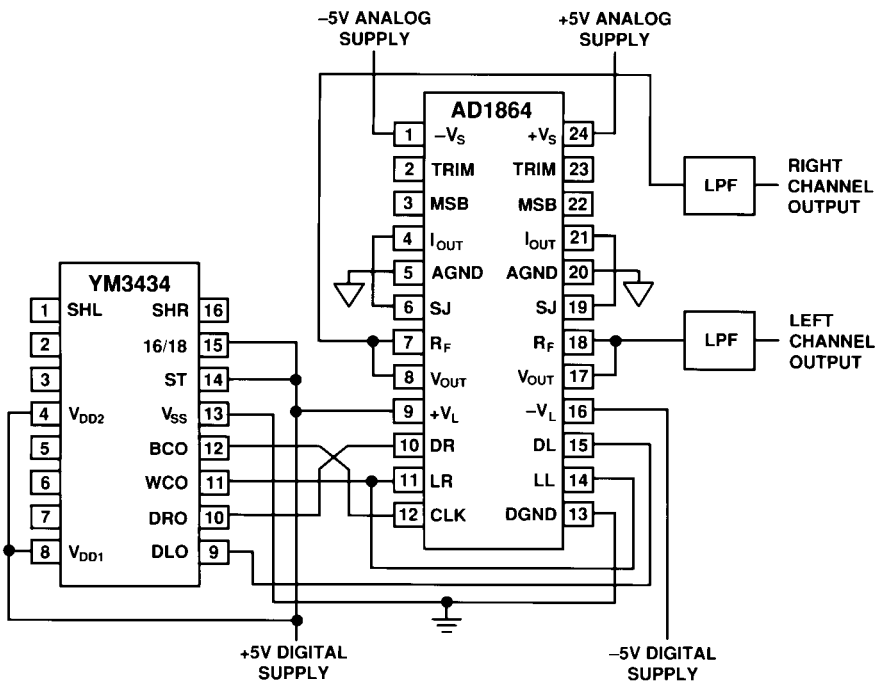


Figure 14. AD1864 with Yamaha YM3434 Digital Filter

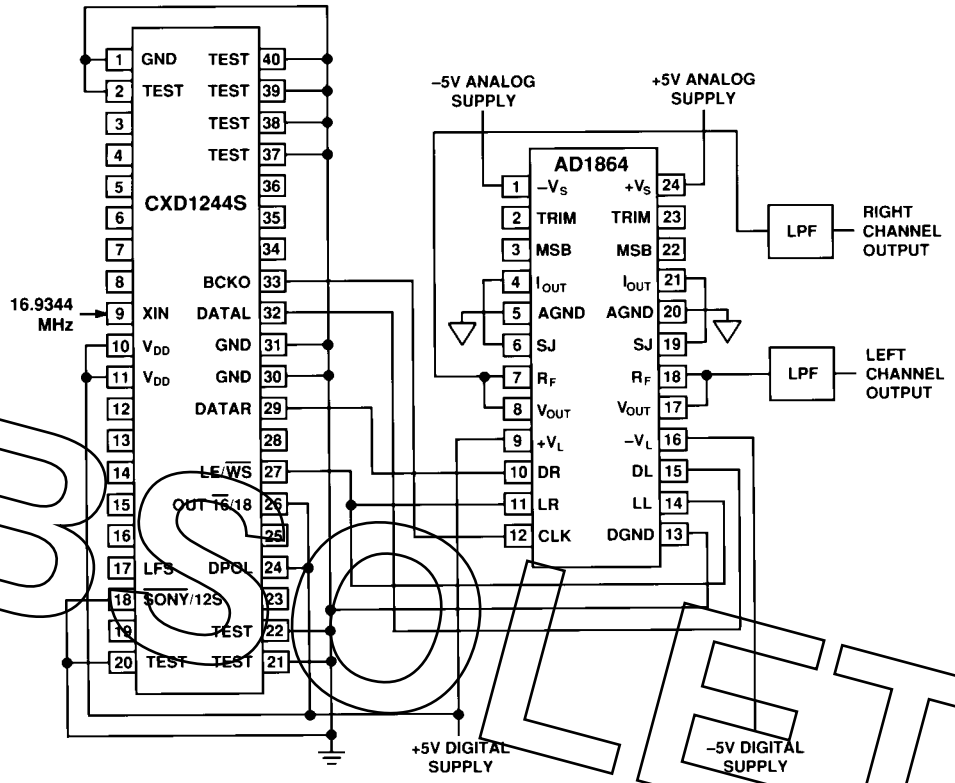


Figure 15. AD1864 with Sony CXD1244S Digital Filter

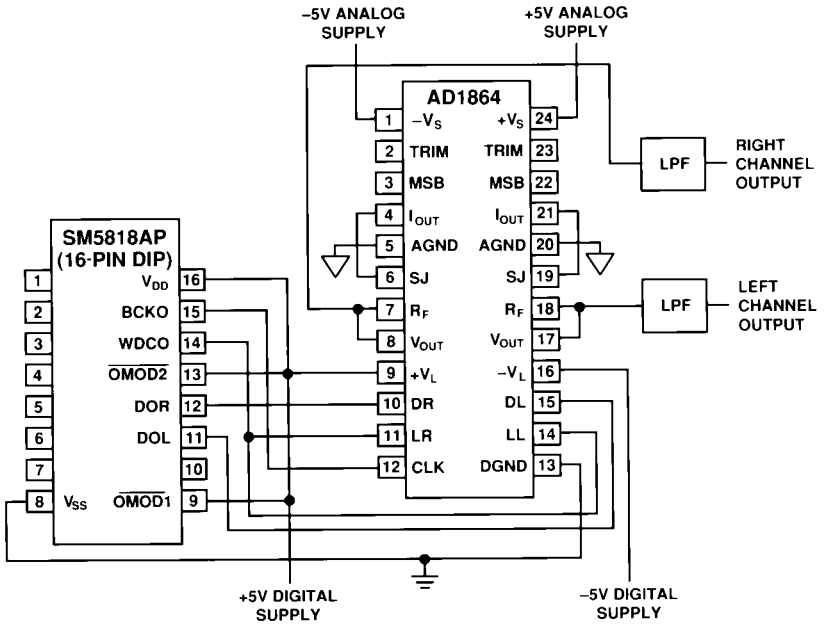
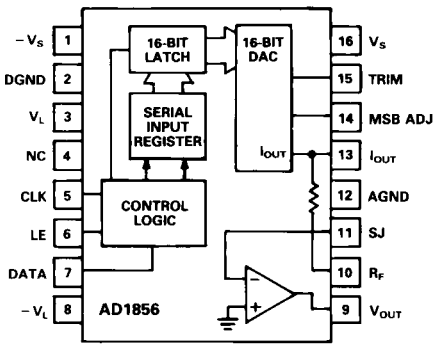
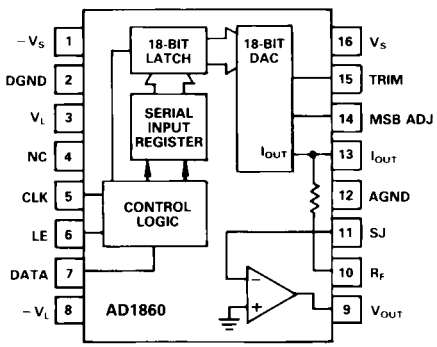


Figure 16. AD1864 with NPC SM5818AP Digital Filter

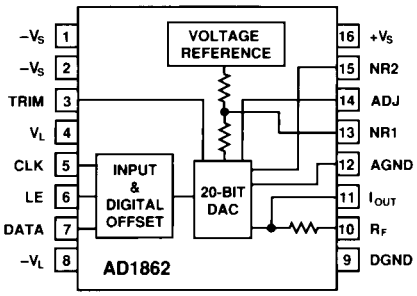
OTHER DIGITAL AUDIO COMPONENTS AVAILABLE FROM ANALOG DEVICES



NC = NO CONNECT



NC = NO CONNECT



AD1856 16-BIT AUDIO DAC
Complete, No External Components Required
0.0025% THD
Low Cost
16-Pin DIP or SOIC Package
Standard Pinout

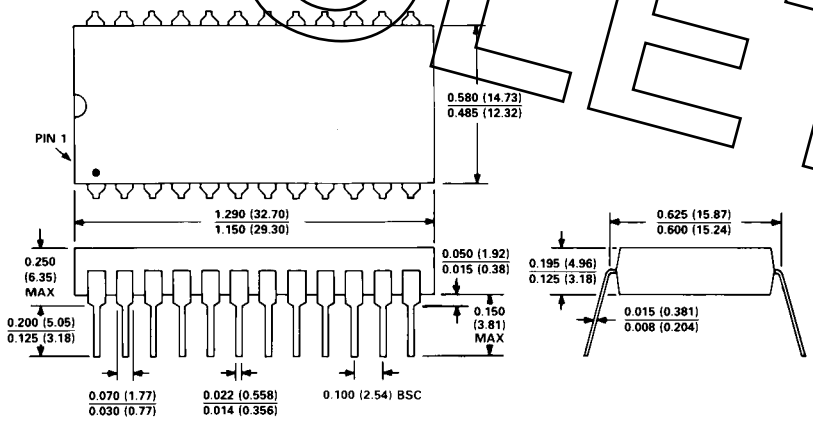
AD1860 18-BIT AUDIO DAC
Complete, No External Components Required
0.002% THD+N
108 dB Signal-to-Noise Ratio
16-Pin DIP or SOIC Package
Standard Pinout

AD1862 20-BIT AUDIO DAC
120 dB Signal-to-Noise Ratio
0.0012% THD+N
105 dB D-Range Performance
±1 dB Gain Linearity
16-Pin DIP

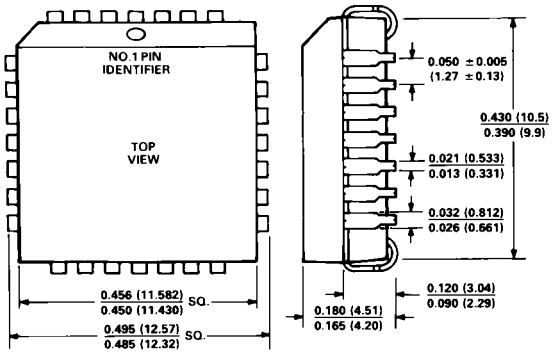
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Pin Plastic DIP



28-Pin PLCC



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