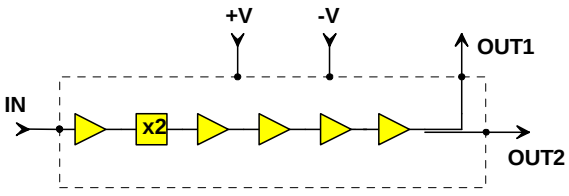
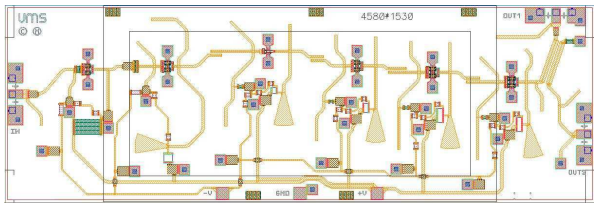
W-band Multifunction: Multiplier / MPA

GaAs Monolithic Microwave IC

Description

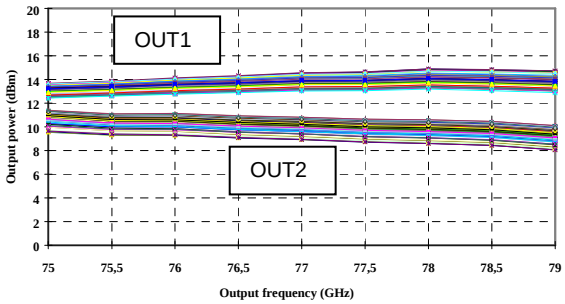
The CHU2277a is a W-band monolithic multifunction which integrates a frequency multiplier, a four-stage amplifier and a power divider. The frequency multiplier is based on an active transistor and allows operating at low input level with reduced power consumption. This chip provides two outputs at 77GHz, the main one is for the transmission path and the auxiliary one for the receiving mixer(s) LO signal. All the active devices are internally self-biased. This chip is compatible with automatic equipment for assembly.
The circuit is manufactured with the P-HEMT process: 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.





Main Features

- Wide operating frequency range
- Low input power : 5dBm typical
- High output power (OUT1)
- Auxiliary output power (OUT2
- Low AM noise
- High temperature range
- On-chip self biasing
- Low DC power consumption
- BCB layer protection
- Chip size: 4.65x1.6x0.1mm



Typical output power characteristic
Pin = 7dBm (on wafer measurement)

Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	38.0		38.5	GHz
P_in	Input power	0	5	12	dBm
P_out1	Output power (OUT1)		13		dBm
P_out2	Output power (OUT2)		10		dBm

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

United Monolithic Semiconductors S.A.S.
Route Départementale 128 - BP46 - 91401 Orsay Cedex France
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Main Characteristics

Tamb.= +25℃

Symbol	Parameter	Min	Typ	Max	Unit
F_in	Input frequency	38.0		38.5	GHz
F_out	Output frequency	76		77	dB
P_in	Input power	0	5	12	dB
P_out1	Output power (OUT1) (1)		13		dBm
P_out2	Output power (OUT2) (2)		10		dBm
Fin_rej	Fundamental rejection (dBc/Pout1(2Fin))		55		dBc
S_rej	Spurious rejection (Harmonic Rejection)				
	74 GHz		40		dBc
	111 GHz		40		dBc
	Spurious rejection (Non Harmonic Rej.)				
	76.5GHz		40		dBc
An	Amplitude noise @ 1KHz (SSB)		-137		dBc/Hz
	Amplitude noise @ 10KHz (SSB)		-145		dBc/Hz
	Amplitude noise @ 100KHz (SSB)		-151		dBc/Hz
	Amplitude noise @ 200KHz (SSB)		-153		dBc/Hz
	Amplitude noise @ 1MHz (SSB)		-157		dBc/Hz
VSWR_in	VSWR at input port (50Ω)		2:1	2.5:1	
+V	Positive supply voltage (2)	4.4	4.5	4.6	V
+I	Positive supply current		180	240	mA
-V	Negative supply voltage (2)	-4.6	-4.5	-4.4	V
-I	Negative supply current		14	20	mA
Top	Operating temperature range	-40		100	℃

(1) Defined on load VSWR ≤ 1.5:1
(2) Negative supply voltage must be applied at least 1µs before positive supply voltage

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Absolute Maximum Ratings

Tamb.= +25℃ (1)

Symbol	Parameter	Values	Unit
P_in	Input power (2)	13	dBm
+V	Positive supply voltage	5	V
-V	Negative supply voltage	-5	V
+I	Positive supply current	250	mA
-I	Negative supply current	20	mA
Tstg	Storage temperature range	-55 to +155	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

Typical Bias Conditions

Tamb.= +25℃

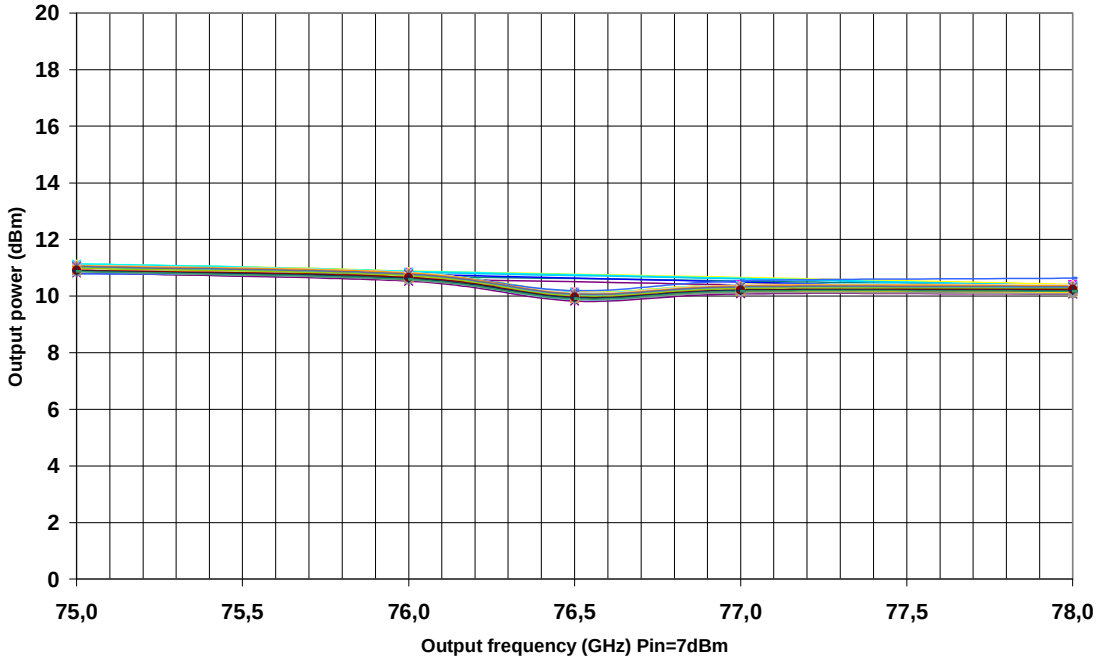
Symbol	Pad N°	Parameter	Values	Unit
+V	10	Positive supply voltage	+4.5	V
-V	12	Negative supply voltage	-4.5	V

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

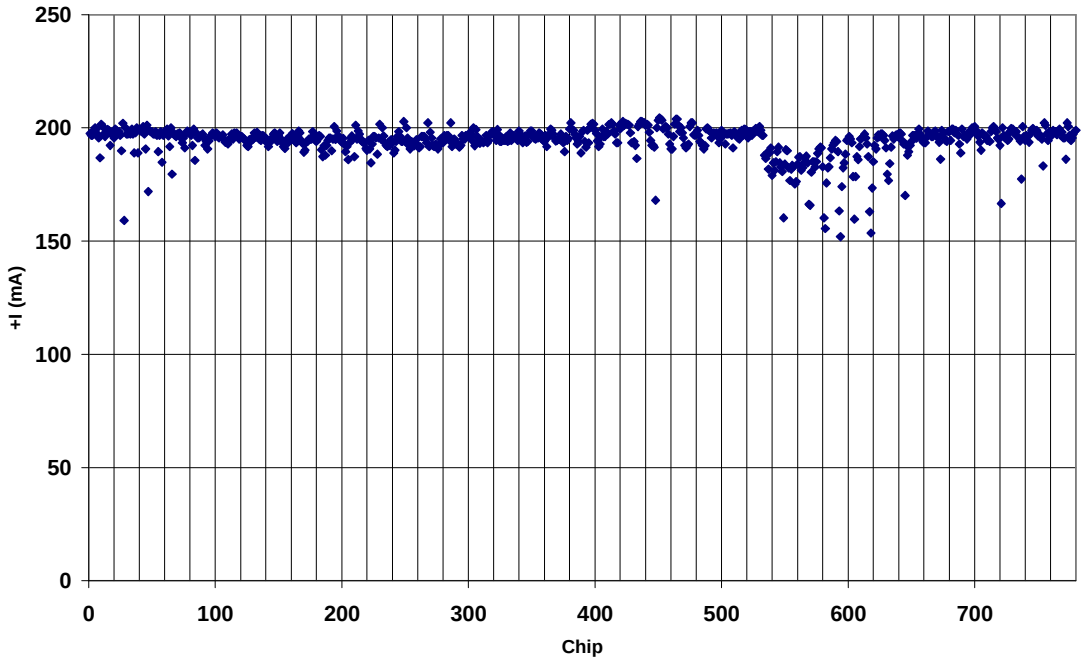
Typical on wafer Measurements

Tamb.= +25℃, Vd = +4.5V, +I = 200mA

Output power (OUT2): P_in=+6dBm



Positive supply current (F_in=38.25GHz, P_in=+6dBm)

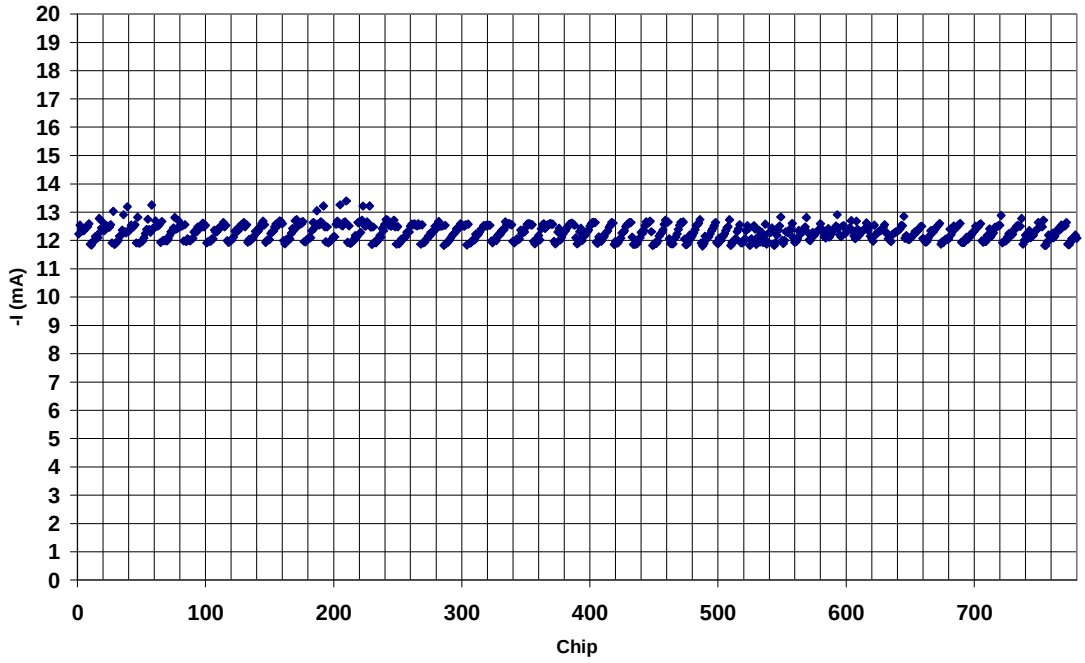


Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Typical on wafer Measurements

Tamb.= +25℃, +V = +4.5V, -V=-4.5V

Negative supply current (F_in=38.25GHz, P_in=+6dBm)

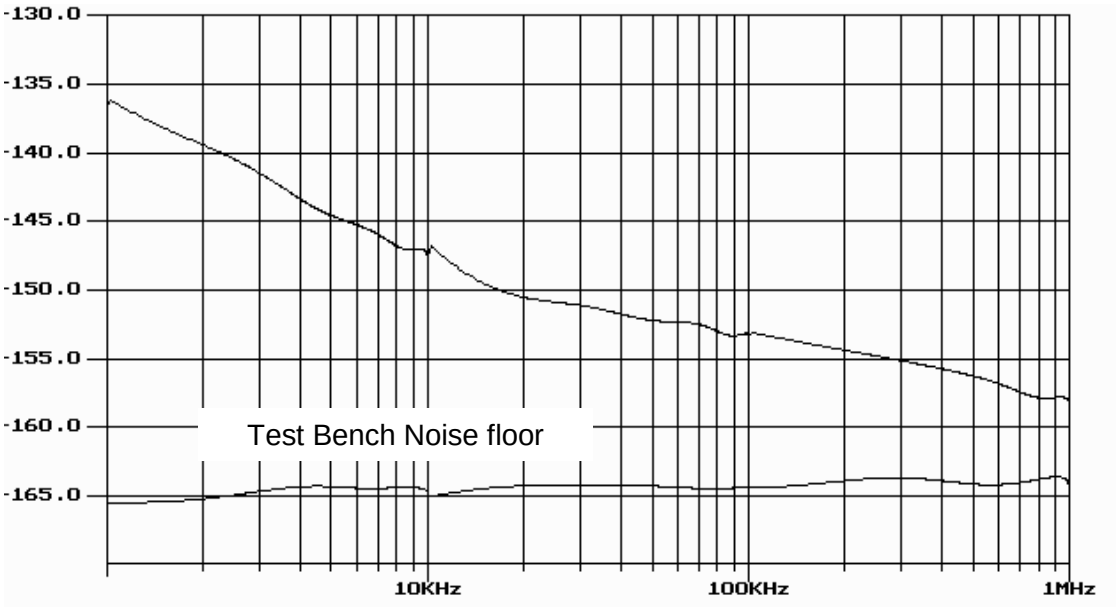


AM Noise over temperature (F_in=38.25GHz P_in=+4dBm)

AM NOISE

(CHU2277 (Tx2) in test jig, @ T=25℃, Vd=+4.5V, Out _freq=76.5GHz)

dBc/Hz

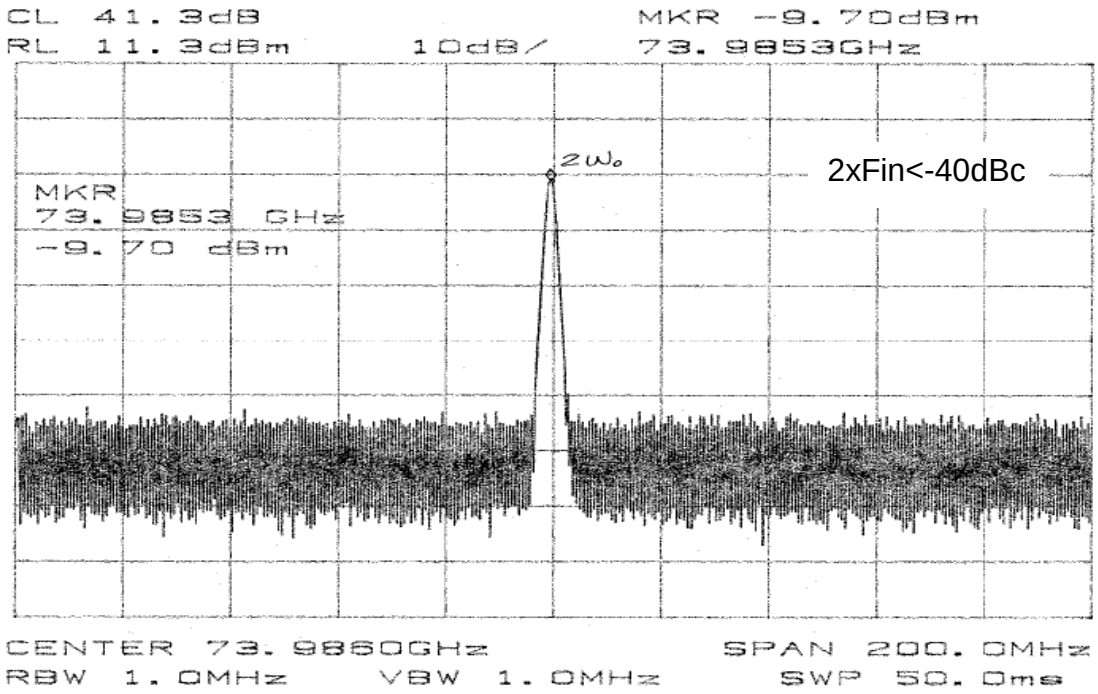


Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

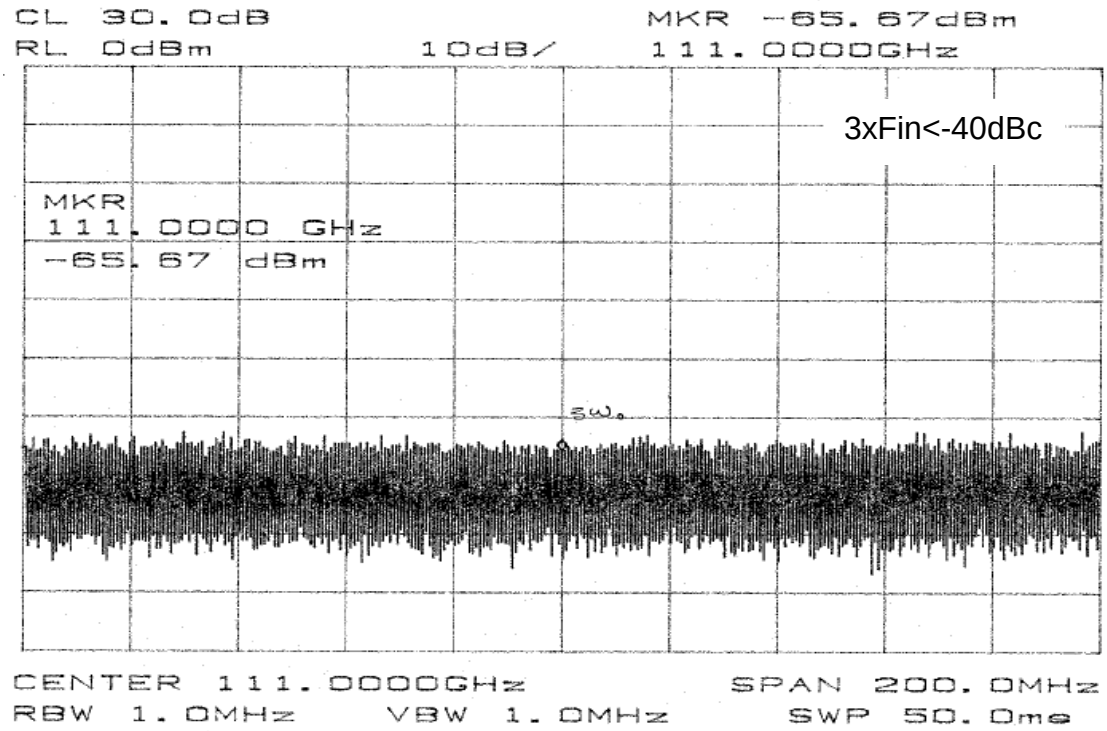
Typical on wafer Measurements

Tamb.= +25℃, +V = +4.5V, -V = -4.5V

Harmonic Spurious Rejection: F_out=74GHz, P_in=+7dBm



Harmonic Spurious Rejection: F_in=74GHz, P_in=+7dBm



Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Typical on wafer Measurements

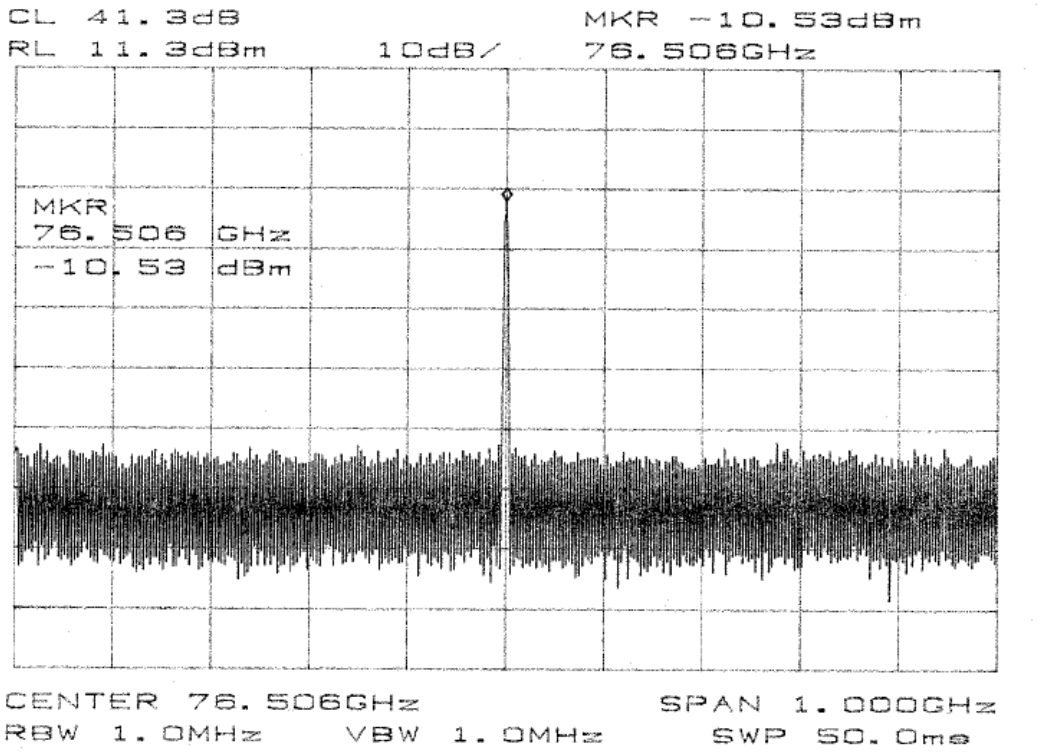
Tamb.= +25℃, +V = +4.5V, -V = -4.5V

No Harmonic Spurious Rejection: F_out=76.5GHz, P_in=+7dBm

NON HARMONIC SPURIOUS

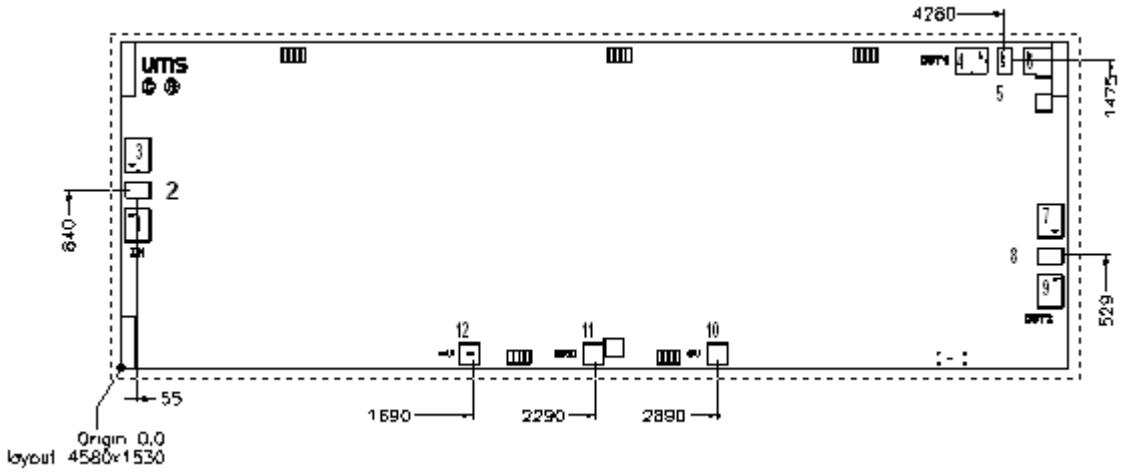
2.Fin output signal => **Non harmonic < -40 dBc**

(3 stage version 7352 in test jig @ T=25℃, Vd=4,5V , 2.Fin_Out_freq=76.5 GHz, input power=7 dBm)



Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Mechanical data

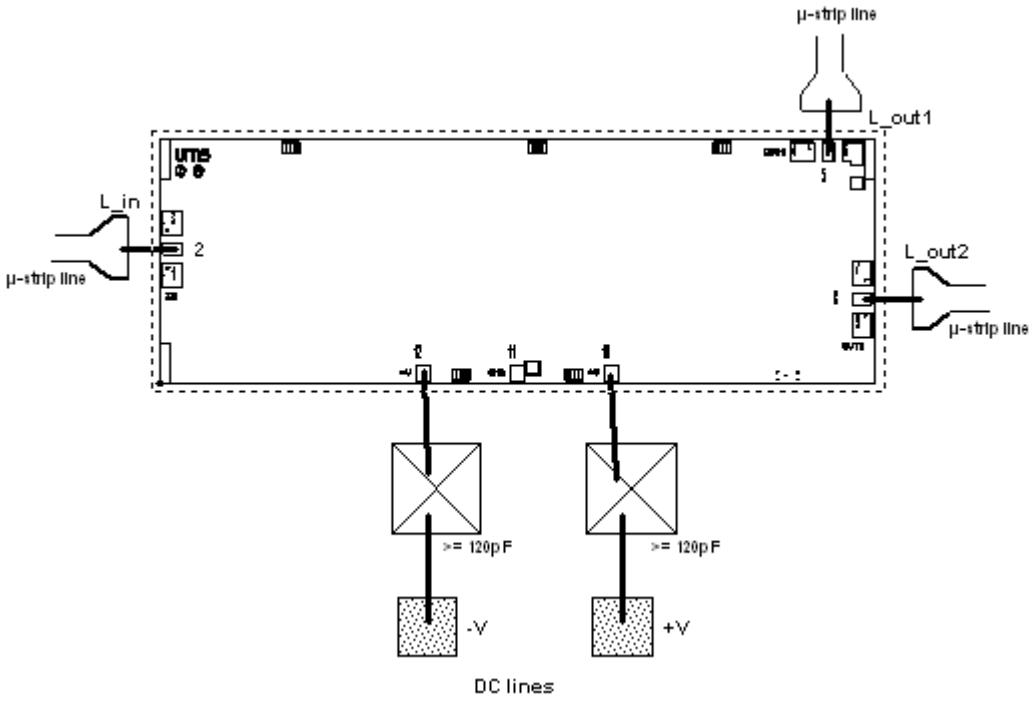


Unit = µm
External chip size (layout size + dicing streets) = 4650x1600 ±35
Chip thickness = 100 ±10
HF Pads (2, 5,8) = 105x86 (BCB opening)
DC Pads = 86x83 (BCB opening)

Pin number	Pin name	Description
1, 3, 4, 6, 7, 9		Ground: should not be bonded. If required, please ask for more information
11		Ground (optional)
2	IN	Input port
5	OUT1	Main output
8	OUT2	Auxiliary output
10	+V	Positive supply voltage
12	-V	Negative supply voltage

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Recommended assembly plan



25µm wedge bonding is preferred

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

This drawing shows an example of assembly and bias configuration. All the transistors are internally self-biased. An external capacitor is recommended for the positive and negative supply voltages.

For the RF pads the equivalent wire bonding inductance (diameter=25µm) have to be according to the following recommendation.

Recommended circuit bonding table

Port	Equivalent inductance (nH)	Wire length (mm) [1]
IN (2)	L_in=0.32	0.4
OUT1 (5)	L_out1=0.32	0.4
OUT2 (8)	L_out2=0.32	0.4

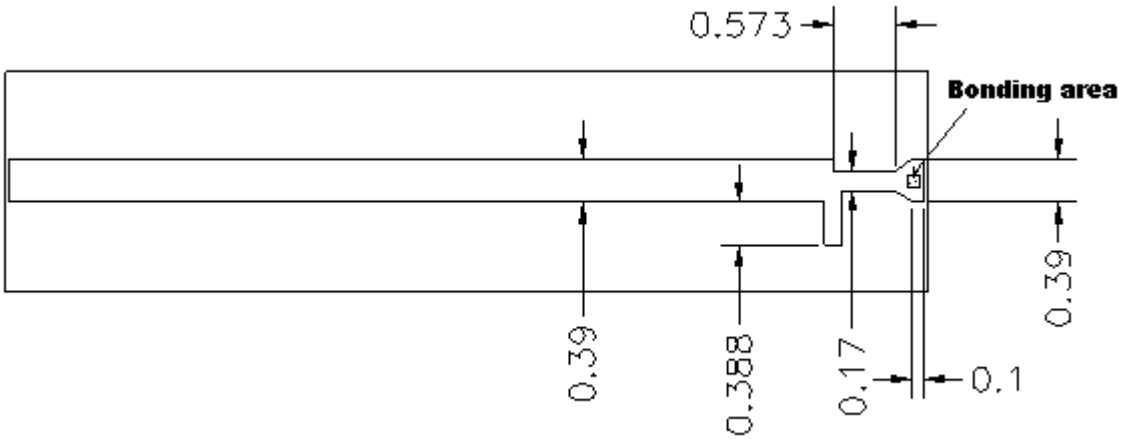
[1] This value is the total length including the necessary loop from pad to pad.

For a micro-strip configuration a hole in the substrate is necessary for chip assembly

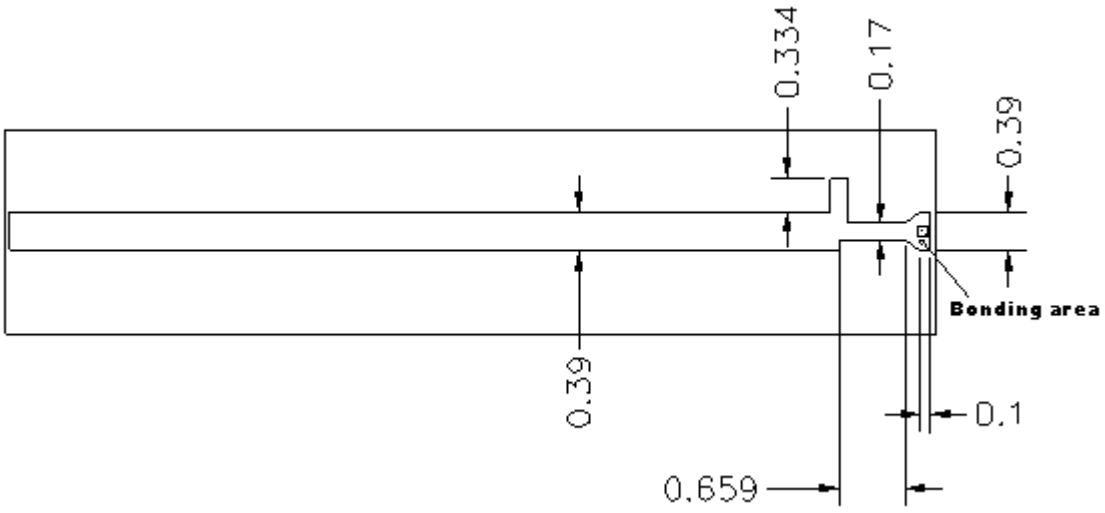
Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Notes

As the connections at 77GHz (between MMIC and MMIC or between MMIC and external substrate) are critical, the transition matching network is split into two parts: one on MMIC and one on the external substrate. This choice allows doing, for OUT2 port, a direct connection between MMICs. For a connection to an external substrate a network is proposed on soft substrate for OUT1 and OUT2 ports. The following drawings gives the dimensions for a DUROID substrate (thickness=0.127mm, ε_r=2.2).



Proposed matching network for a 50Ω transition between OUT1 and a µ-strip line on DUROID substrate.



Proposed matching network for a 50Ω transition between OUT2 and a µ-strip line on DUROID substrate.

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Notes

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form: CHU2277a98F/00

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09