Datasheet

Beam-forming

Signal Processing IC for Ultra- Directional Microphone Effect

BU8332CKV-M

Automotive Grade

General Description

BU8332CKV-M enables cardioid directivity through beam-forming technology using two omnidirectional microphones placed 10mm apart. Beam forming technology provides sharper directivity than unidirectional microphones. Features include selection of different polar patterns of response, adjustable sharpness of directivity via zoom function and switchable direction sensitivity. The processor enables hands-free calling and improves speech recognition in a variety of devices.

Features

- Directional Microphone Function (Beam-forming)
- Microphone Pitch: 10mm
- Selectable Polar Patterns of Response
- Adjustable Sharpness of Directivity
- Switchable Direction Sensitivity
- Digital Block Powered by Internal 1.5V Regulator
- Built-in Microphone Bias and Pre-amplifier
- Analog Microphone Inputs (Differential or Single Ended)x 2ch
- Analog Line Output
- PCM Output
- 2-wire Host Interface(Slave Address : 0x61)
- Stand-alone Operation with External EEPROM

Applications

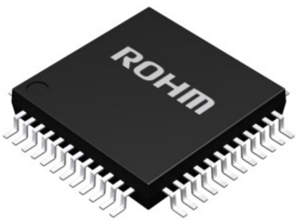
- Hands-free Operation / Speech Recognition in Car Navigation Systems
- Portable Devices such as Mobile Phones, Smart Phones, Headset, or Game Machines
- Applications that Require Voice Input

Key Specifications

- Operating Power Supply Range: 3.0V to 3.6V
- Operating Temperature Range: -40℃ to +85℃
- Operating Current: 15mA(Typ)
- Deep Standby Current: 1µA(Typ)
- Polar Pattern Type: "Cardioid", "Bidirectional", "Hyper-cardioid"

Package

	W(Typ) x D(Typ) x H(Max)
VQFP48	9.00mm x 9.00mm x 1.625mm



Typical Application Circuit

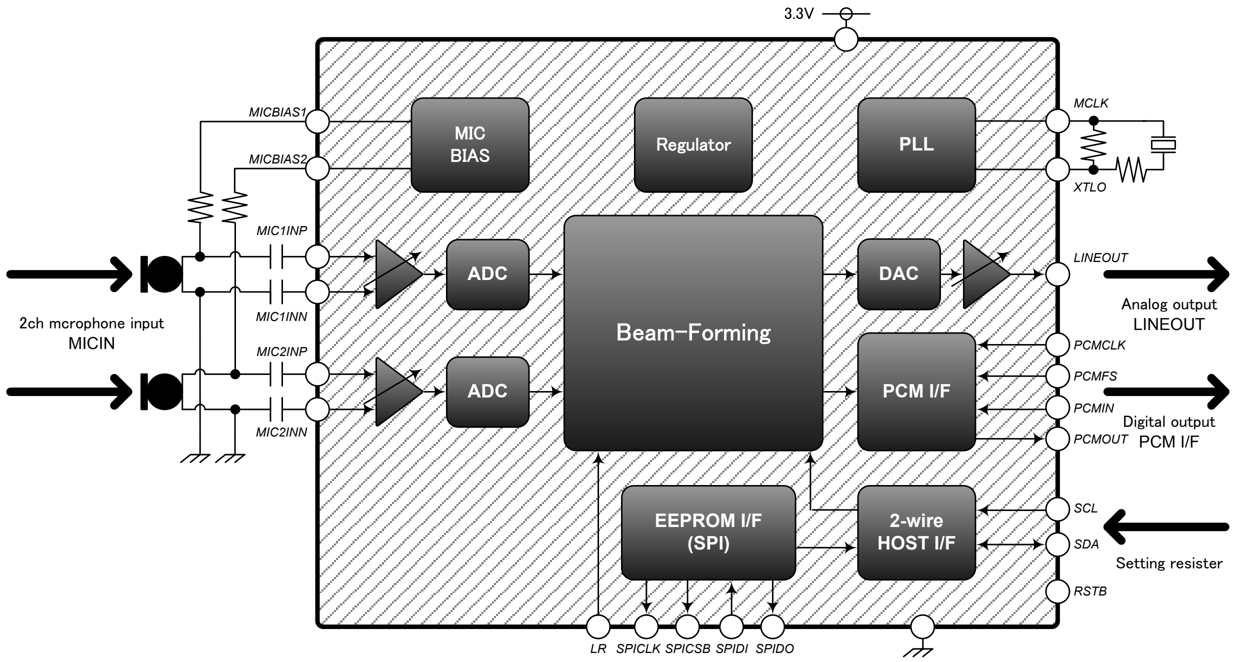


Figure 1 Typical Application Circuit

○Product structure:Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

Pin Configuration

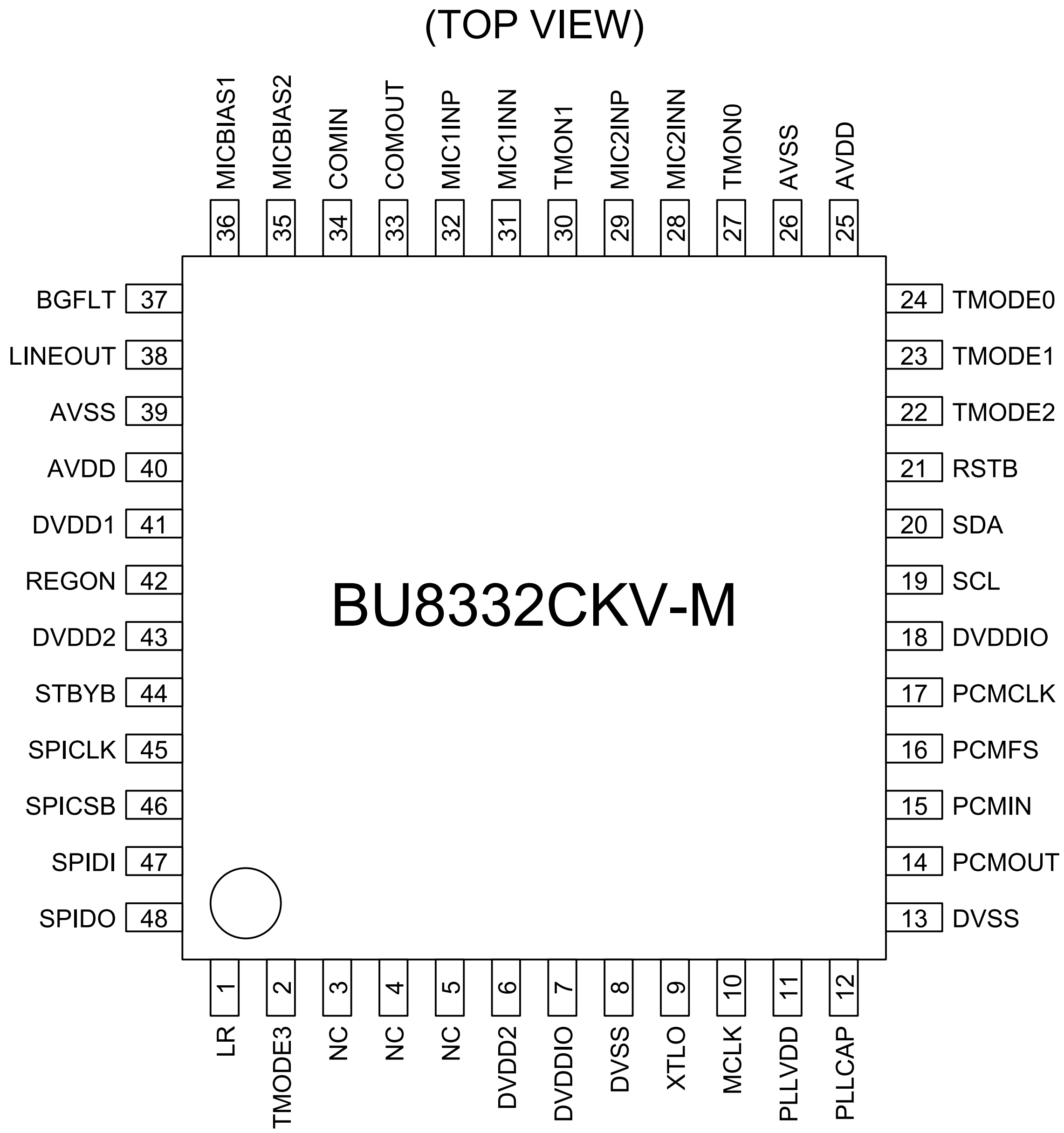


Figure 2 Pin Configuration

Pin Description

Pin No.	Symbol	I/O	Function	Power supply system	I/O equal circuit
1	LR	I	To select directional axis (“L”: Left, ”Open”: Right)	DVDDIO	A
2	TMODE3	I	Test pin (Open)	DVDDIO	A
3	NC	-	NC	-	-
4	NC	-	NC	-	-
5	NC	-	NC	-	-
6	DVDD2	-	Digital power supply2 (Controlled by STBYB)	-	B
7	DVDDIO	-	I/O power supply	-	-
8	DVSS	-	Digital GND	-	-

Pin No.	Symbol	I/O	Function	Power supply system	I/O equal circuit
9	XTLO	O	Oscillator output	DVDDIO	C
10	MCLK	I	External clock input / Oscillator input	DVDDIO	C
11	PLLVDD	-	PLL power supply	-	-
12	PLLCAP	O	PLL filter pin (Recommended 56nF to DVSS)	PLLVDD	D
13	DVSS	-	Digital GND	-	-
14	PCMOUT	O	PCM signal output	DVDDIO	E
15	PCMIN	I	PCM signal input	DVDDIO	F
16	PCMFS	I	PCM frame signal input	DVDDIO	F
17	PCMCLK	I	PCM clock input	DVDDIO	F
18	DVDDIO	-	I/O power supply	-	-
19	SCL	I	Serial Clock input for 2-wire Host Interface	DVDDIO	J
20	SDA	I/O	Serial Data for 2-wire Host Interface (Data input or output)	DVDDIO	H
21	RSTB	I	Reset pin (“L” : Power down)	DVDDIO	G
22	TMODE2	I	Test pin (Connect to DVSS)	DVDDIO	F
23	TMODE1	I	Test pin (Connect to DVSS)	DVDDIO	F
24	TMODE0	I	Test pin (Connect to DVSS)	DVDDIO	F
25	AVDD	-	Analog power supply	-	-
26	AVSS	-	Analog GND	-	-
27	TMON0	O	Test pin (Open)	AVDD	D
28	MIC2INN	I	Analog microphone input (2-)	AVDD	D
29	MIC2INP	I	Analog microphone input (2+)	AVDD	D
30	TMON1	O	Test pin (Open)	AVDD	D
31	MIC1INN	I	Analog microphone input (1-)	AVDD	D
32	MIC1INP	I	Analog microphone input (1+)	AVDD	D
33	COMOUT	O	Analog reference voltage output (Recommended 1µF to AVSS)	AVDD	D
34	COMIN	I	Analog reference voltage (Recommended 1µF to AVSS)	AVDD	D
35	MICBIAS2	O	Microphone bias output2	AVDD	D
36	MICBIAS1	O	Microphone bias output1	AVDD	D
37	BGFLT	O	Bias filter pin (Recommended 0.1µF to AVSS)	AVDD	D
38	LINEOUT	O	Line output	AVDD	D
39	AVSS	-	Analog GND	-	-
40	AVDD	-	Analog power supply	-	-
41	DVDD1	-	Digital power supply1 (Direct input)	-	-
42	REGON	I	To control 1.5V regulator (“L”:OFF, “H”:ON)	DVDDIO	I
43	DVDD2	-	Digital power supply2 (Controlled by STBYB)	-	B
44	STBYB	I	To control standby (“L” : Power down, ”H” : Normal)	DVDDIO	I
45	SPICLK	O	SPI clock output	DVDDIO	E
46	SPICSB	O	SPI chip select output	DVDDIO	E
47	SPIDI	I	SPI data input	DVDDIO	F
48	SPIDO	O	SPI data output	DVDDIO	E

“H” level is voltage value of DVDDIO, ”L” level is voltage value of DVSS.

Block Diagram

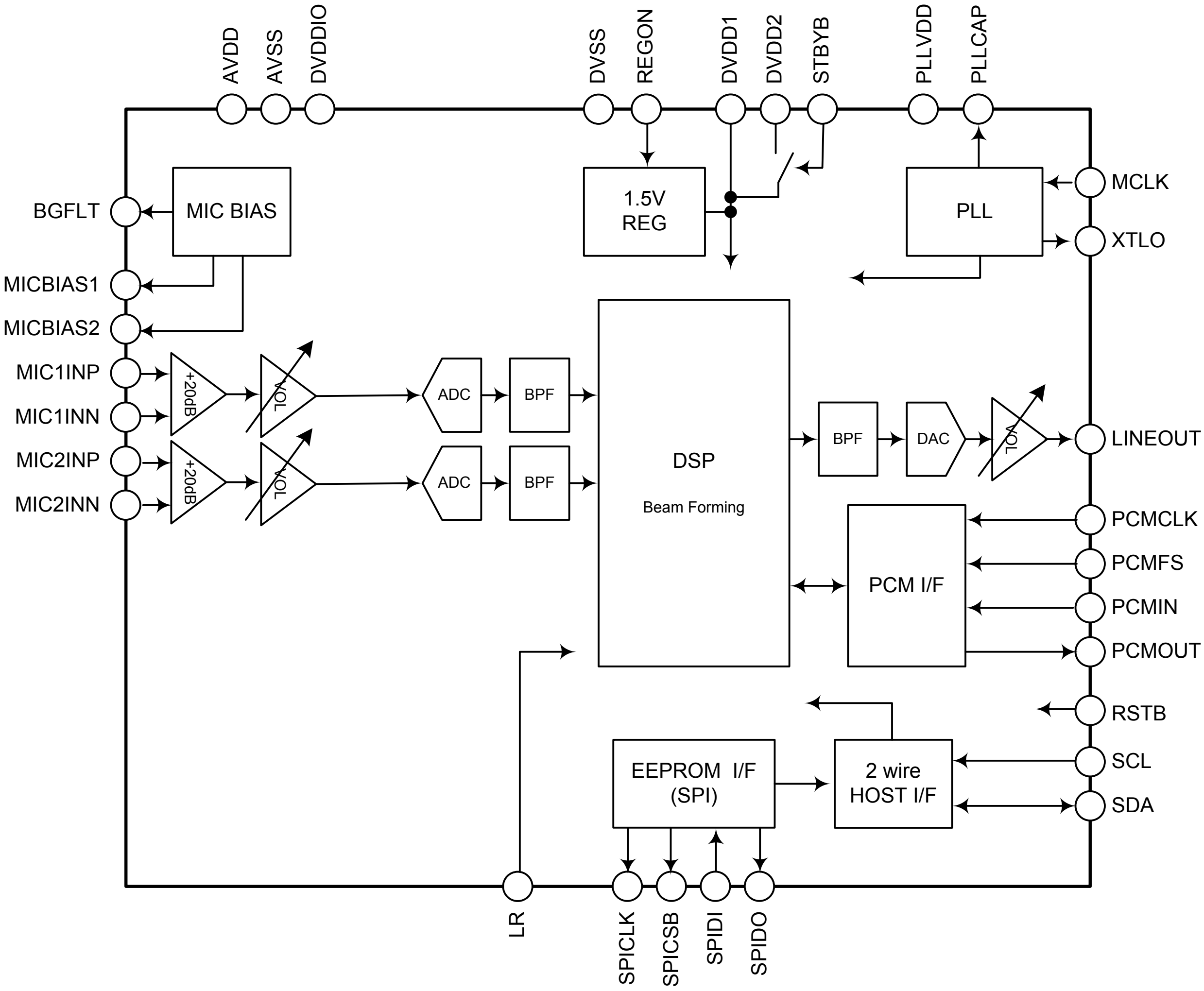


Figure 3 Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit.
Analog power supply	AVDD	-0.3 to 4.5	V
PLL power supply	PLLVDD	-0.3 to 4.5	V
I/O power supply	DVDDIO	-0.3 to 4.5	V
Digital power supply	DVDD1 DVDD2	-0.3 to 2.16	V
Analog input voltage	VTA	AVSS-0.3 to AVDD+0.3	V
Digital input voltage	VTD	DVSS-0.3 to DVDDIO+0.3	V
Input current *1	IIN	-10 to +10	mA
Power Dissipation *2	Pd	0.90	W
Storage temperature range	TS	-50 to 125	℃

*1: I/O B, J and H of Equivalence Circuits are not included.
*2: For operating over 25℃, de-rate the value at 9mW/℃.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Analog power supply	AVDD	3.0	3.3	3.6	V
PLL power supply	PLLVDD	3.0	3.3	3.6	V
I/O power supply	DVDDIO	DVDD1 DVDD2	3.3	3.6	V
Digital power supply	DVDD1	1.4	1.5	1.6	V
	DVDD2	1.45	1.5	1.6	V
Clock input frequency	FMCLK	4	-	8	MHz
Duty	DMCLK	40	50	60	%
Operating temperature range	Ta	-40	25	85	℃

Electrical Characteristics

◆DC Characteristics

Application Circuit (Figure 33), Ta=25℃, AVDD=3.3V, PLLVDD=3.3V, REGON=”H” unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Current *3	IST	-	10	90	μA	Standby (Setting register)
	IDST	-	1	5	μA	Deep standby (STBYB=”L”)
	IDD	-	15	30	mA	FS=16kHz,BF=ON
Digital Hi level input voltage	VIH	0.7* DVDDIO	-	-	V	-
Digital Low level input voltage	VIL	-	-	0.3* DVDDIO	V	-
Digital Hi level input current	IIH	-	-	1.0	μA	VIH=DVDDIO (Pull-down resistance input pins are excluded)
Digital Low level input current	IIL	-1.0	-	-	μA	VIL=DVSS
Digital Hi level output voltage	VOH	0.8* DVDDIO	-	-	V	IOH=-1mA
Digital Low level output voltage	VOL	0	-	0.2* DVDDIO	V	IOL=1mA
Digital Low level output voltage	VOL	0	-	0.2* DVDDIO	V	IOL=3mA (SDA)
Regulator output voltage	VREG	-	1.5	-	V	

*3 Digital and analog output pin is no-load.

◆CODEC Characteristics

Application Circuit (Figure 33), Ta=25°C, AVDD=3.3V, PLLVDD=3.3V, REGON="H", BF=OFF
FS=16 kHz, MIC1VOL/MIC2VOL/LOUTVOL=0dB unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Transmit signal-to-distortion ratio + Noise MICIN → PCMOUT	SDT	45	-	-	dB	Input signal:0dBm0, 1020Hz Using filter:20kHz LPF
Receive signal-to-distortion ratio + Noise PCMIN → LINEOUT	SDR	45	-	-	dB	Input signal:0dBm0, 1020Hz Using filter:20kHz LPF
Transmit gain tracking (-10dBm0 reference) MICIN → PCMOUT	GTX	-3.0	-	3.0	dB	Input signal:+3.0 to +0.5dBm0, 1020Hz Using filter:1020Hz BPF
		-1.0	-	1.0		Input signal:+0.5 to -40dBm0, 1020Hz Using filter:1020Hz BPF
		-2.0	-	2.0		Input signal:-40 to -55dBm0, 1020Hz Using filter:1020Hz BPF
Receive gain tracking (-10dBm0 reference) PCMIN → LINEOUT	GRX	-1.0	-	1.0	dB	Input signal:+3.0 to -40dBm0, 1020Hz Using filter:1020Hz BPF
		-2.0	-	2.0		Input signal:-40 to -55dBm0, 1020Hz Using filter:1020Hz BPF
Transmit reference level	VITX	0.037	0.050	0.068	Vrms	Input signal:0dBm0, 1020Hz Using filter:1020Hz BPF 20dB amplification in inside
Receive reference level	VORX	0.400	0.500	0.625	Vrms	Input signal:0dBm0, 1020Hz Using filter:1020Hz BPF
Transmit gain loss relative to frequency (1020Hz reference) MICIN → PCMOUT	GRTX	24	-	-	dB	Input signal:0dBm0, 0.06kHz Using filter:BPF
		0	-	2.5		Input signal:0dBm0, 0.2kHz Using filter:BPF
		-1.0	-	1.0		Input signal:0dBm0, 0.3 to 6.8kHz Using filter:BPF
		0	-	-		Input signal:0dBm0, 7.2kHz Using filter:BPF
		6.5	-	-		Input signal:0dBm0, 7.56kHz Using filter:BPF
Receive gain loss relative to frequency (1020Hz reference) PCMIN → LINEOUT	GRRX	24	-	-	dB	Input signal:0dBm0, 0.06kHz Using filter:BPF
		0	-	2.5		Input signal:0dBm0, 0.2kHz Using filter:BPF
		-1.0	-	1.0		Input signal:0dBm0, 0.3 to 6.8kHz Using filter:BPF
		0	-	-		Input signal:0dBm0, 7.2kHz Using filter:BPF
		6.5	-	-		Input signal:0dBm0, 7.56kHz Using filter:BPF
Transmit noise level	VNTX	-	-	-73	dBFS	COMOUT input in MICIN Using filter:A-Weight
Receive noise level	VNRX	-	-	-85	dBV	PCMIN="L" fixation Using filter:A-Weight

◆Transmit / Receive analog block

Application Circuit (Figure 33), Ta=25℃, AVDD=3.3V, PLLVDD=3.3V, REGON="H", f=1kHz unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Minimum load resistance	RALRT	600	-	-	Ω	Measurement Pin:LINEOUT
Maximum load capacitance	CALRX	-	-	50	pF	Measurement Pin:LINEOUT
Maximum output level	VAORX	1.9	-	-	Vpp	Measurement Pin:LINEOUT
Volume gain setting range MIC1/MIC2	GTVOL	-20	-	30	dB	Measurement Path: MICIN → PCMOUT
Volume step width MIC1/MIC2	GTSTEP	-	2	-	dB	Measurement Path: MICIN → PCMOUT
Volume gain setting range LINEOUT	GRVOL	-25	-	16	dB	Measurement Path: MICIN → LINEOUT
Volume step width LINEOUT	GRSTEP	-	1	-	dB	Measurement Path: MICIN → LINEOUT

◆Reference

Application Circuit (Figure 33), Ta=25℃, AVDD=3.3V, PLLVDD=3.3V, REGON="H" unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Output voltage	VAG	0.45* AVDD	0.5* AVDD	0.55* AVDD	V	Measurement Pin: COMIN, COMOUT
Rise time *4	TAG	-	-	15	ms	RSTB="L"→"H" 90%attainment time COMIN=1μF, COMOUT=1μF

*4 Rise time is affected to power supply, COMIN capacitance, and process. Please, have sufficient margin when value determination.

◆Microphone BIAS (MICBIAS)

Application Circuit (Figure 33), Ta=25℃, AVDD=3.3V, PLLVDD=3.3V, REGON="H", f=1kHz unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
MICBIAS output voltage	VMICB	2.2	2.5	2.8	V	Measurement Pin: MICBIAS1, MICBIAS2 Iload=1mA
MICBIAS output noise	VNOMICB	-	-95	-80	dBV	Measurement Pin: MICBIAS1, MICBIAS2 RL=2kΩ Using filter:A-Weight
PSRR	PSRMICB	40	-	-	dB	Measurement Pin: MICBIAS1, MICBIAS2 Using filter:1kHz BPF GMIC=0dB, Vrippl=100mVpp

Typical Performance Curve(s)

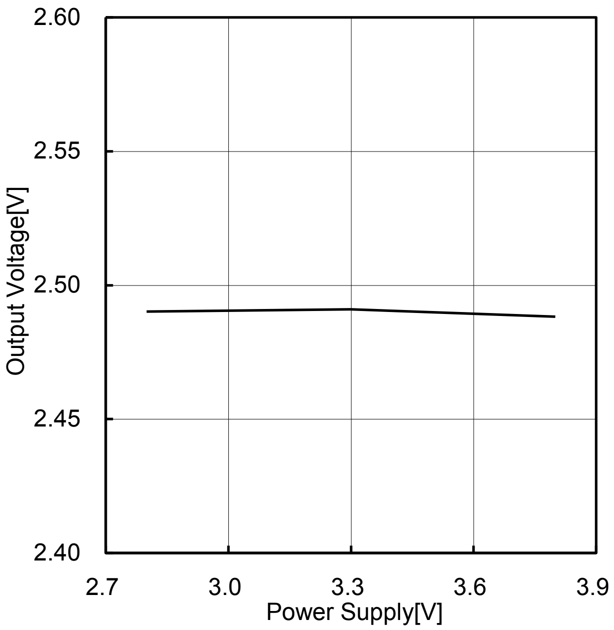


Figure 4. Output Voltage vs Power Supply
(MICBIAS1 output voltage)

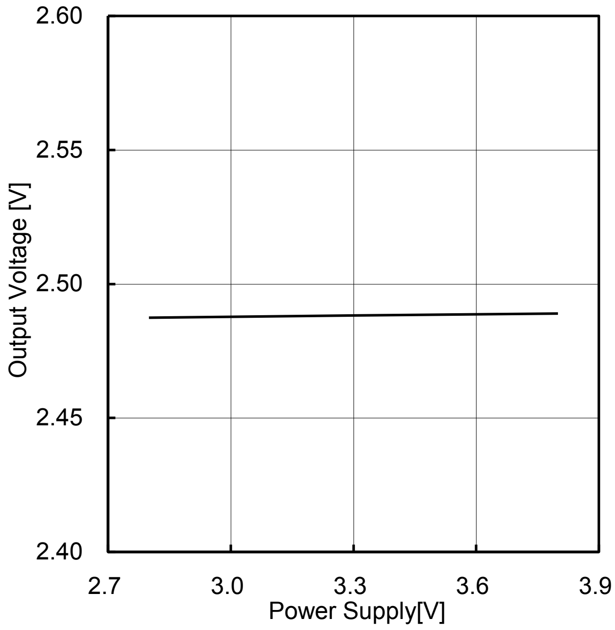


Figure 5. Output Voltage vs Power Supply
(MICBIAS2 output voltage)

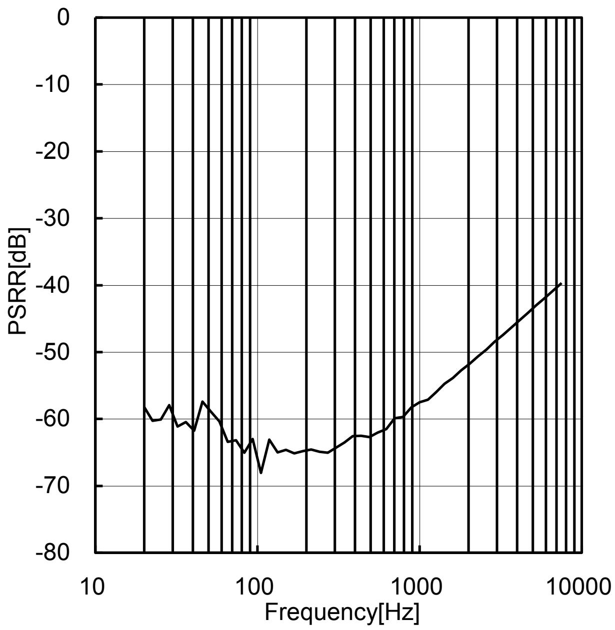


Figure 6. PSRR vs Frequency
(MICBIAS1PSRR)

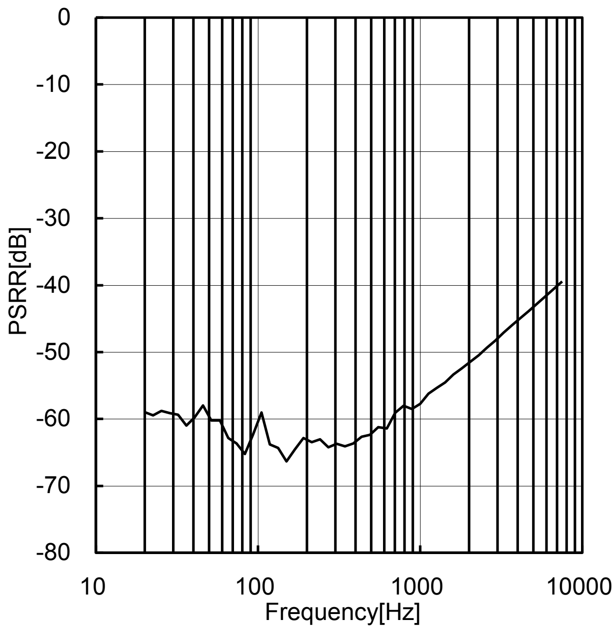


Figure 7. PSRR vs Frequency
(MICBIAS2PSRR)

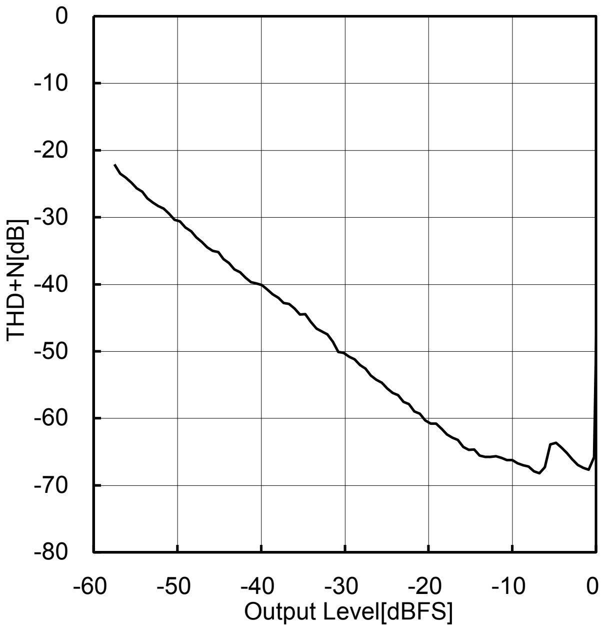


Figure 8. THD+N vs Output Level
(MIC1 signal-to-distortion ratio + Noise)

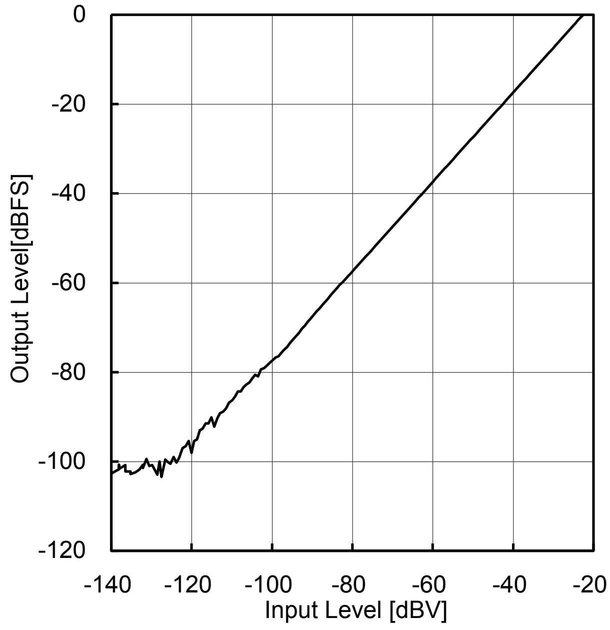


Figure 9. Output Level vs Input Level
(MIC1 signal level)

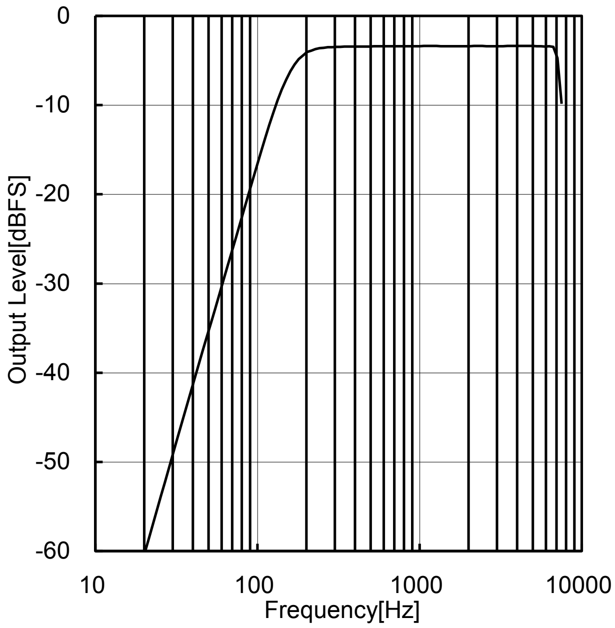


Figure 10. Output Level vs Frequency
(MIC1 gain loss relative to frequency)

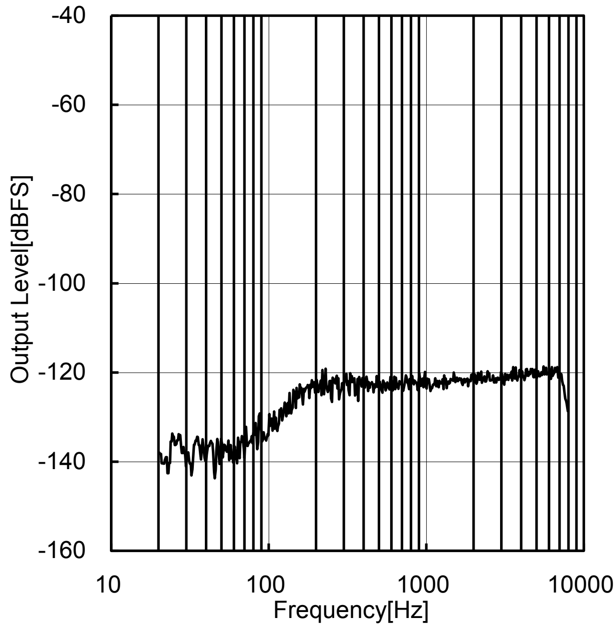


Figure 11. Output Level vs Frequency
(MIC1 noise level)

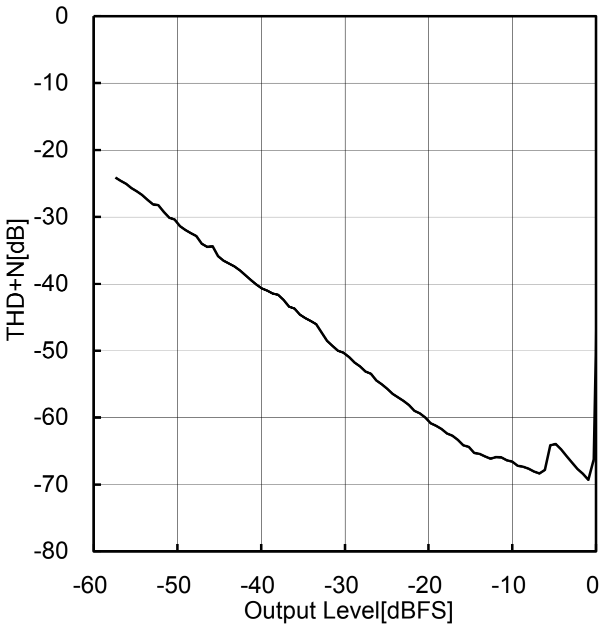


Figure 12. THD+N vs Output Level
(MIC2 signal-to-distortion ratio + Noise)

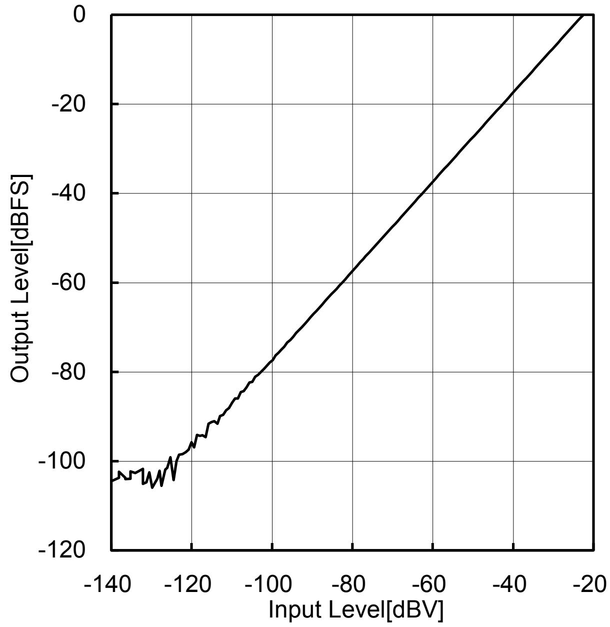


Figure 13. Output Level vs Input Level
(MIC2 signal level)

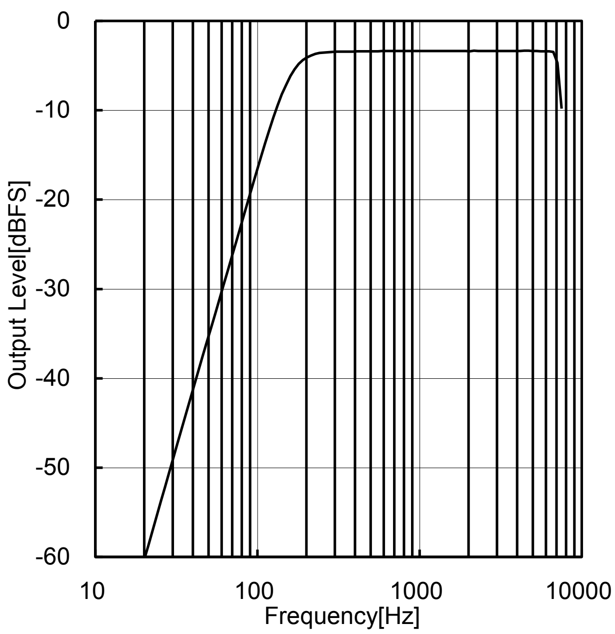


Figure 14. Output Level vs Frequency
(MIC2 gain loss relative to frequency)

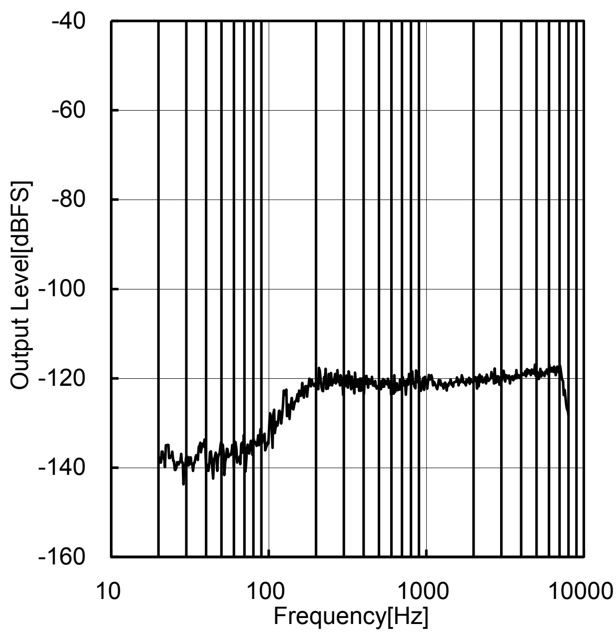


Figure 15. Output Level vs Frequency
(MIC2 noise level)

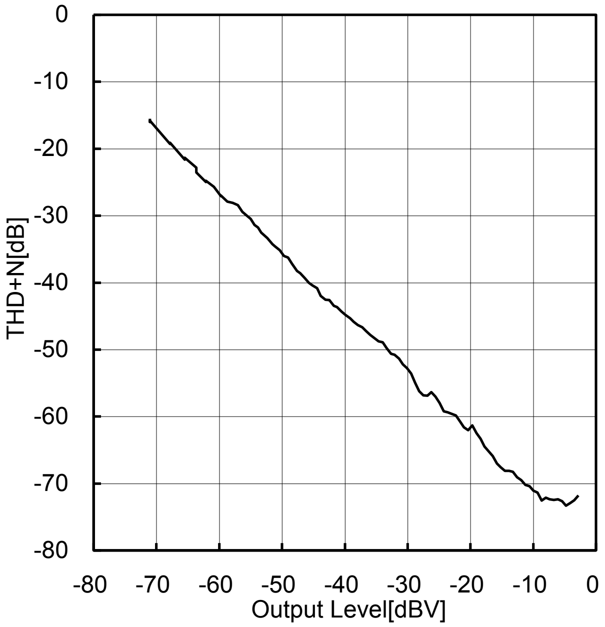


Figure 16. THD+N vs Output Level
(LINEOUT signal-to-distortion ratio + Noise)

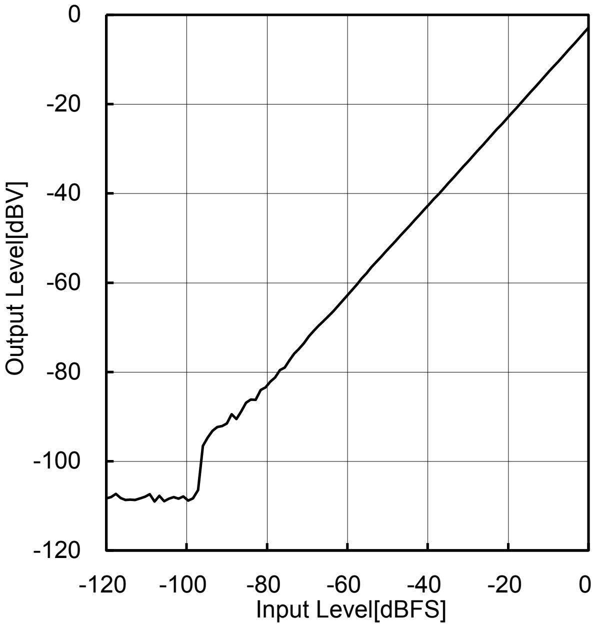


Figure 17. Output Level vs Input Level
(LINEOUT signal level)

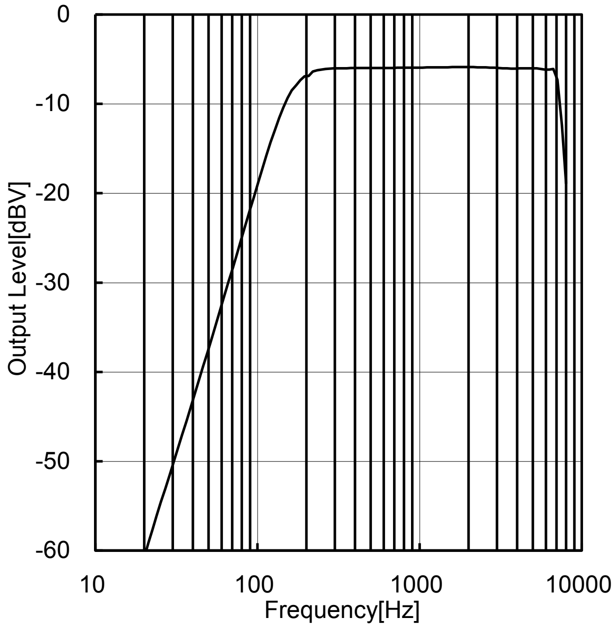


Figure 18. Output Level vs Frequency
(LINEOUT gain loss relative to frequency)

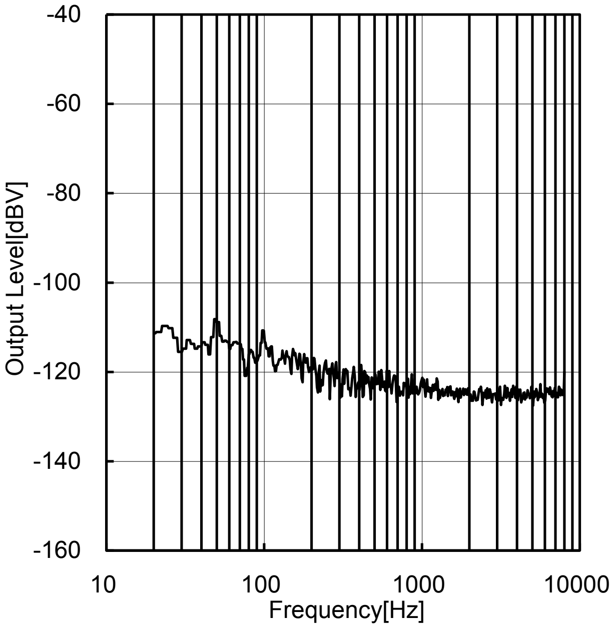


Figure 19. Output Level vs Frequency
(LINEOUT noise level)

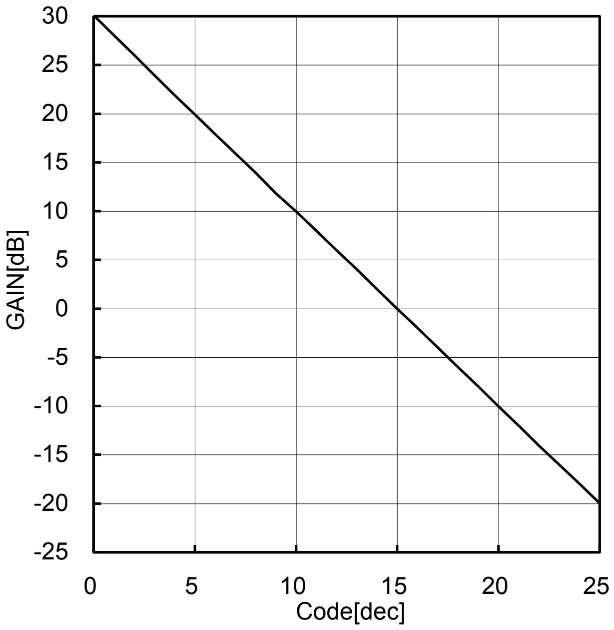


Figure 20. GAIN vs Code
(MIC1 Volume)

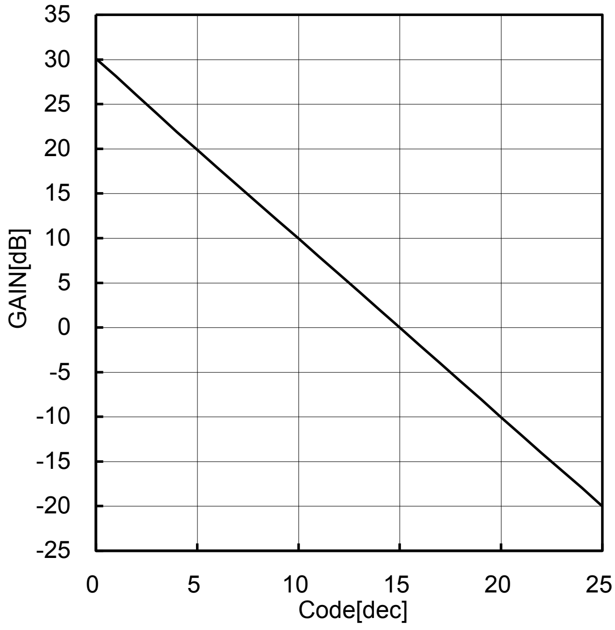


Figure 21. GAIN vs Code
(MIC2 Volume)

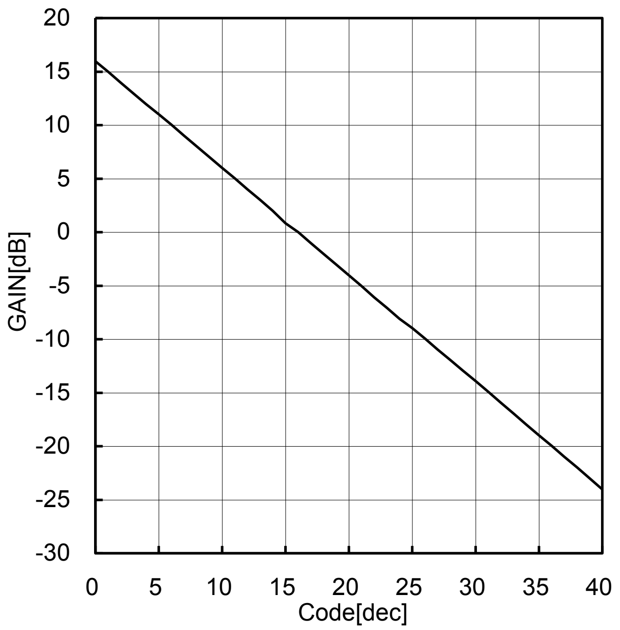


Figure 22. GAIN vs Code
(LINEOUT Volume)

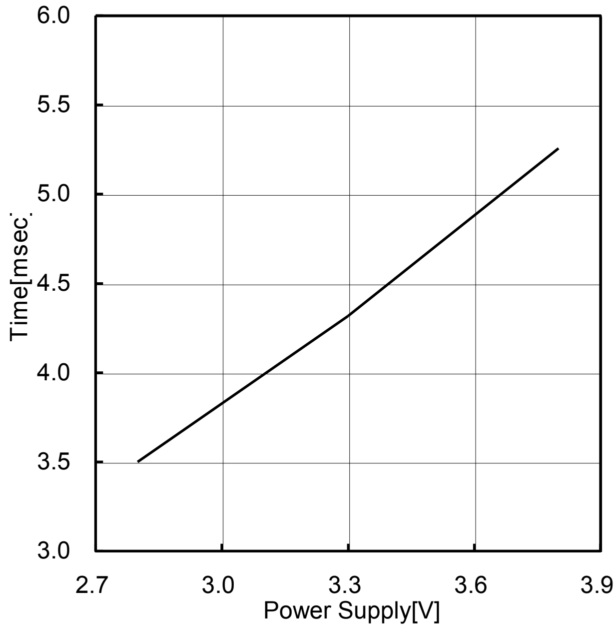


Figure 23. Time vs Power Supply
(PLL pull-in time)

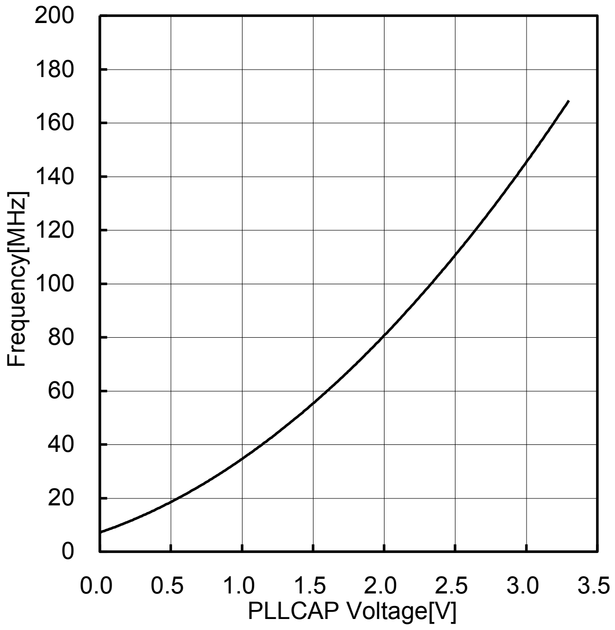


Figure 24. Frequency vs PLL CAP Voltage
(V-F characteristic)

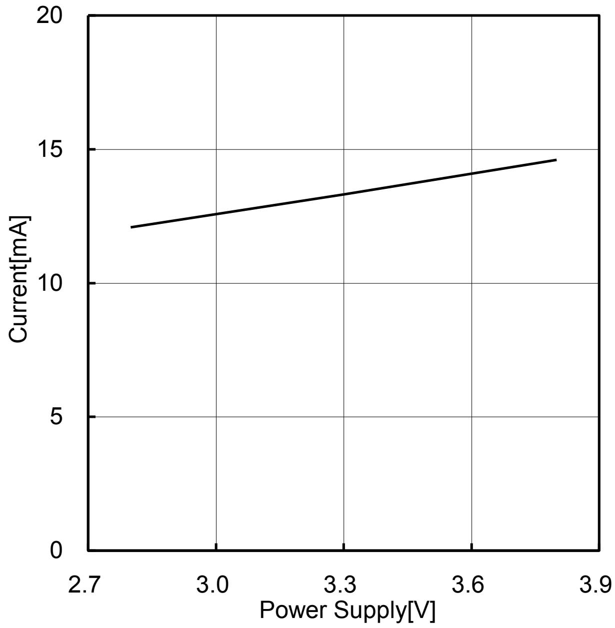


Figure 25. Current vs Power Supply
(Operating Current)

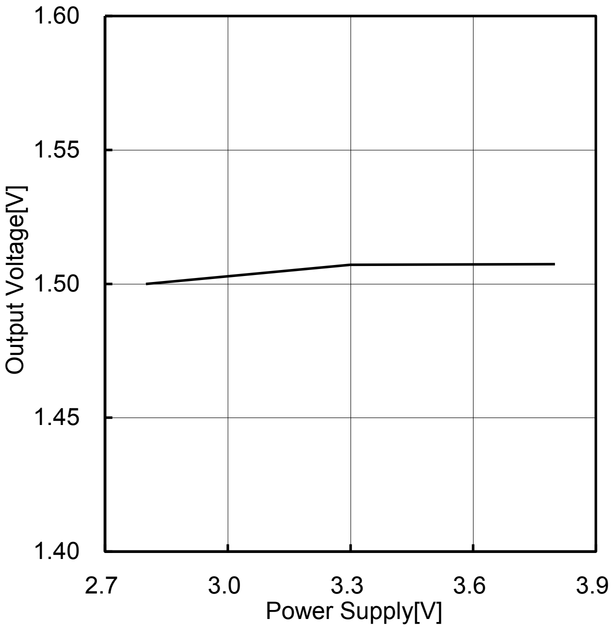


Figure 26. Output Voltage vs Power Supply
(Regulator output voltage)

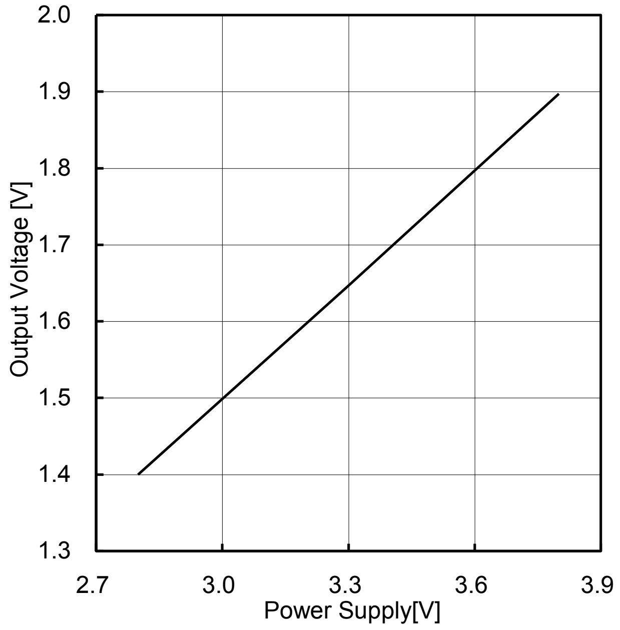


Figure 27. Output Voltage vs Power Supply
(COMOUT output voltage)

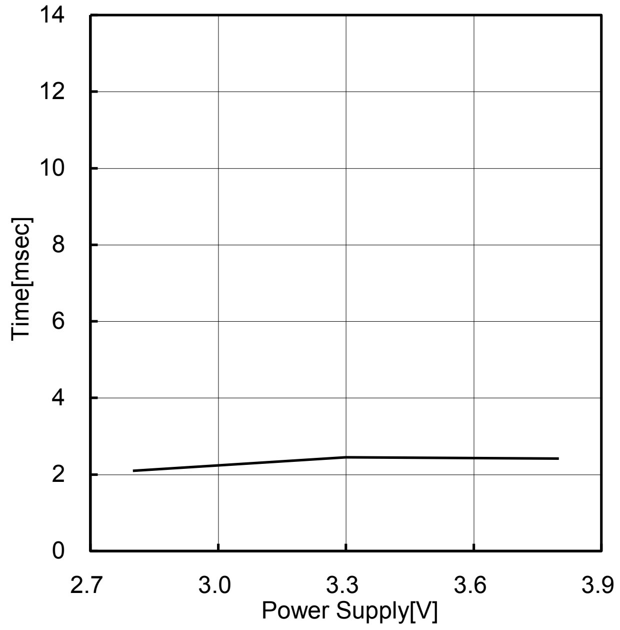


Figure 28. Time vs Power Supply
(COMOUT rise time)

Digital interface characteristic

1. PCM interface

Parameter	Symbol	Conditions	Limits			Unit
			Min	Typ	Min	
Clock frequency (PCMCLK)	f_{PCLK}	PCMFS=16kHz	256		2048	kHz
Clock duty	f_{DU}	-	40	-	60	%
Frame synchronization signal frequency(PMCFS)	f_{FS}	-	15.992	16	16.008	kHz
Digital input rise time	t_{IR}	DVDDIO*0.3→DVDDIO*0.7 PCKCLK, PCMFS, PCMIN	-	-	40	ns
Digital input fall time	t_{IF}	DVDDIO*0.7→DVDDIO*0.3 PCMCLK, PCMFS, PCMIN	-	-	40	ns
Transmit / Receive synchronization signal timing	t_{RS}	PCMIN setup time (vs. PCMCLK↓)	20	-	-	ns
	t_{RH}	PCMIN hold time (vs. PCMCLK↓)	0	-	-	ns
	t_{SR}	PCMCLK↓ vs. PCMFS↑	20	-	-	ns
	t_{SS}	PCMFS setup time (vs. PCMCLK↓)	20	-	-	ns
	t_{SH}	PCMFS hold time (vs. PCMCLK↓)	20	-	-	ns
	t_{SO}	PCMOUT determined time (vs. PCMFS↑)	-	-	30	ns
	t_{DO}	PCMOUT determined time (vs. PCMCLK↑)	-	-	30	ns

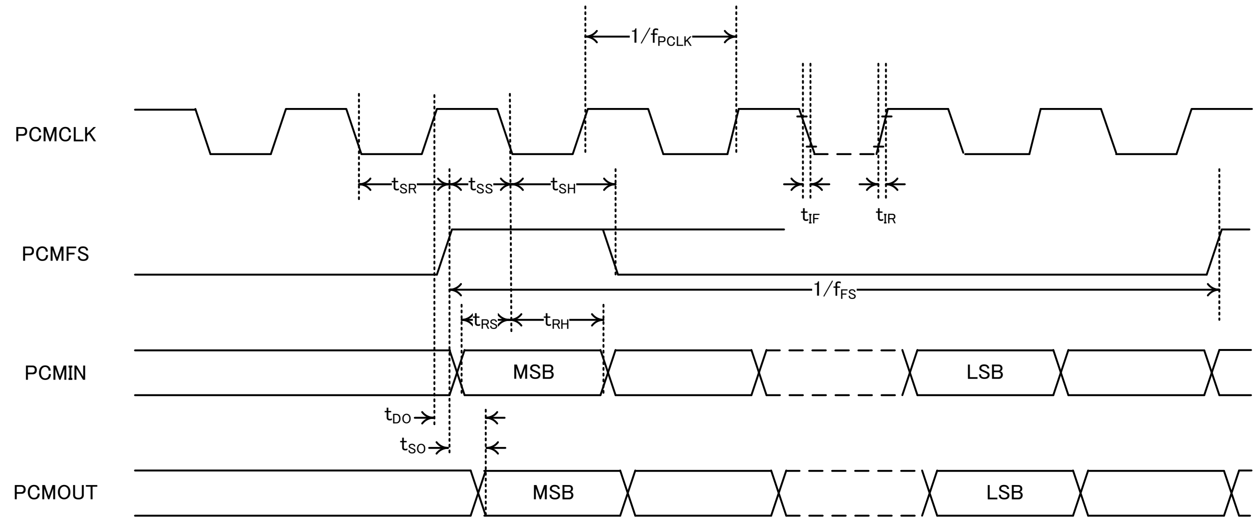


Figure 29 Timing of PCM long frame interface

* The accuracy of the clock

Make sure to use below 100ppm accuracy for PCM interface clock PCMCLK and master clock MCLK. In case more than 100ppm oscillate is in use, output signal may not work properly.

2. 2-wire host interface (Slave)

Parameter	Symbol	Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
”H” level of SCL	t_{HI}	4.0	-	0.6	-	μs
”L” level of SCL	t_{LO}	4.7	-	1.2	-	μs
Setup time of repeat start condition	t_{SUSTA}	4.7	-	0.6	-	μs
Hold time of repeat start condition	t_{HDSTA}	4.0	-	0.6	-	μs
Data setup time	t_{SUDAT}	0.25	-	0.1	-	μs
Data hold time	t_{HDDAT}	0	3.5	0	0.9	μs
Setup time of Stop condition	t_{SUSTP}	4.0	-	0.6	-	μs
Bus release time of between stop condition and start condition	t_{BUF}	4.7	-	1.2	-	μs

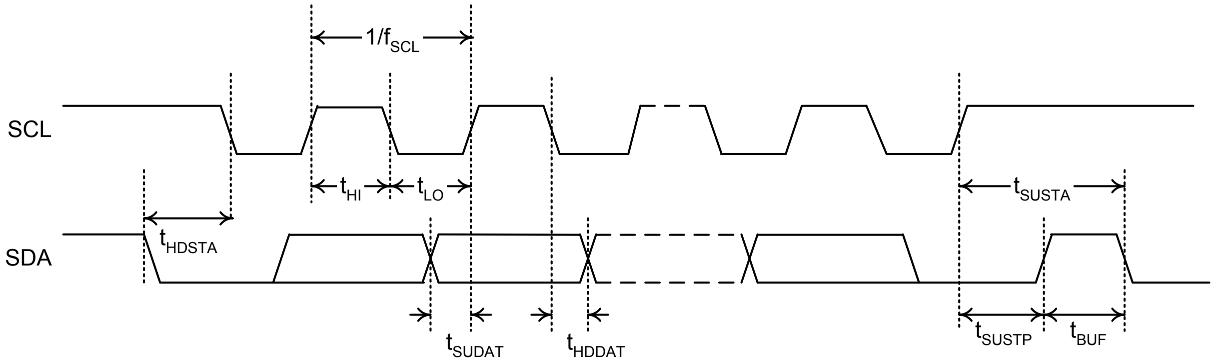


Figure 30 Timing of 2-wire host interface

3. EEPROM (SPI master) interface

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
SPICLK clock frequency	f_{CK}	-	-	3.25	MHz
"H" time of SPICLK clock	t_{CK_HI}	100	-	-	ns
"L" time of SPICLK clock	t_{CK_LO}	100	-	-	ns
"H" time of SPICSB chip select	t_{CS_HI}	100	-	-	ns
Setup time of SPICSB chip select	t_{CS_SU}	100	-	-	ns
Enable hold time of SPICSB chip select	t_{CS_HD}	100	-	-	ns
Data output delay time of SPIDO	t_{DO_SU}	-	-	80	ns
Output hold time of SPIDO	t_{DO_HD}	0	-	-	ns
Setup time of SPIDI	t_{DI_SU}	20	-	-	ns
Hold time of SPIDI	t_{DI_SO}	40	-	-	ns

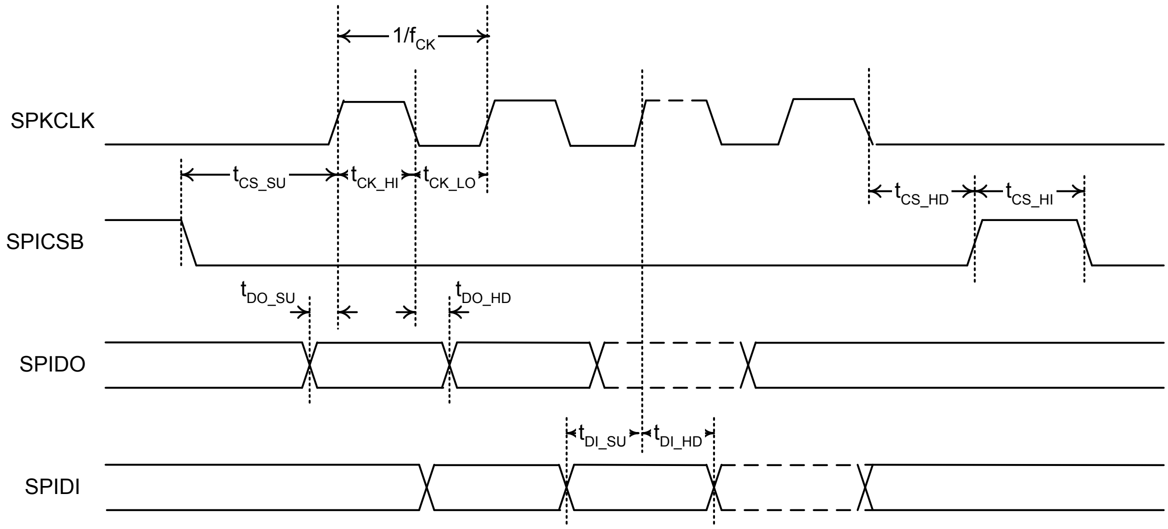


Figure 31 Timing of EEPROM (SPI) interface

Timing Chart

Turn on AVDD and DVDDIO simultaneously and then turn on DVDD1 or DVDD2. Please note that DVDD1 can be supplied by internal voltage regulator. Please set REGON pin ="H" to use internal regulator.
It is necessary to input clock on MCLK, before reset (RSTB) is released.
Initial values of register are automatically downloaded from EEPROM and register is updated, after reset (RSTB) release. This processing is skipped when EEPROM is not connected.
Then, using via 2-wire host interface, please carry out required register setup.

2-wire host interface is compatible with I^2C bus specification, but is not 5V tolerant.

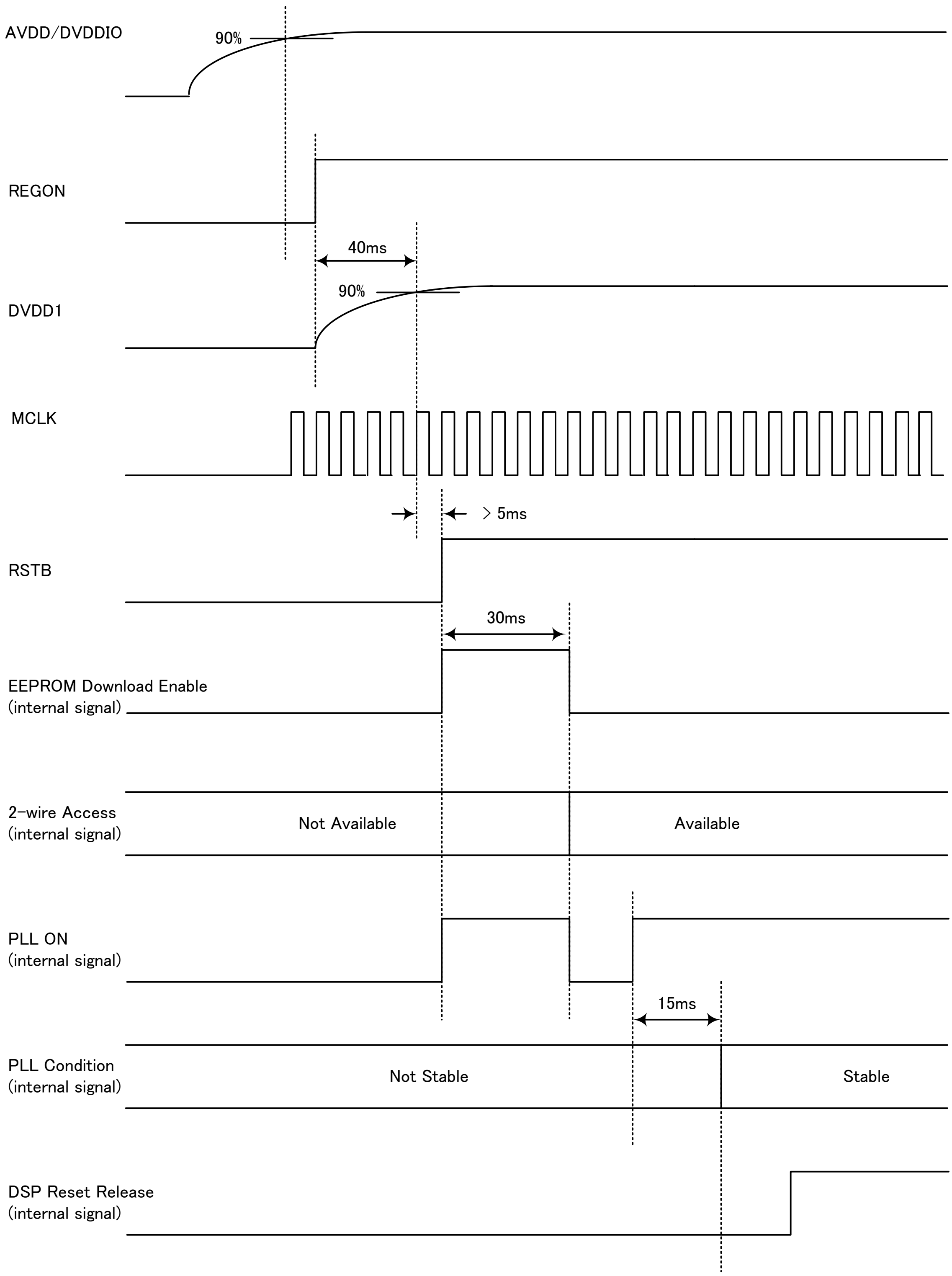


Figure 32 Timing Chart

Application Example

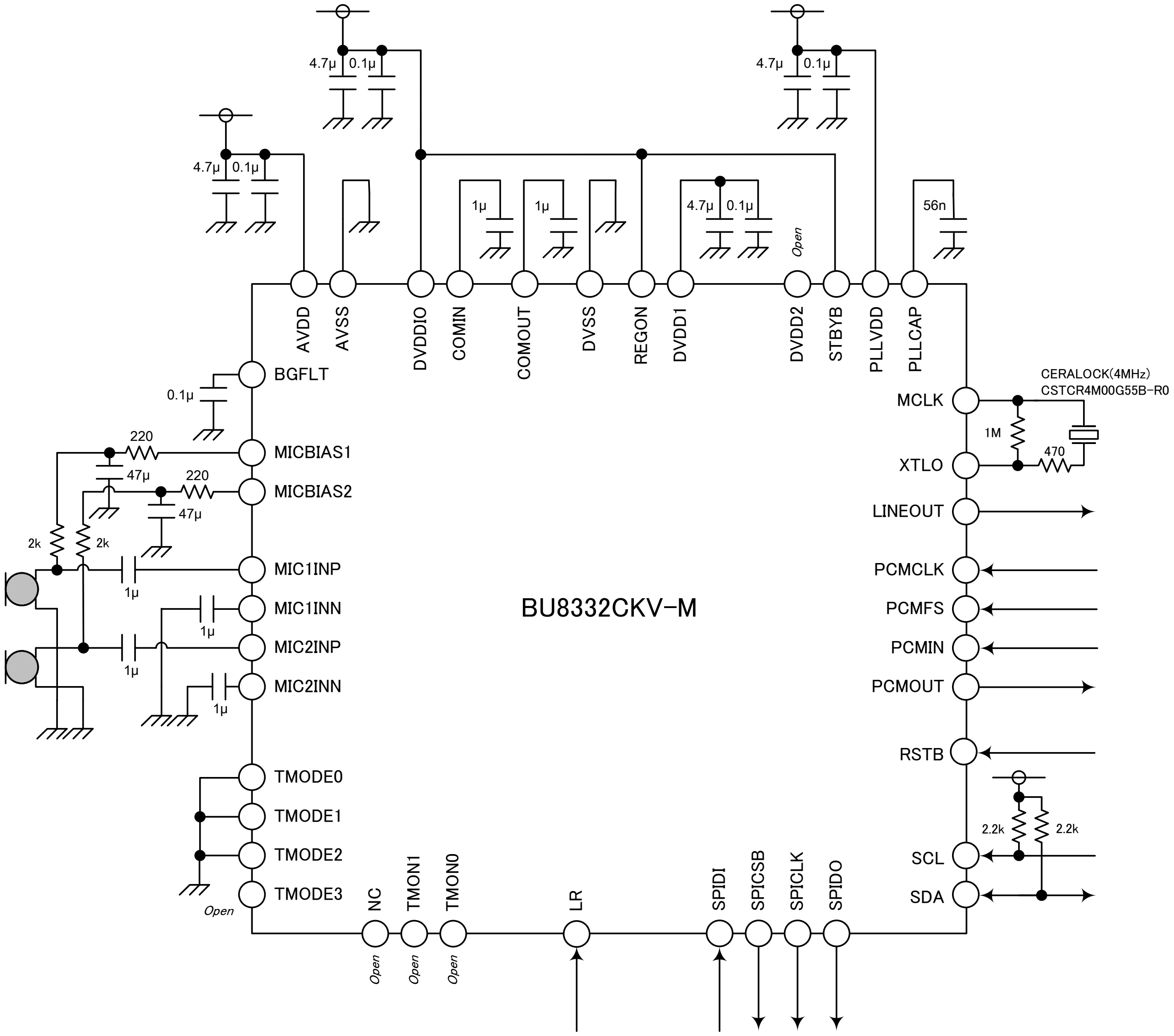


Figure 33 Application Circuit

Application circuit above shows line output. Please follow Timing Chart described earlier. DVDDIO should be selected depending on I/O interface voltage level requirement, without exceeding the maximum specification. PCM output may be used if required. An EEPROM may be connected to SPI BUS pins to load register values automatically upon reset.

Circuit constant should be selected one that tolerance is within 10%. Resistor for microphone bias should be decided by actual microphone specification. Also circuit elements around oscillator circuit should be estimated based on matching evaluation for each actual board.

I/O Equivalence Circuits

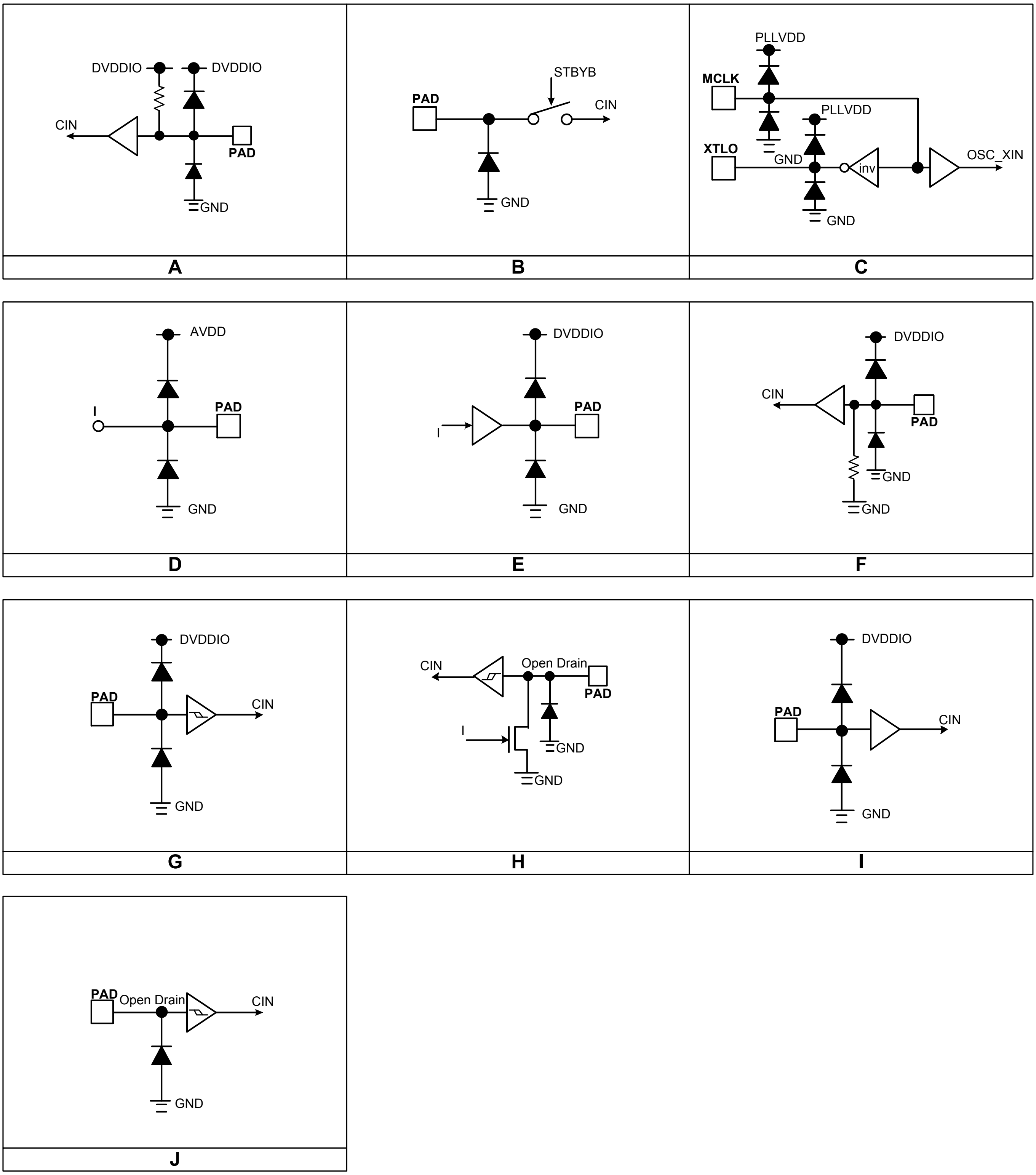


Figure 34 I/O equivalent circuits

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. **Ceramic Capacitor**
    When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

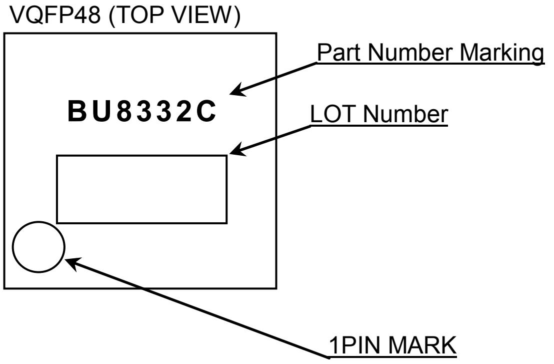
B	U	8	3	3	2	C	K	V	-	ME 2

Parts Number

Package
KV: VQFP48

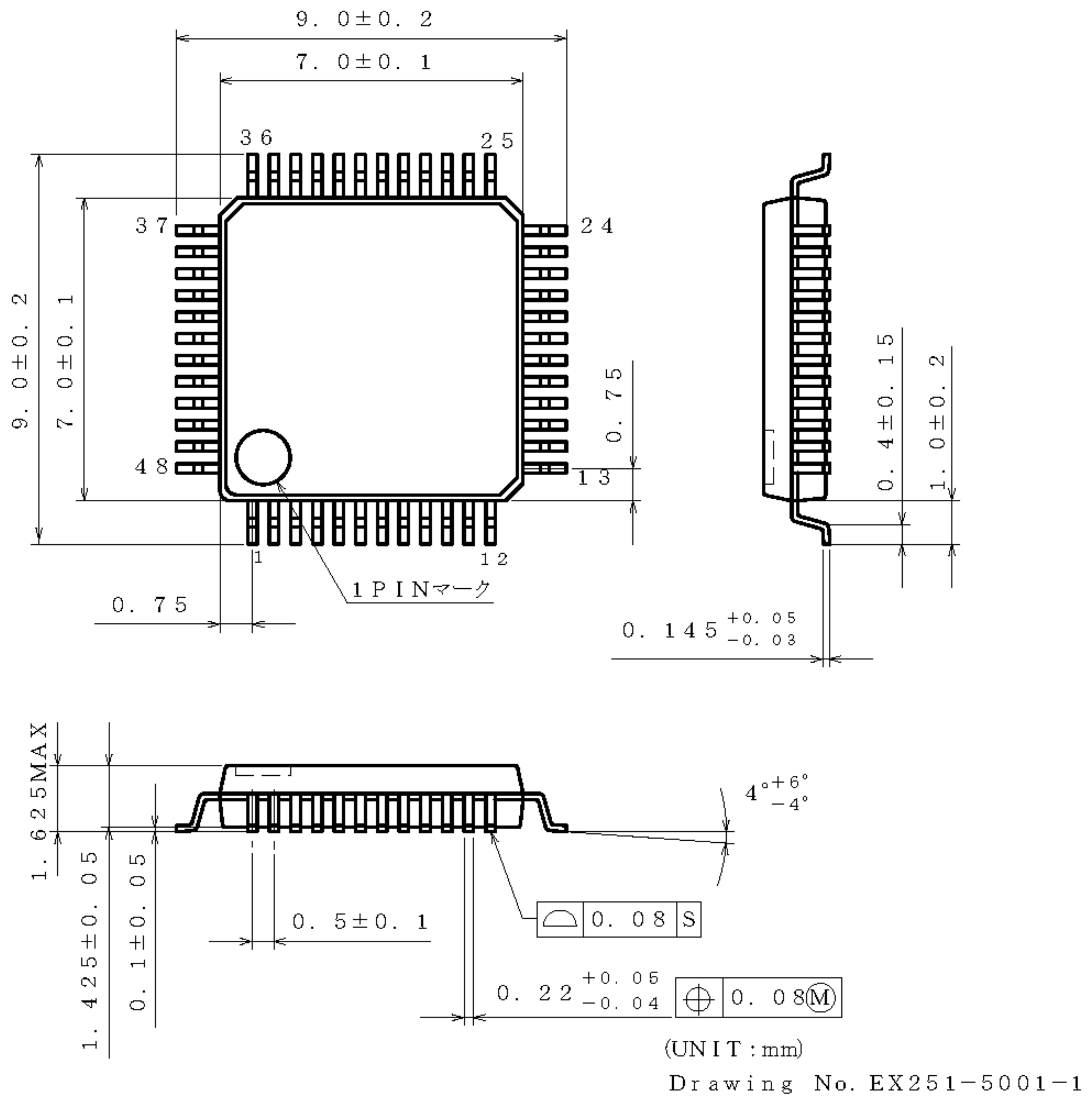
Product Rank
M:for Automotive
Packaging Specification
E2: Embossed tape and reel

Marking Diagram



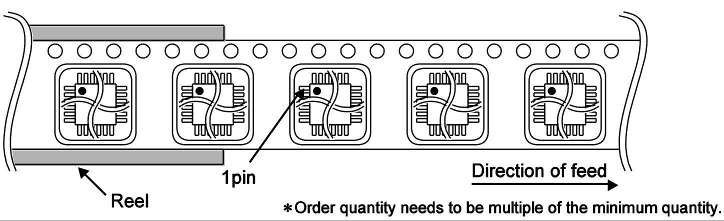
Physical Dimension, Tape and Reel Information

Package Name	VQFP48



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision history

Date	Revision	Changes
2014.10.10	001	New Release
2014.10.31	002	Delete ALC, Noise Suppression, LINE IN

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

   (Note1) Medical Equipment Classification of the Specific Applications

<table>
<tr><th>JAPAN</th><th>USA</th><th>EU</th><th>CHINA</th></tr>
<tr><td>CLASSⅢ</td><td rowspan="2">CLASSⅢ</td><td>CLASSⅡb</td><td rowspan="2">CLASSⅢ</td></tr>
<tr><td>CLASSⅣ</td><td>CLASSⅢ</td></tr>
</table>

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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