

N-channel 600 V, 7 A - IPAK Very fast PowerMESH™ IGBT

Datasheet - production data

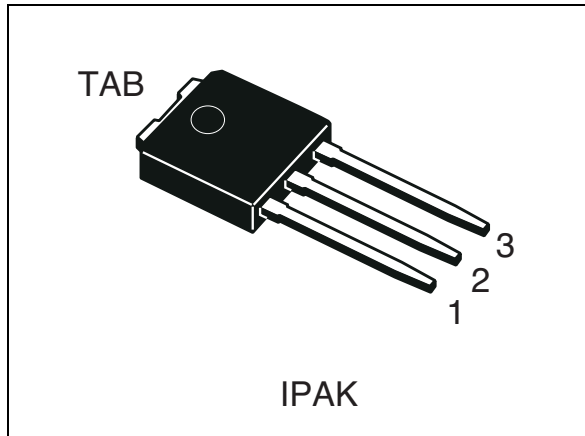
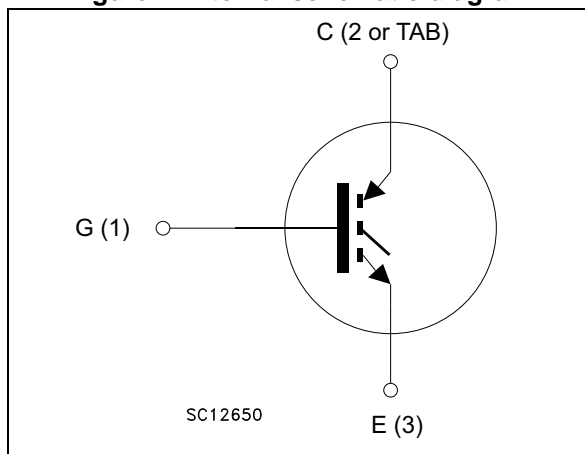


Figure 1. Internal schematic diagram



Features

Type	V_{CES}	$V_{CE(sat)}$ max@25°C	I_C @100°C
STGD6NC60H	600V	<2.5V	7A

- Low on voltage drop (V_{cesat})
- Low C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- High frequency operation

Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix H identifies a family optimized for high frequency application in order to achieve very high switching performances (reduced t_{fall}) maintaining a low voltage drop.

Applications

- High frequency inverters
- SMPS and PFC in both hard switch and resonant topologies
- Motor drivers

Table 1. Device summary

Part number	Marking	Package	Packaging
STGD6NC60H-1	GD6NC60H	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GS} = 0$)	600	V
$I_C^{(1)}$	Collector current (continuous) at $T_C = 25^\circ\text{C}$	15	A
$I_C^{(1)}$	Collector current (continuous) at $T_C = 100^\circ\text{C}$	7	A
$I_{CM}^{(2)}$	Collector current (pulsed)	21	A
V_{GE}	Gate-emitter voltage	± 20	V
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	62.5	W
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature		
T_l	Maximum lead temperature for soldering purpose (for 10sec. 1.6 mm from case)	300	$^\circ\text{C}$

1. Calculated according to the iterative formula.:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C \cdot I_C)}$$

2. Pulse width limited by max junction temperature

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	2	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal resistance junction-ambient max	100	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{mA}, V_{GE} = 0$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{V}, I_C = 3\text{A}$ $V_{GE} = 15\text{V}, I_C = 3\text{A}, T_C = 125^{\circ}C$		1.9 1.7	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}, I_C = 250\ \mu\text{A}$	3.75		5.75	V
I_{CES}	Collector cut-off current ($V_{GE} = 0$)	$V_{CE} = 600\text{V}$ $V_{CE} = 600\text{V}, T_C = 125^{\circ}C$			10 1	μA mA
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20\text{V}, V_{CE} = 0$			± 100	nA
g_{fs}	Forward transconductance	$V_{CE} = 15\text{V}, I_C = 3\text{A}$		3		S

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{V}, f = 1\text{MHz},$ $V_{GE} = 0$	-	205	-	pF
C_{oes}	Output capacitance		-	32	-	pF
C_{res}	Reverse transfer capacitance		-	5.5	-	pF
Q_g	Total gate charge	$V_{CE} = 390\text{V}, I_C = 3\text{A},$ $V_{GE} = 15\text{V},$ (see Figure 17)	-	13.6	-	nC
Q_{ge}	Gate-emitter charge			3.4		nC
Q_{gc}	Gate-collector charge			5.1		nC
I_{CL}	Turn-off SOA minimum current	$V_{clamp} = 390\text{V}, T_j = 150^{\circ}C,$ $R_G = 10\ \Omega, V_{GE} = 15\text{V}$	-	19	-	A

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390V, I_C = 3A$ $R_G = 10\Omega, V_{GE} = 15V,$ (see Figure 18)	-	12	-	ns
t_r	Current rise time		-	5	-	ns
$(di/dt)_{on}$	Turn-on current slope		-	612	-	A/ μs
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390V, I_C = 3A$ $R_G = 10\Omega, V_{GE} = 15V,$ $T_j = 125^\circ C$ (see Figure 18)	-	13	-	ns
t_r	Current rise time		-	4.3	-	ns
$(di/dt)_{on}$	Turn-on current slope		-	560	-	A/ μs
$t_{r(Voff)}$	Off voltage rise time	$V_{CC} = 390V, I_C = 3A,$ $R_{GE} = 10\Omega, V_{GE} = 15V$ (see Figure 18)	-	40	-	ns
$t_{d(off)}$	Turn-off delay time		-	76	-	ns
t_f	Current fall time		-	100	-	ns
$t_{r(Voff)}$	Off voltage rise time	$V_{CC} = 390V, I_C = 3A,$ $R_{GE} = 10\Omega, V_{GE} = 15V,$ $T_j = 125^\circ C$ (see Figure 18)	-	60	-	ns
$t_{d(off)}$	Turn-off delay time		-	98	-	ns
t_f	Current fall time		-	124	-	ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390V, I_C = 3A$ $R_G = 10\Omega, V_{GE} = 15V$ (see Figure 18)	-	20	-	μJ
$E_{off}^{(2)}$	Turn-off switching losses		-	68	-	μJ
E_{ts}	Total switching losses		-	88	-	μJ
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390V, I_C = 3A$ $R_G = 10\Omega, V_{GE} = 15V, T_j = 125^\circ C$ (see Figure 18)	-	37	-	μJ
$E_{off}^{(2)}$	Turn-off switching losses		-	93	-	μJ
E_{ts}	Total switching losses		-	130	-	μJ

- E_{on} is the turn-on losses when a typical diode is used in the test circuit in Figure 18. If the IGBT is offered in a package with a co-pak diode, the co-pak diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)
- Turn-off losses include also the tail of the collector current

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

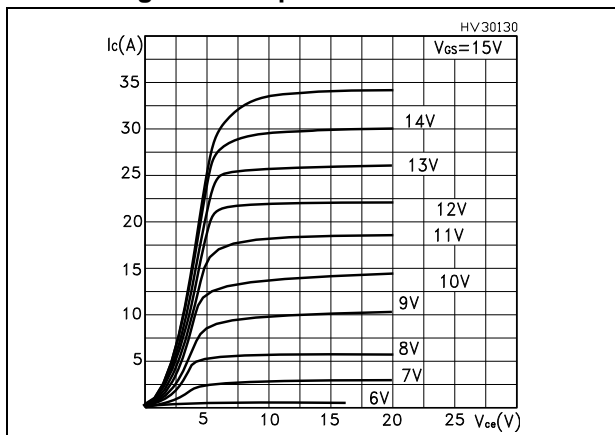


Figure 3. Transfer characteristics

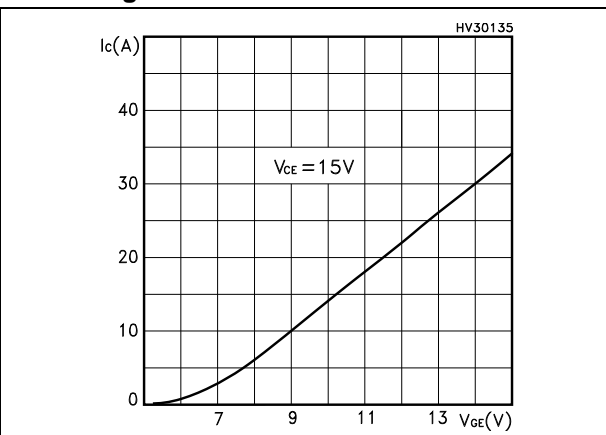


Figure 4. Transconductance

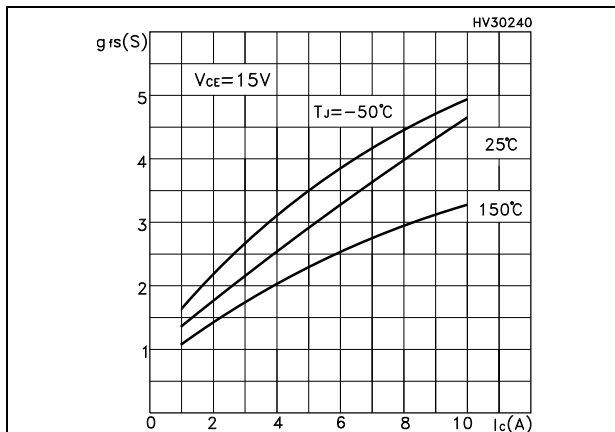


Figure 5. Collector-emitter on voltage vs temperature

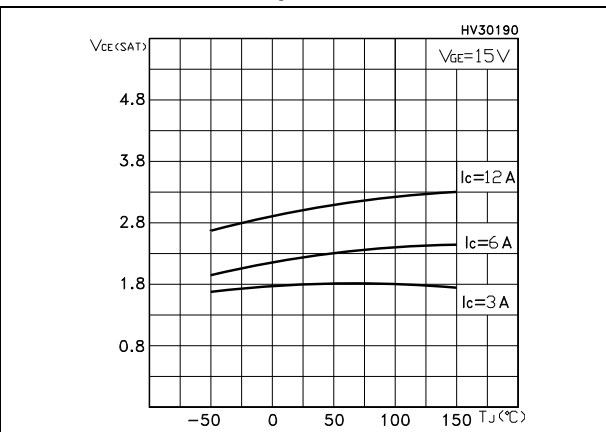


Figure 6. Gate charge vs gate-source voltage

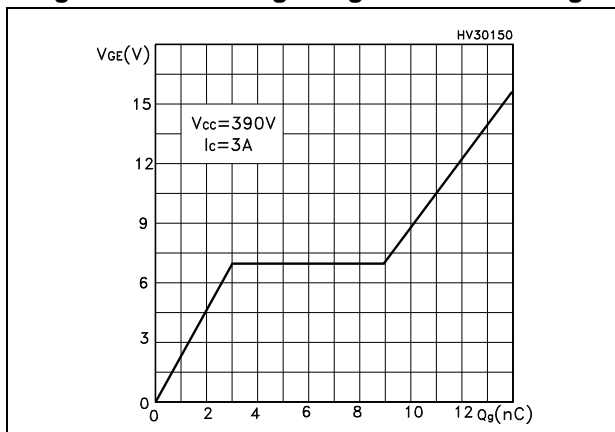


Figure 7. Capacitance variations

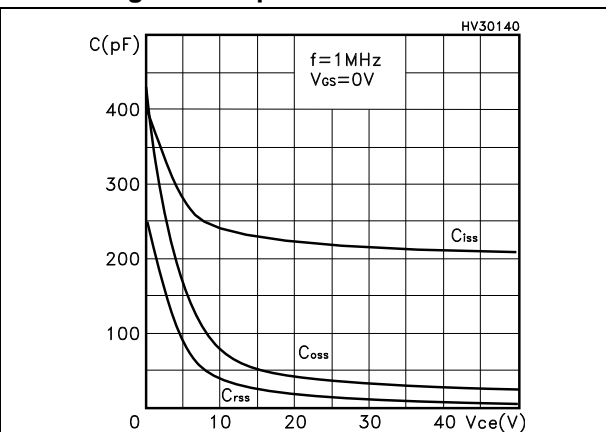


Figure 8. Normalized gate threshold voltage vs temperature

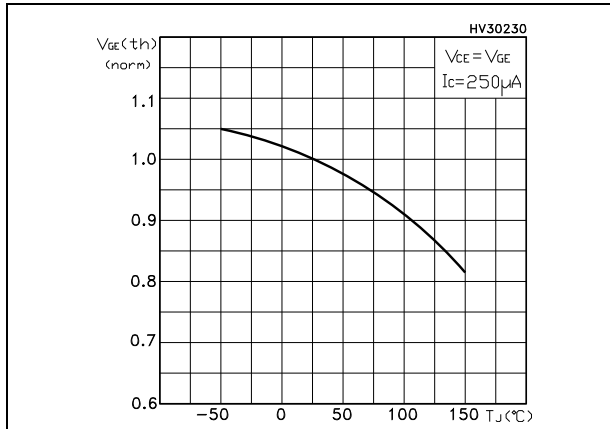


Figure 9. Collector-emitter on voltage vs collector current

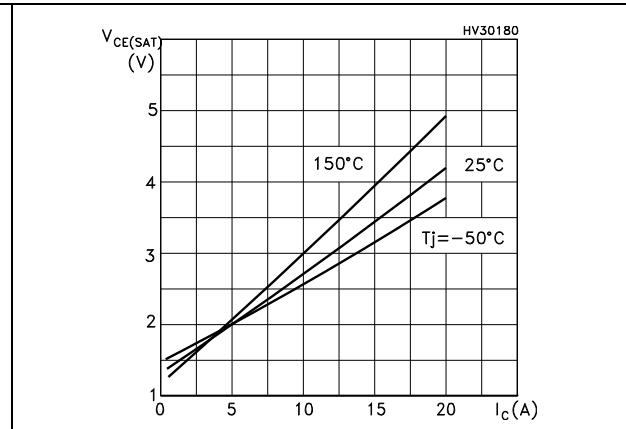


Figure 10. Normalized breakdown voltage vs temperature

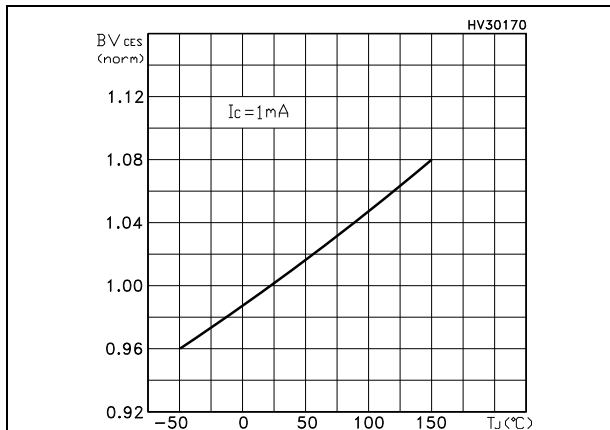


Figure 11. Switching losses vs temperature

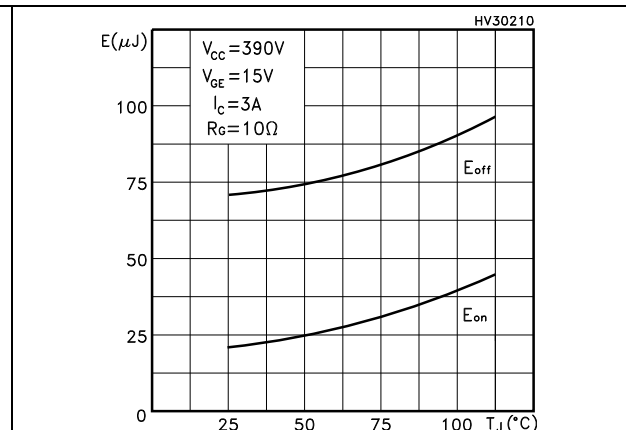


Figure 12. Switching losses vs gate resistance

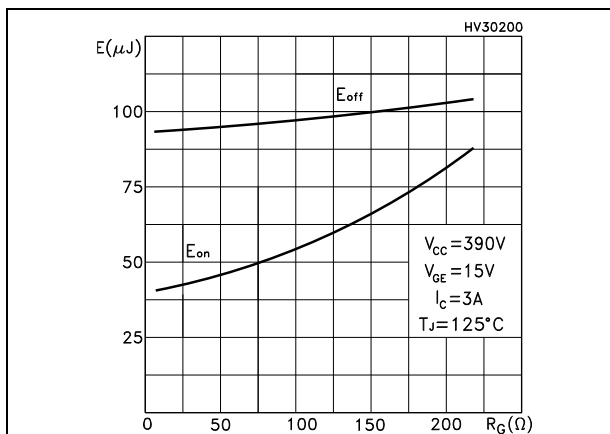


Figure 13. Switching losses vs collector current

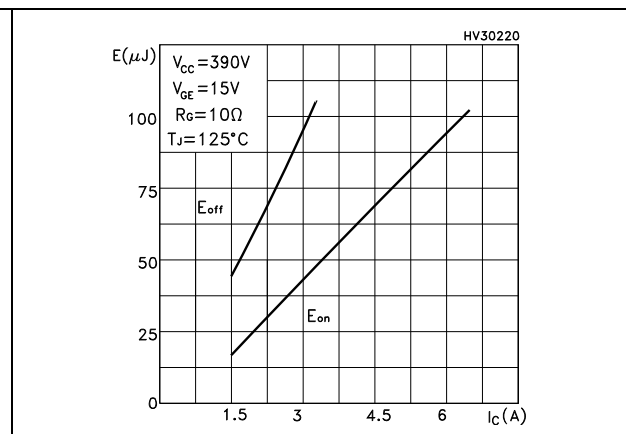


Figure 14. Thermal impedance

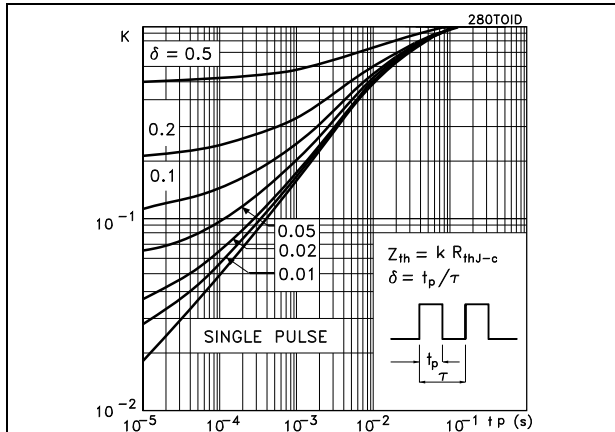
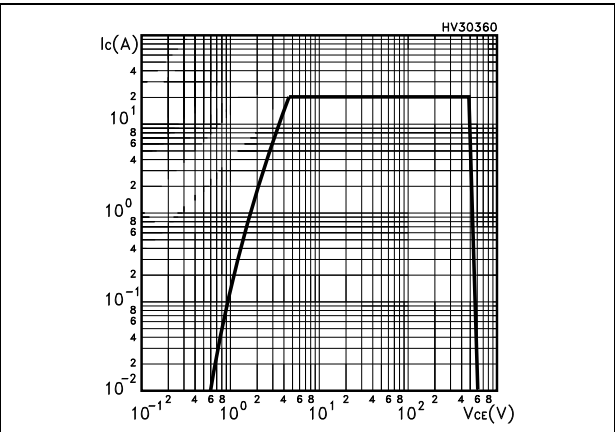


Figure 15. Turn-off SOA



3 Test circuit

Figure 16. Test circuit for inductive load switching

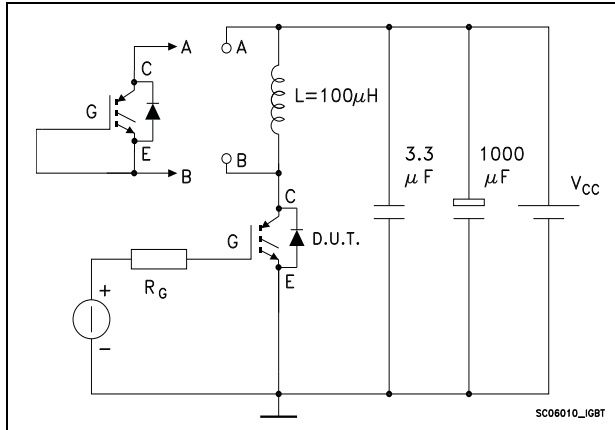


Figure 17. Gate charge test circuit

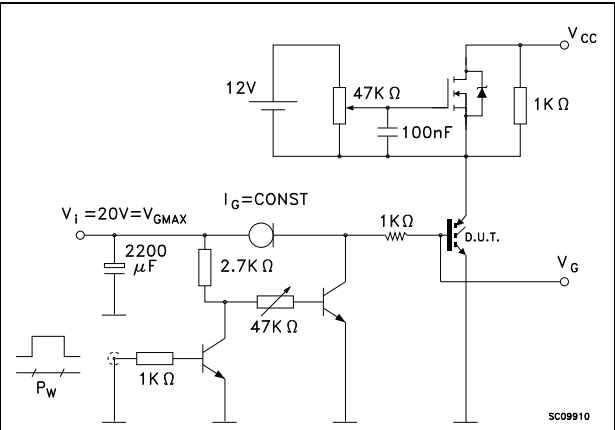


Figure 18. Switching waveform

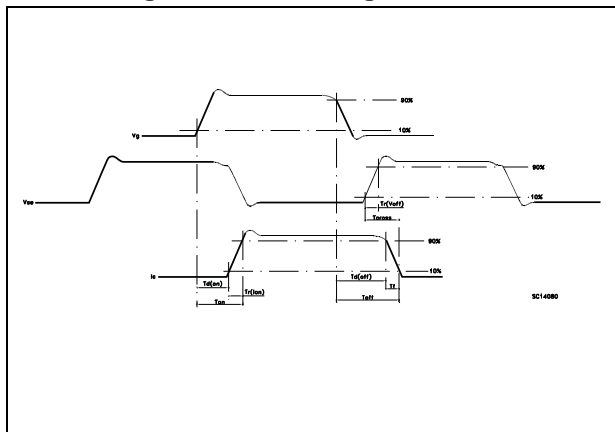
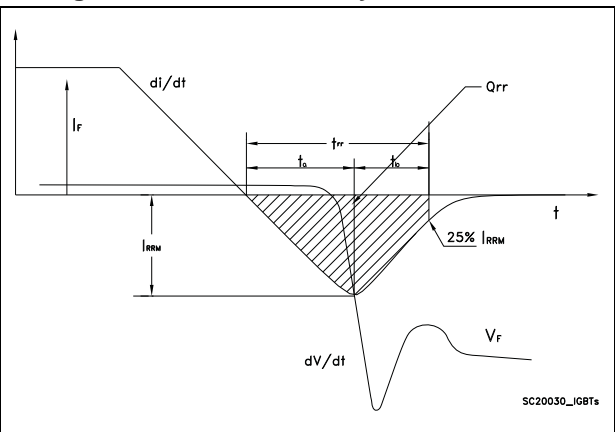


Figure 19. Diode recovery time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 20. IPAK (TO-251) drawing

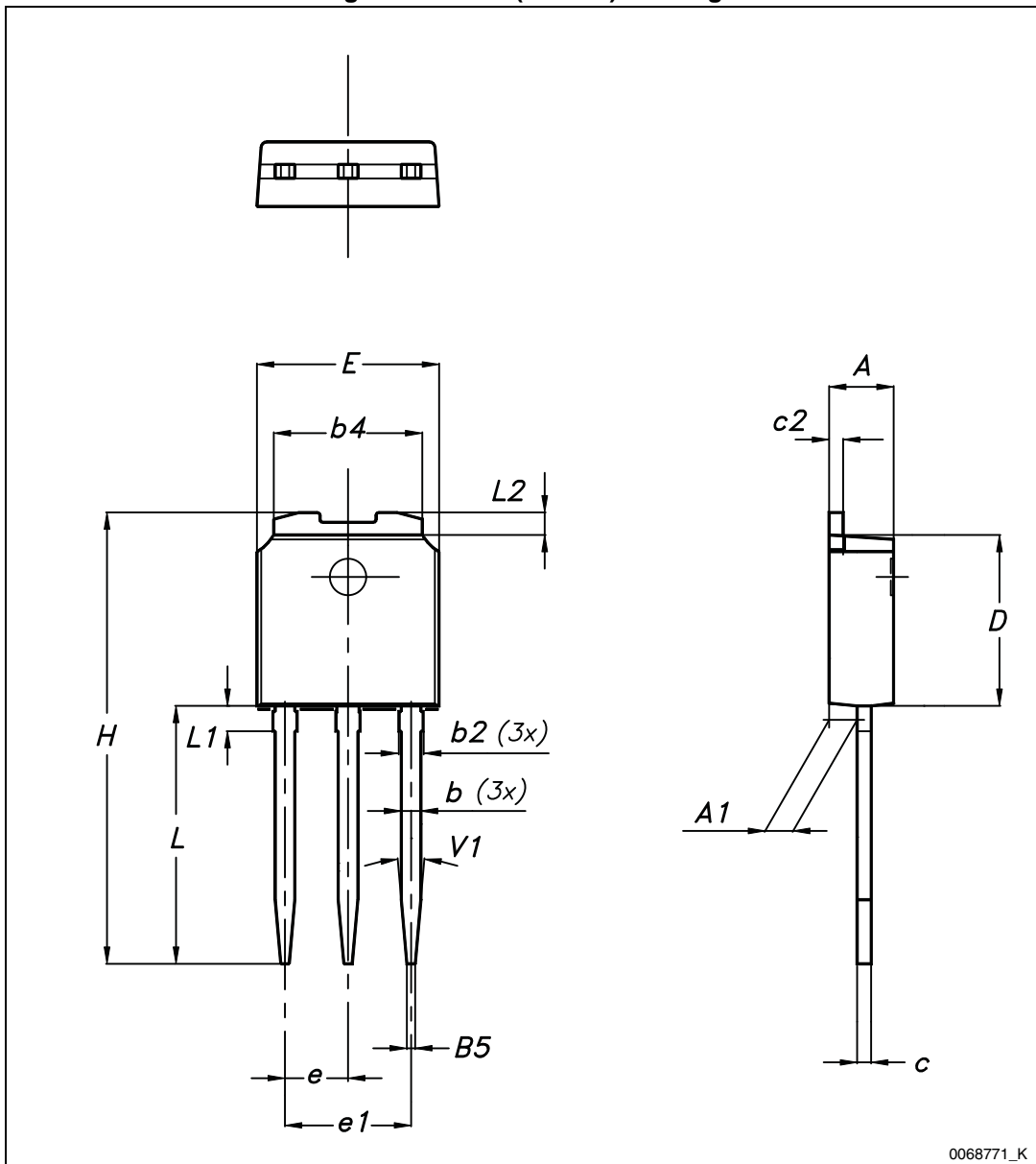


Table 8. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Revision history

Table 9. Revision history

Date	Revision	Changes
08-Apr-2014	1	First release.

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