**Integrated
Circuit
Systems, Inc.**

**ICS9248-169**

# Frequency Generator & Integrated Buffers for Celeron & PII/III™

**Recommended Application:**

440BX/VIA Apollo 133/694X style chipset.

**Output Features:**

- 2 - CPUs @2.5V, up to 166MHz.
- 1 - IOAPIC @ 2.5V
- 13 - SDRAM @ 3.3V
- 6 - PCI @3.3V,
- 1 - 48MHz, @3.3V fixed.
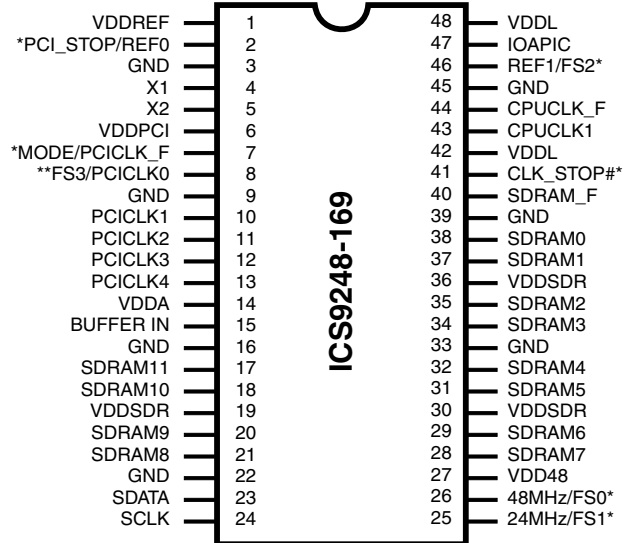- 1 - 24MHz @ 3.3V
- 2 - REF @3.3V, 14.318MHz.

**Features:**

- Up to 166MHz frequency support
- Support power management: PCI, CPU stop and Mode
- Spread spectrum for EMI control (± 0.50%).
- Uses external 14.318MHz crystal

**Skew Specifications:**

- CPU – CPU: <175ps
- SDRAM - SDRAM: <500ps
- PCI – PCI: <500ps
- CPU(early)-PCI: Typ=1.0ns

## Pin Configuration

| | | | | |
|---|---|---|---|---|
| VDDREF | 1 | | 48 | VDDL |
| *PCI_STOP/REF0 | 2 | | 47 | IOAPIC |
| GND | 3 | | 46 | REF1/FS2* |
| X1 | 4 | | 45 | GND |
| X2 | 5 | | 44 | CPUCLK_F |
| VDDPCI | 6 | | 43 | CPUCLK1 |
| *MODE/PCICLK_F | 7 | | 42 | VDDL |
| **FS3/PCICLK0 | 8 | | 41 | CLK_STOP#** |
| GND | 9 | | 40 | SDRAM_F |
| PCICLK1 | 10 | | 39 | GND |
| PCICLK2 | 11 | | 38 | SDRAM0 |
| PCICLK3 | 12 | ICS9248-169 | 37 | SDRAM1 |
| PCICLK4 | 13 | | 36 | VDDSDR |
| VDDA | 14 | | 35 | SDRAM2 |
| BUFFER IN | 15 | | 34 | SDRAM3 |
| GND | 16 | | 33 | GND |
| SDRAM11 | 17 | | 32 | SDRAM4 |
| SDRAM10 | 18 | | 31 | SDRAM5 |
| VDDSDR | 19 | | 30 | VDDSDR |
| SDRAM9 | 20 | | 29 | SDRAM6 |
| SDRAM8 | 21 | | 28 | SDRAM7 |
| GND | 22 | | 27 | VDD48 |
| SDATA | 23 | | 26 | 48MHz/FS0* |
| SCLK | 24 | | 25 | 24MHz/FS1* |

**48-Pin 300mil SSOP**

\* Internal Pull-up Resistor of 120K to VDD
\*\* Internal Pull-down resistor of 120K to GND

## Block Diagram
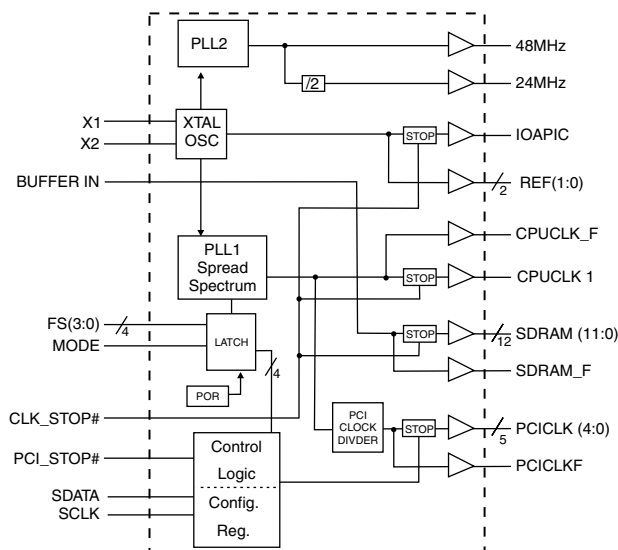


## Functionality

| FS3 | FS2 | FS1 | FS0 | CPU (MHz) | PCICLK (MHz) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 80.00 | 40.00 |
| 0 | 0 | 0 | 1 | 75.00 | 37.50 |
| 0 | 0 | 1 | 0 | 83.31 | 41.65 |
| 0 | 0 | 1 | 1 | 66.82 | 33.41 |
| 0 | 1 | 0 | 0 | 103.00 | 34.33 |
| 0 | 1 | 0 | 1 | 112.01 | 37.34 |
| 0 | 1 | 1 | 0 | 68.01 | 34.01 |
| 0 | 1 | 1 | 1 | 100.23 | 33.41 |
| 1 | 0 | 0 | 0 | 120.00 | 40.00 |
| 1 | 0 | 0 | 1 | 114.99 | 38.33 |
| 1 | 0 | 1 | 0 | 109.99 | 36.66 |
| 1 | 0 | 1 | 1 | 105.00 | 35.00 |
| 1 | 1 | 0 | 0 | 140.00 | 35.00 |
| 1 | 1 | 0 | 1 | 150.00 | 37.50 |
| 1 | 1 | 1 | 0 | 124.00 | 31.00 |
| 1 | 1 | 1 | 1 | 133.33 | 33.33 |

# ICS9248-169

## Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1, 6, 14, 19, 27, 30, 36 | VDD | PWR | 3.3V Power supply |
| 2 | REF0 | OUT | 14.318 Mhz reference clock. |
| | PCI_STOP#[1] | IN | Halts PCICLK(0:4) clocks at logic 0 level, when input low  (In mobile mode, MODE=0) |
| 3,9,16,22, 33,39,45 | GND | PWR | Ground |
| 4 | X1 | IN | Crystal input, has internal load cap (36pF) and feedback resistor from X2 |
| 5 | X2 | OUT | Crystal output, nominally 14.318MHz. Has internal load cap (36pF) |
| 7 | PCICLK_F | OUT | Free running PCI clock not affected by PCI_STOP# for power management. |
| | MODE[1, 2] | IN | Pin 7 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input. |
| 8 | FS3 | IN | Frequency select pin. Latched Input. Internal Pull-down to GND |
| | PCICLK0 | OUT | PCI clock outputs. Syncheronous to CPU clocks with 1-4ns skew (CPU early) |
| 13, 12, 11, 10 | PCICLK (4:1) | OUT | PCI clock outputs. Syncheronous to CPU clocks with 1-4ns skew (CPU early) |
| 15 | BUFFER IN | IN | Input to Fanout Buffers for SDRAM outputs. |
| 17, 18, 20, 21, 28, 29, 31, 32, 34, 35,37,38 | SDRAM (11:0) | OUT | SDRAM clock outputs, Fanout Buffer outputs from BUFFER IN pin (controlled by chipset). |
| 23 | SDATA | I/O | Data pin for I²C circuitry 5V tolerant |
| 24 | SCLK | IN | Clock pin of I²C circuitry 5V tolerant |
| 25 | 24MHz | OUT | 24MHz output clock |
| | FS1[1, 2] | IN | Frequency select pin. Latched Input. |
| 26 | 48MHz | OUT | 48MHz output clock |
| | FS0[1, 2] | IN | Frequency select pin. Latched Input |
| 40 | SDRAM_F | OUT | Free running SDRAM clock output. Not affected by CPU_STOP# |
| 41 | CLK_STOP# | IN | This asynchronous input halts CPUCLK1, IOAPIC & SDRAM (0:11) at logic "0" level when driven low. |
| 42, 48 | VDDL | PWR | Supply for CPU, IOAPIC clocks, either 2.5V or 3.3V nominal |
| 43 | CPUCLK1 | OUT | CPU clock outputs, powered by VDDL2. Low if CPU_STOP#=Low |
| 44 | CPUCLK_F | OUT | Free running CPU clock. Not affected by the CPU_STOP# |
| 46 | REF1 | OUT | 14.318 MHz reference clock. |
| | FS2[1, 2] | IN | Frequency select pin. Latched Input |
| 47 | IOAPIC | OUT | IOAPIC clock output. 14.318 MHz Powered by VDDL1. |

**Notes:**

1:   Internal Pull-up Resistor of 120K to 3.3V on indicated inputs
2:   Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor
     to program logic Hi to VDD or GND for logic low.

## General Description

The **ICS9248-169** is a single chip clock solution for Desktop designs. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I$^2$C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-169 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I$^2$C interface allows changing functions, stop clock programming and frequency selection.

## Power Groups

VDDREF = REF (1:0), X1, X2
VDDPCI = PCICLK_F, PCICLK(4:0)
VDDA = Supply for PLL core
VDD48 = 24MHz, 48MHz
VDDL = CPUCLK, CPUCLK_F, IOAPIC
VDDSDR = SDRAM

## Mode Pin - Power Management Input Control

| MODE, Pin 7 (Latched Input) | Pin 2 |
|---|---|
| 0 | PCI_STOP# (Input) |
| 1 | REF0 (Output) |

# General I$^2$C serial interface information

The information in this section assumes familiarity with I$^2$C programming.
For more information, contact ICS for an I$^2$C programming application note.

## How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will *acknowledge*
- Controller (host) sends a dummy command code
- ICS clock will *acknowledge*
- Controller (host) sends a dummy byte count
- ICS clock will *acknowledge*
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will *acknowledge* each byte *one at a time*.
- Controller (host) sends a Stop bit

## How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 $_{(H)}$
- ICS clock will *acknowledge*
- ICS clock will send the *byte count*
- Controller (host) acknowledges
- ICS clock sends first byte *(Byte 0) through byte 5*
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Write: | |
|---|---|
| **Controller (Host)** | **ICS (Slave/Receiver)** |
| Start Bit | |
| Address D2$_{(H)}$ | |
| | *ACK* |
| Dummy Command Code | |
| | *ACK* |
| Dummy Byte Count | |
| | *ACK* |
| Byte 0 | |
| | *ACK* |
| Byte 1 | |
| | *ACK* |
| Byte 2 | |
| | *ACK* |
| Byte 3 | |
| | *ACK* |
| Byte 4 | |
| | *ACK* |
| Byte 5 | |
| | *ACK* |
| Stop Bit | |

| How to Read: | |
|---|---|
| **Controller (Host)** | **ICS (Slave/Receiver)** |
| Start Bit | |
| Address D3$_{(H)}$ | |
| | *ACK* |
| | *Byte Count* |
| ACK | |
| | *Byte 0* |
| ACK | |
| | *Byte 1* |
| ACK | |
| | *Byte 2* |
| ACK | |
| | *Byte 3* |
| ACK | |
| | *Byte 4* |
| ACK | |
| | *Byte 5* |
| ACK | |
| Stop Bit | |

## Notes:

1. The ICS clock generator is a slave/receiver, I$^2$C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I$^2$C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

## Serial Configuration Command Bitmap

**Byte0: Functionality and Frequency Select Register (default = 0)**

| Bit | Description | | | | | | | PWD |
|---|---|---|---|---|---|---|---|---|
| | Bit (2, 7, 6, 5, 4) | | | | | CPUCLK (MHz) | PCICLK (MHz) | |
| Bit 2, Bit 7:4 | 0 | 0 | 0 | 0 | 0 | 80.00 | 40.00 | 00101 Note1 |
| | 0 | 0 | 0 | 0 | 1 | 75.00 | 37.50 | |
| | 0 | 0 | 0 | 1 | 0 | 83.31 | 41.65 | |
| | 0 | 0 | 0 | 1 | 1 | 66.82 | 33.41 | |
| | 0 | 0 | 1 | 0 | 0 | 103.00 | 34.33 | |
| | 0 | 0 | 1 | 0 | 1 | 112.01 | 37.34 | |
| | 0 | 0 | 1 | 1 | 0 | 68.01 | 34.01 | |
| | 0 | 0 | 1 | 1 | 1 | 100.23 | 33.41 | |
| | 0 | 1 | 0 | 0 | 0 | 120.00 | 40.00 | |
| | 0 | 1 | 0 | 0 | 1 | 114.99 | 38.33 | |
| | 0 | 1 | 0 | 1 | 0 | 109.99 | 36.66 | |
| | 0 | 1 | 0 | 1 | 1 | 105.00 | 35.00 | |
| | 0 | 1 | 1 | 0 | 0 | 140.00 | 35.00 | |
| | 0 | 1 | 1 | 0 | 1 | 150.00 | 37.50 | |
| | 0 | 1 | 1 | 1 | 0 | 124.00 | 31.00 | |
| | 0 | 1 | 1 | 1 | 1 | 133.33 | 33.33 | |
| | 1 | 0 | 0 | 0 | 0 | 135.00 | 33.75 | |
| | 1 | 0 | 0 | 0 | 1 | 129.99 | 32.50 | |
| | 1 | 0 | 0 | 1 | 0 | 126.00 | 31.50 | |
| | 1 | 0 | 0 | 1 | 1 | 118.00 | 39.33 | |
| | 1 | 0 | 1 | 0 | 0 | 115.98 | 38.66 | |
| | 1 | 0 | 1 | 0 | 1 | 95.00 | 31.67 | |
| | 1 | 0 | 1 | 1 | 0 | 90.00 | 30.00 | |
| | 1 | 0 | 1 | 1 | 1 | 85.01 | 28.34 | |
| | 1 | 1 | 0 | 0 | 0 | 166.00 | 41.50 | |
| | 1 | 1 | 0 | 0 | 1 | 160.01 | 40.00 | |
| | 1 | 1 | 0 | 1 | 0 | 154.99 | 38.75 | |
| | 1 | 1 | 0 | 1 | 1 | 147.95 | 36.99 | |
| | 1 | 1 | 1 | 0 | 0 | 145.98 | 36.50 | |
| | 1 | 1 | 1 | 0 | 1 | 143.98 | 35.99 | |
| | 1 | 1 | 1 | 1 | 0 | 141.99 | 35.50 | |
| | 1 | 1 | 1 | 1 | 1 | 138.01 | 34.50 | |
| Bit 3 | 0 - Frequency is selected by hardware select, Latched Inputs <br> 1 - Frequency is selected by Bit 2, 7:4 | | | | | | | 0 |
| Bit 1 | 0 - Normal <br> 1 - Spread Spectrum Enabled ± 0.50% Center Spread | | | | | | | 1 |
| Bit 0 | 0 - Running <br> 1- Tristate all outputs | | | | | | | 0 |

Note1: Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

**Byte 1: CPU, Active/Inactive Register**
(1= enable, 0 = disable)

| BIT | PIN# | PWD | DESCRIPTION |
|-----|------|-----|-------------|
| Bit 7 | - | X | Latched FS2# |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | - | 1 | (Reserved) |
| Bit 3 | 40 | 1 | SDRAM_F |
| Bit 2 | - | 1 | (Reserved) |
| Bit 1 | 43 | 1 | CPUCLK1 |
| Bit 0 | 44 | 1 | CPUCLK_F |

**Byte 2: PCI, Active/Inactive Register**
(1= enable, 0 = disable)

| BIT | PIN# | PWD | DESCRIPTION |
|-----|------|-----|-------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | 7 | 1 | PCICLK_F |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | 13 | 1 | PCICLK4 |
| Bit 3 | 12 | 1 | PCICLK3 |
| Bit 2 | 11 | 1 | PCICLK2 |
| Bit 1 | 10 | 1 | PCICLK1 |
| Bit 0 | 8 | 1 | PCICLK0 |

**Byte 3: SDRAM, Active/Inactive Register**
(1= enable, 0 = disable)

| BIT | PIN# | PWD | DESCRIPTION |
|-----|------|-----|-------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | X | Latched FS0# |
| Bit 5 | 26 | 1 | 48MHz |
| Bit 4 | 25 | 1 | 24 MHz |
| Bit 3 | - | 1 | (Reserved) |
| Bit 2 | 21,20, 18,17 | 1 | SDRAM (8:11) |
| Bit 1 | 32,31, 29,28 | 1 | SDRAM (4:7) |
| Bit 0 | 38,37, 35,34 | 1 | SDRAM (0:3) |

**Byte 4: Reserved , Active/Inactive Register**
(1= enable, 0 = disable)

| BIT | PIN# | PWD | DESCRIPTION |
|-----|------|-----|-------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | - | 1 | (Reserved) |
| Bit 3 | - | X | Latched FS1# |
| Bit 2 | - | 1 | (Reserved) |
| Bit 1 | - | X | Latched FS3# |
| Bit 0 | - | 1 | (Reserved) |

**Byte 5: Peripheral , Active/Inactive Register**
(1= enable, 0 = disable)

| BIT | PIN# | PWD | DESCRIPTION |
|-----|------|-----|-------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | 47 | 1 | IOAPIC |
| Bit 3 | - | 1 | (Reserved) |
| Bit 2 | - | 1 | (Reserved) |
| Bit 1 | 46 | 1 | REF1 |
| Bit 0 | 2 | 1 | REF0 |

**Byte 6: Peripheral , Active/Inactive Register**
(1= enable, 0 = disable)

| BIT | PIN# | PWD | DESCRIPTION |
|-----|------|-----|-------------|
| Bit7 | - | 0 | Reserved (Note) |
| Bit6 | - | 0 | Reserved (Note) |
| Bit5 | - | 0 | Reserved (Note) |
| Bit4 | - | 0 | Reserved (Note) |
| Bit3 | - | 0 | Reserved (Note) |
| Bit2 | - | 1 | Reserved (Note) |
| Bit1 | - | 1 | Reserved (Note) |
| Bit0 | - | 0 | Reserved (Note) |

**Note: Don't write into this register, writing into this register can cause malfunction**
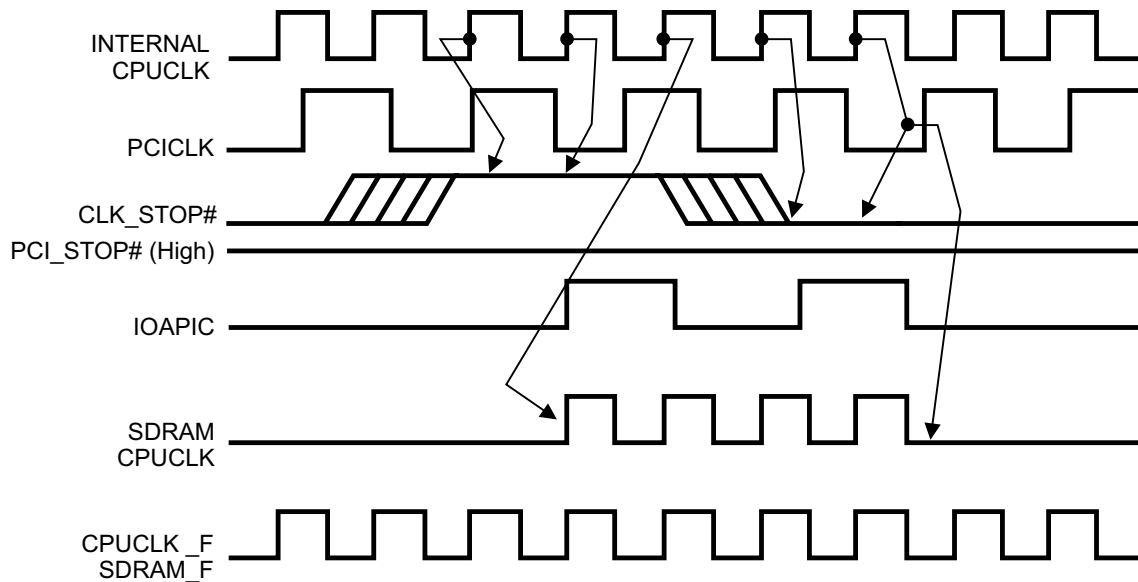
**Notes:**
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

## CLK_STOP#  Timing Diagram

CLK_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CLK_STOP# is synchronized by the **ICS9248-169**. The minimum that the CPU clock is enabled (CLK_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.

**Notes:**

1. All timing is referenced to the internal CPU clock.

2. CLK_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-169.

3. IOAPIC output is Stopped Glitch Free by CLK_STOP# going low.

4. SDRAM-F output is controlled by Buffer in signal, not affected by the **ICS9248-169** CLK_STOP# signal. SDRAM's are controlled as shown.

5. All other clocks continue to run undisturbed.

## PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-169**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-169** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.
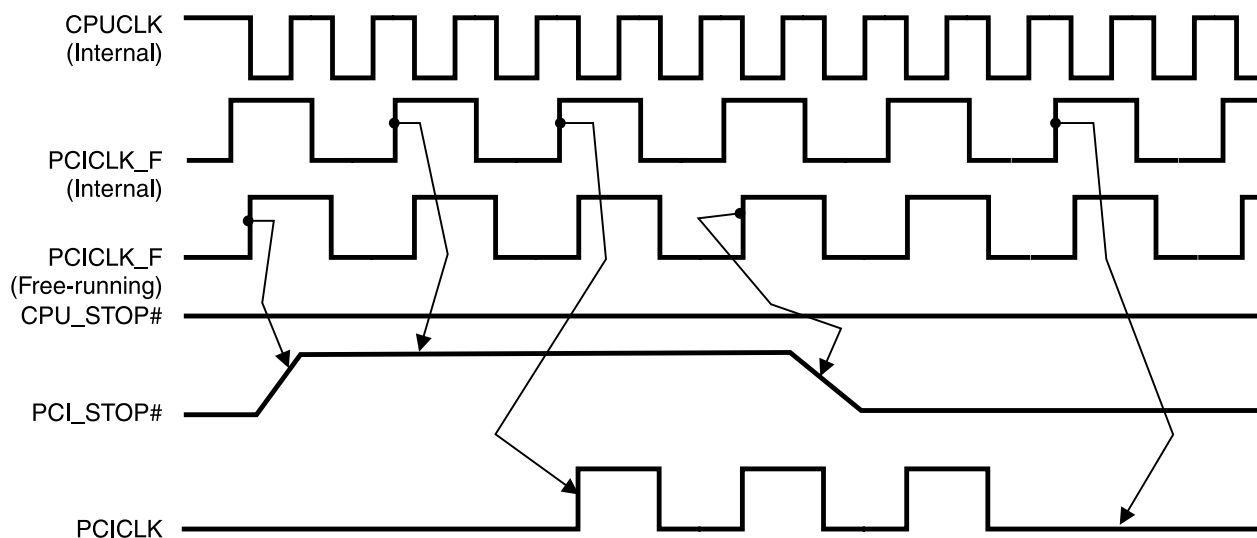


**Notes:**

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-169 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248-169.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

## Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-169 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.
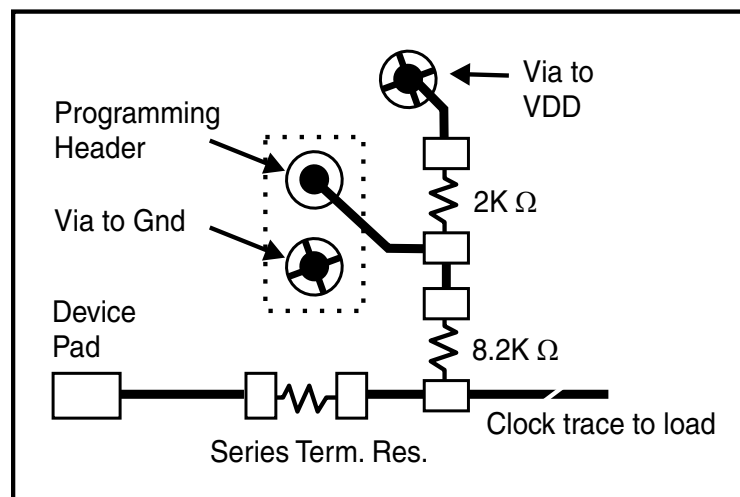


**Fig. 1**

## Absolute Maximum Ratings

Supply Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5 V
Logic Inputs . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . GND –0.5 V to $V_{DD}$ +0.5 V
Ambient Operating Temperature . . . . . . . . . . . . . 0°C to +70°C
Case Temperature . . . . . . . . . . . . . . . . . . . . . . . . . 115°C
Storage Temperature . . . . . . . . . . . . . . . . . . . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = 0 - 70º C; Supply Voltage $V_{DD}$ =$V_{DDL}$= 3.3 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | 2 | | $V_{DD}$+0.3 | V |
| Input Low Voltage | $V_{IL}$ | | $V_{SS}$-0.3 | | 0.8 | V |
| Input High Current | $I_{IH}$ | $V_{IN}$=$V_{DD}$ | | | 5 | uA |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | uA |
| Input Low Current | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | uA |
| Operating Supply Current | $I_{DD3.3OP66}$ | $C_L$ = 0 pF; Select @ 66.8 MHz | | 94 | 180 | mA |
| | $I_{DD3.3OP100}$ | $C_L$ = 0 pF; Select @ 100 MHz | | 130 | | |
| Input frequency | $F_i$ | $V_{DD}$ = 3.3 V | 12 | 14.318 | 16 | MHz |
| Input Capacitance[1] | $C_{IN}$ | Logic Inputs | | | 5 | pF |
| | $C_{INX}$ | X1 & X2 pins | 27 | | 45 | pF |
| Clk Stabilization[1] | $T_{STAB}$ | From $V_{DD}$ = 3.3 V to 1% target Freq. | | | 3 | ms |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = 0 - 70º C; Supply Voltage $V_{DD}$ = 3.3 V +/- 5%, $V_{DDL}$= 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Operating Supply Current | $I_{DD2.5OP66}$ | $C_L$ = 0 pF; Select @ 66.8 MHz | | | 72 | mA |
| | $I_{DD2.5OP100}$ | $C_L$ = 0 pF; Select @ 100 MHz | | | 100 | |
| Skew[1] | $t_{CPU-PCI}$ | $V_T$ = 1.5V; $V_{TL}$ = 1.25V | 0.5 | 1.12 | 1.5 | ns |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - CPUCLK

$T_A$ = 0 - 70C; $V_{DD}$=3.3V +/- 5%, $V_{DDL}$=2.5V +/- 5%; $C_L$ = 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH2B}$ | $I_{OH}$ = -8 mA | 2 | 2.4 | | V |
| Output Low Voltage | $V_{OL2B}$ | $I_{OL}$ = 12 mA | | 0.17 | 0.4 | V |
| Output High Current | $I_{OH2B}$ | $V_{OH}$ = 1.7 V | | -58 | -16 | mA |
| Output Low Current | $I_{OL2B}$ | $V_{OL}$ = 0.7 V | 19 | 46 | | mA |
| Rise Time[1] | $t_{r2B}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.0 V | | 1.3 | 1.6 | ns |
| Fall Time[1] | $t_{f2B}$ | $V_{OH}$ = 2.0 V, $V_{OL}$ = 0.4 V | | 1.0 | 1.6 | ns |
| Duty Cycle[1] | $d_{t2B}$ | $V_T$ = 1.25 V | 45 | 47.5 | 55 | % |
| Skew [1] | $t_{sk2B}$ | $V_T$ = 1.25 V | | 41 | 175 | ps |
| Jitter, Cycle-to-cycle[1] | $t_{jcyc-cyc2B}$ | $V_T$ = 1.25 V | | 216 | 250 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - PCICLK

$T_A$ = 0 - 70C; $V_{DD}$ = 3.3V +/-5%, $V_{DDL}$ = 2.5V +/-5%; $C_L$ = 30 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH1}$ | $I_{OH}$ = -11 mA | 2.4 | 3.15 | | V |
| Output Low Voltage | $V_{OL1}$ | $I_{OL}$ = 9.4 mA | | 0.13 | 0.4 | V |
| Output High Current | $I_{OH1}$ | $V_{OH}$ = 2.0 V | | -97 | -40 | mA |
| Output Low Current | $I_{OL1}$ | $V_{OL}$ = 0.8 V | 41 | 69 | | mA |
| Rise Time[1] | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | | 1.66 | 2.0 | ns |
| Fall Time[1] | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | | 1.52 | 2.0 | ns |
| Duty Cycle[1] | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 49.7 | 55 | % |
| Skew[1] | $t_{sk1}$ | $V_T$ = 1.5 V | | 254 | 500 | ps |
| Jitter, Absolute[1] | $t_{jabs1}$ | $V_T$ = 1.5 V | -500 | 180 | 500 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - SDRAM

$T_A$ = 0 - 70C; $V_{DD}$ = 3.3V +/-5%, $V_{DDL}$ = 2.5V +/-5%; $C_L$ = 30 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH3}$ | $I_{OH}$ = -28 mA | 2.4 | 3.0 | | V |
| Output Low Voltage | $V_{OL3}$ | $I_{OL}$ = 20 mA | | 0.18 | 0.4 | V |
| Output High Current | $I_{OH3}$ | $V_{OH}$ = 2.0 V | | -110 | -40 | mA |
| Output Low Current | $I_{OL3}$ | $V_{OL}$ = 0.8 V | 41 | 86 | | mA |
| Rise Time[1] | $t_{r3}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | | 1.13 | 2 | ns |
| Fall Time[1] | $t_{f3}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | | 1.11 | 2 | ns |
| Duty Cycle[1] | $d_{t3}$ | $V_T$ = 1.5 V | 45 | 53.1 | 55 | % |
| Skew [1] | $t_{sk3}$ | $V_T$ = 1.5 V | | 215 | 500 | ps |
| Propagation Delay[1] (Buffer In to Output) | Tprop | $V_T$ = 1.5 V | | 3.26 | 5 | ns |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - IOAPIC

$T_A$ = 0 - 70C; $V_{DD}$=3.3V +/- 5%, $V_{DDL}$=2.5V +/- 5%; $C_L$ = 20 pF (unless otherwise stated)

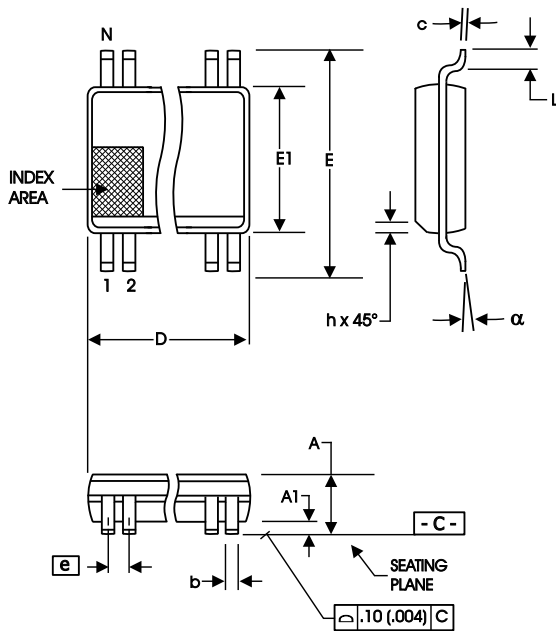| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH4B}$ | $I_{OH}$ = -8 mA | 2 | 2.4 | | V |
| Output Low Voltage | $V_{OL4B}$ | $I_{OL}$ = 12 mA | | 0.17 | 0.4 | V |
| Output High Current | $I_{OH4B}$ | $V_{OH}$ = 1.7 V | | -58 | -16 | mA |
| Output Low Current | $I_{OL4B}$ | $V_{OL}$ = 0.7 V | 19 | 46 | | mA |
| Rise Time[1] | $t_{r4B}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.0 V | | 1.14 | 2 | ns |
| Fall Time[1] | $t_{f4B}$ | $V_{OH}$ = 2.0 V, $V_{OL}$ = 0.4 V | | 1.07 | 2 | ns |
| Duty Cycle[1] | $d_{t4B}$ | $V_T$ = 1.25 V | 45 | 52.7 | 55 | % |
| Jitter, Absolute[1] | $t_{jabs4B}$ | $V_T$ = 1.25 V | -1 | 0.27 | 1 | ns |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - REF, 48MHz, 24MHz

$T_A = 0 - 70C$; $V_{DD} = 3.3V$ +/-5%, $V_{DDL} = 2.5V$ +/-5%; $C_L = 20$ pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH5}$ | $I_{OH}$ = -12 mA | 2.4 | 3.03 | | V |
| Output Low Voltage | $V_{OL5}$ | $I_{OL}$ = 10 mA | | 0.23 | 0.4 | V |
| Output High Current | $I_{OH5}$ | $V_{OH}$ = 2.0 V | | -50 | -22 | mA |
| Output Low Current | $I_{OL5}$ | $V_{OL}$ = 0.8 V | 16 | 40 | | mA |
| Rise Time[1] | $t_{r5}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | | 1.26 | 4.0 | ns |
| Fall Time[1] | $t_{f5}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | | 1.57 | 4.0 | ns |
| Duty Cycle[1] | $d_{t5}$ | $V_T$ = 1.5 V | 45 | 53.3 | 55 | % |
| Jitter, Absolute[1] | $t_{jabs5}$ | $V_T$ = 1.5 V | -1 | 0.25 | 1 | ns |

[1]Guaranteed by design, not 100% tested in production.

Third party brands and names are the property of their respective owners.

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**300 mil SSOP Package**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 48 | 15.75 | 16.00 | .620 | .630 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

## Ordering Information

**ICS9248yF-169-T**

Example:

**ICS XXXX y F - PPP - T**

 └─ **Designation for tape and reel packaging**

 └─ **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**

 └─ **Package Type**
   F=SSOP

 └─ **Revision Designator** (will not correlate with datasheet revision)

 └─ **Device Type (consists of 3 or 4 digit numbers)**

 └─ **Prefix**
   ICS, AV = Standard Device