

Automotive-grade N-channel 600 V, 0.26 Ω typ., 13 A MDmesh™ II Power MOSFET in a TO-247 package

Datasheet - production data

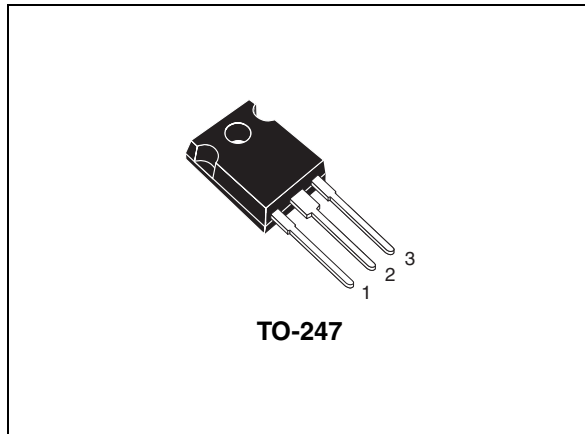
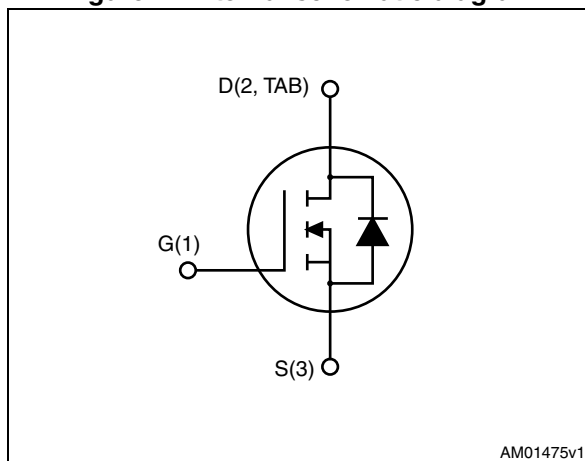


Figure 1. Internal schematic diagram



Features

Order code	V_{DS} (@ T_{jmax})	$R_{DS(on)}$ max.	I_D	P_{TOT}
STW19NM60N	650 V	0.285 Ω	13 A	110 W

- Designed for automotive applications and AEC-Q101 qualified
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STW19NM60N	19NM60N	TO-247	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Revision history	12

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate- source voltage	± 25	
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	13	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8.2	A
$I_{DM}^{(1)}$	Drain current (pulsed)	52	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	350	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_J	Operating junction temperature	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature		$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 13\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} \leq 80\% V_{(BR)DSS}$, $V_{DS(peak)} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.14	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	50	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

($T_{CASE}=25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$			1	μA
		$V_{DS} = 600\text{ V}, T_J = 125\text{ °C}$			10	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 6.5\text{ A}$		0.260	0.285	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	1000	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Output equivalent capacitance	$V_{DS} = 0, \text{ to } 480\text{ V}, V_{GS} = 0$	-	225	-	pF
R_g	Intrinsic resistance	$f = 1\text{ MHz}$ open drain	-	3.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 13\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 15)	-	35	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	20	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 6.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14)	-	12	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
t_f	Fall time		-	25	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		13	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		52	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 13\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16)	-	300		ns
Q_{rr}	Reverse recovery charge		-	4.0		μC
I_{RRM}	Reverse recovery current		-	25		A
t_{rr}	Reverse recovery time	$V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $I_{SD} = 13\text{ A}$ $T_j = 150^\circ\text{C}$ (see Figure 16)	-	360		ns
Q_{rr}	Reverse recovery charge		-	4.5		μC
I_{RRM}	Reverse recovery current		-	25		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

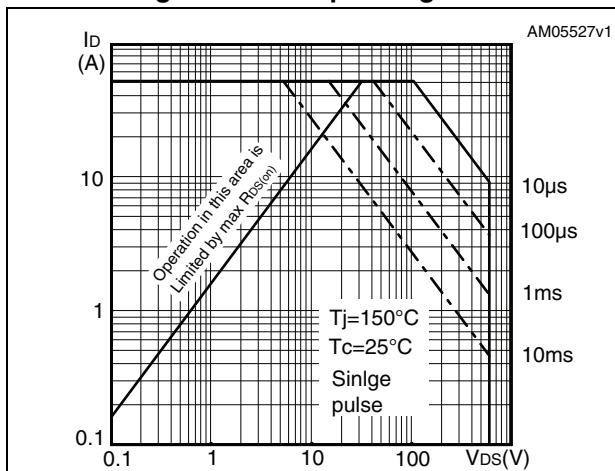


Figure 3. Thermal impedance

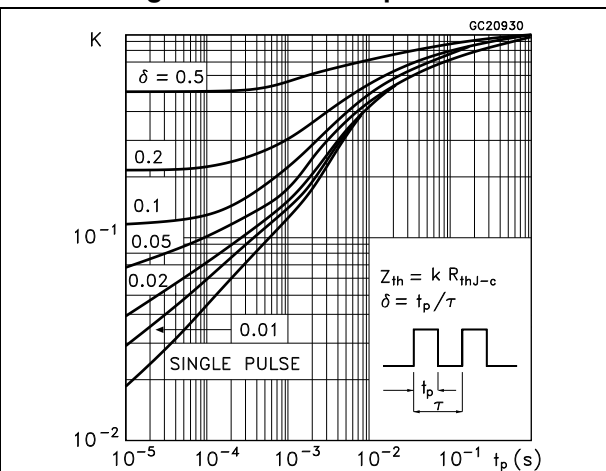


Figure 4. Output characteristics

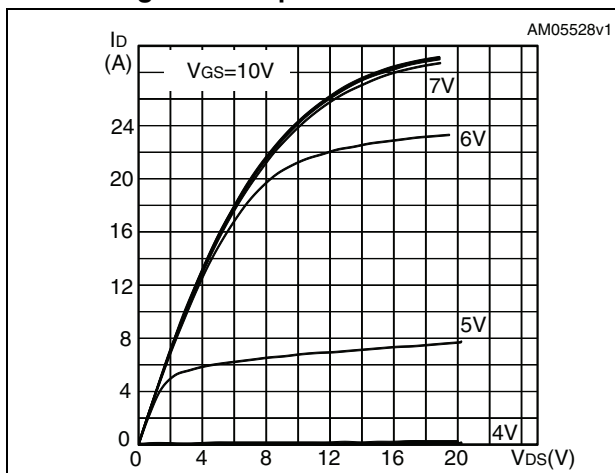


Figure 5. Transfer characteristics

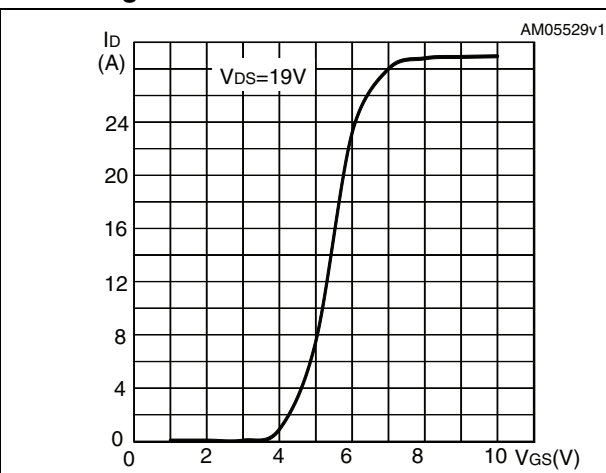


Figure 6. Static drain-source on-resistance

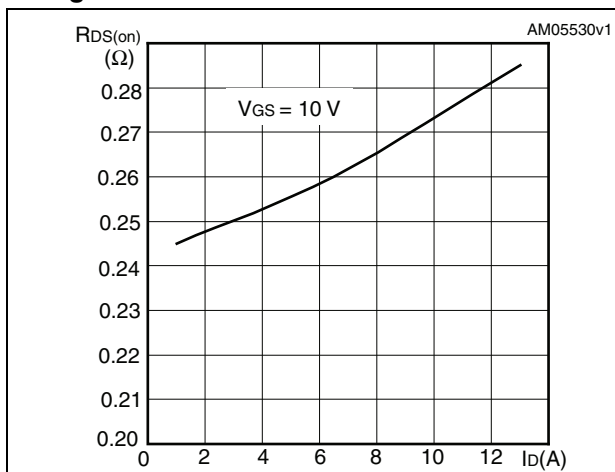


Figure 7. Gate charge vs gate-source voltage

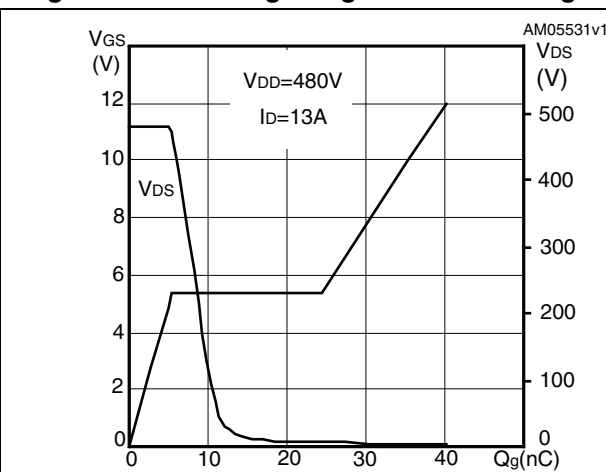


Figure 8. Capacitance variations

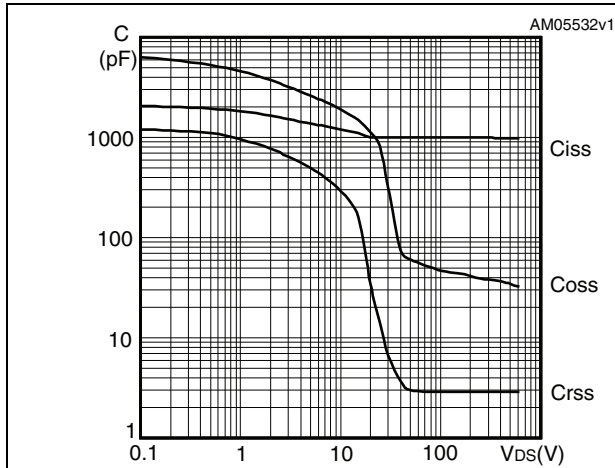


Figure 9. Output capacitance stored energy

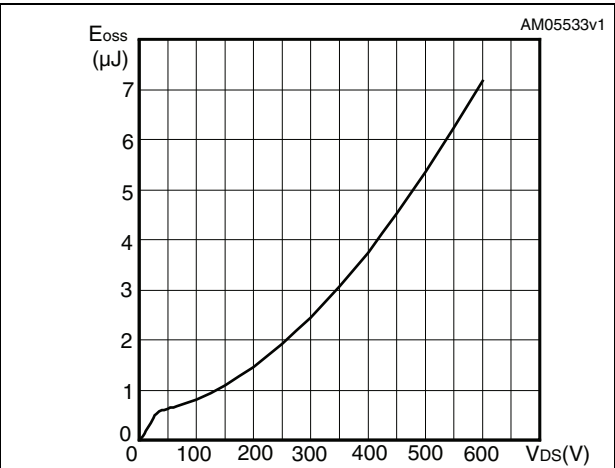


Figure 10. Normalized gate threshold voltage vs temperature

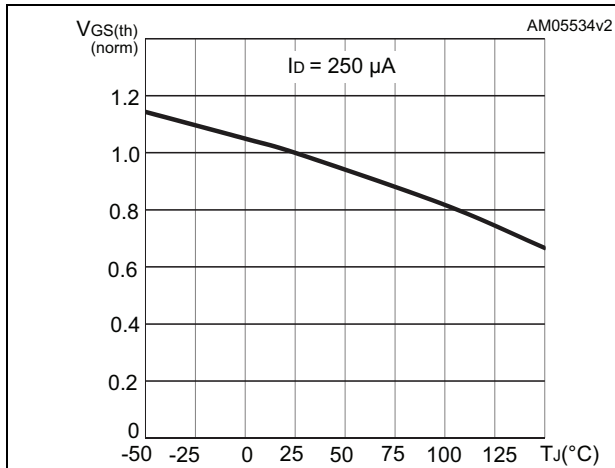


Figure 11. Normalized on-resistance vs temperature

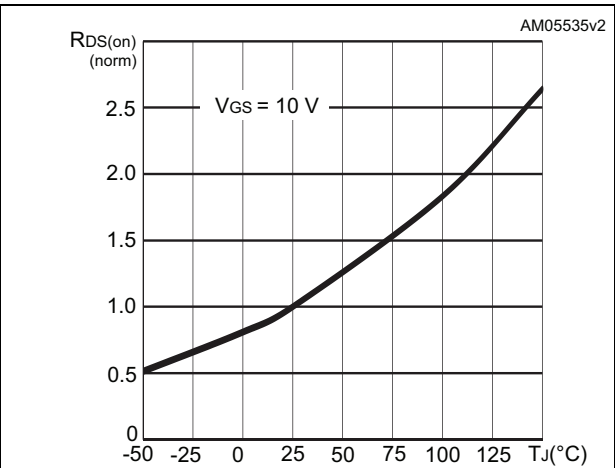


Figure 12. Normalized VDS vs temperature

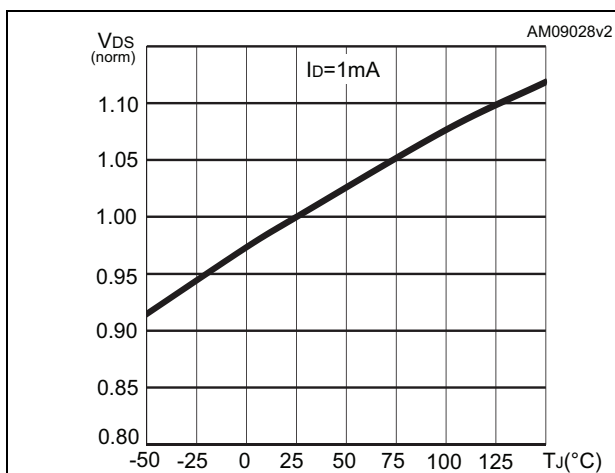
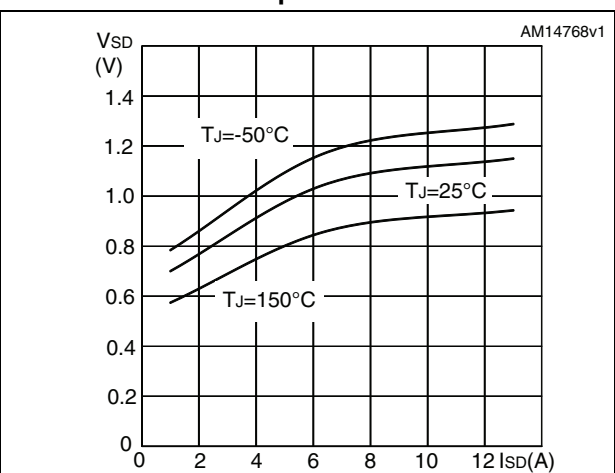
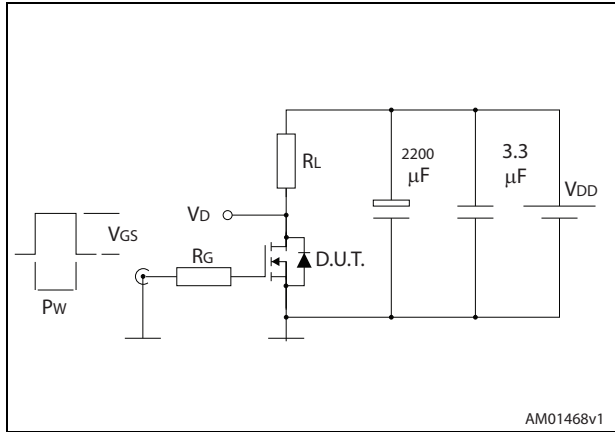


Figure 13. Source-drain diode forward vs temperature



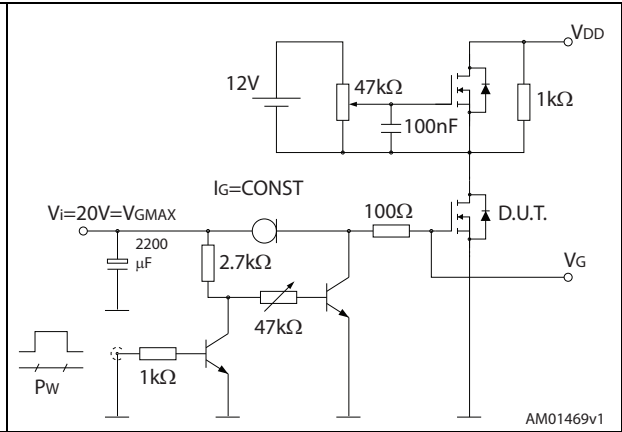
3 Test circuits

Figure 14. Switching times test circuit for resistive load



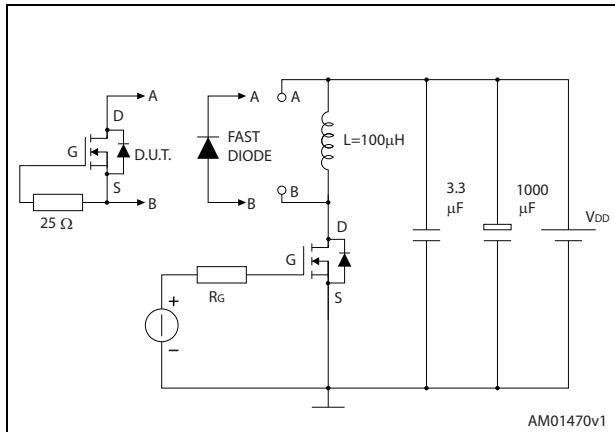
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Figure 15. Gate charge test circuit



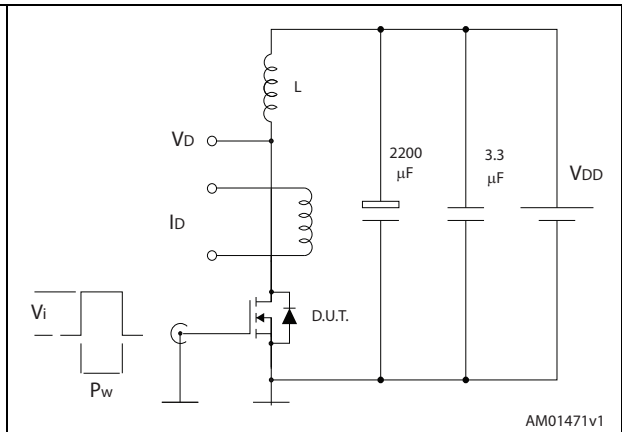
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Figure 16. Test circuit for inductive load switching and diode recovery times



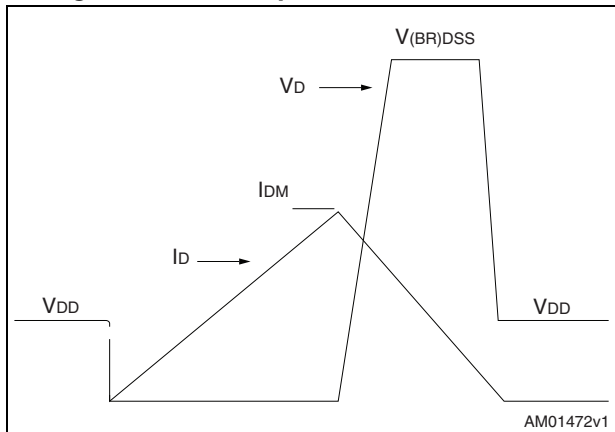
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Figure 17. Unclamped inductive load test circuit



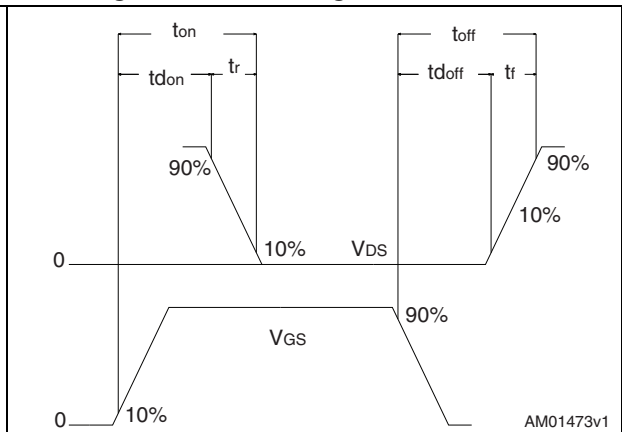
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Figure 18. Unclamped inductive waveform



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Figure 19. Switching time waveform



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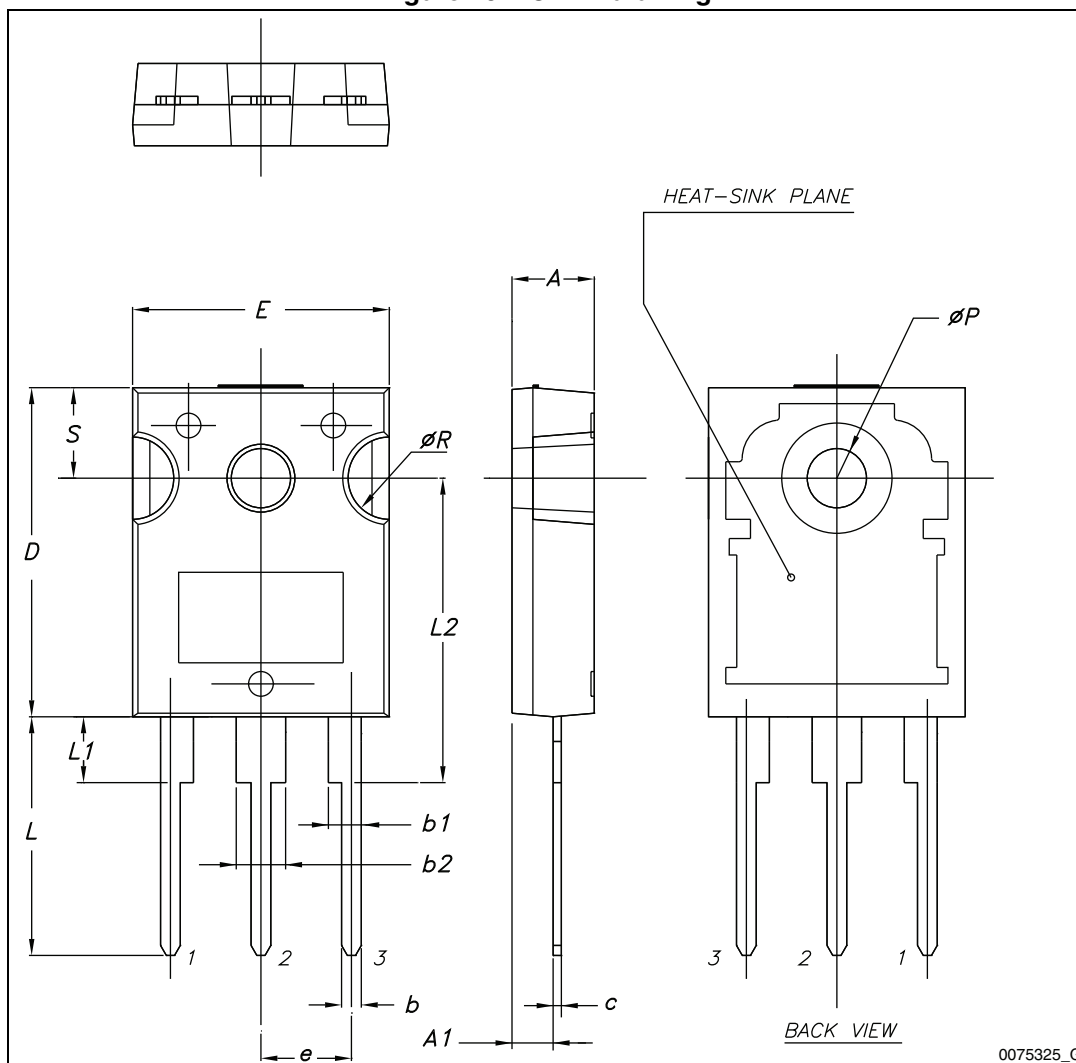
4 Package mechanical data

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Table 8. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 20. TO-247 drawing



0075325_G

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Mar-2013	1	Initial release.
24-Oct-2013	2	– Modified: title, features and applications – Minor text changes

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