STPC® VEGA

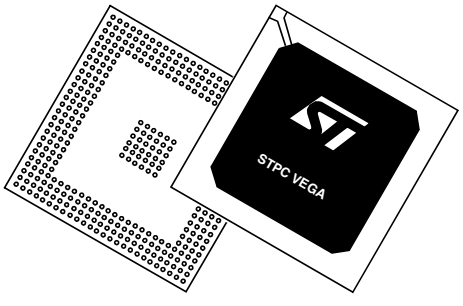
X86 CORE PC COMPATIBLE SOC with ETHERNET and USB

DATA BRIEF

- PENTIUM® II CLASS PROCESSOR CORE
- 64-BIT SDRAM CONTROLLER RUNNING AT UP TO 100 MHZ
- PCI 2.1 COMPLIANT MASTER/SLAVE CONTROLLER
- ISA MASTER / SLAVE
- DUAL PORT USB HOST CONTROLLER (OHCI)
- 10/100 ETHERNET MAC [1)]
- INTEGRATED PERIPHERAL CONTROLLER WITH SUPPPORT FOR EXTERNAL RTC
- ULTRA DMA-66 IDE CONTROLLER
- POWER MANAGEMENT UNIT
- 16-BIT LOCAL BUS INTERFACE
- I2C BUS CONTROLLER
- UART (1 RxTx)
- IEEE 1149.1 JTAG INTERFACE
- 8 GENERAL PURPOSE IO
- PROGRAMMABLE CLOCKS
- 0.18 MICRON TECHNOLOGY
- 1.8 V CORE & 3.3 V I/Os
- LOW POWER CONSUMPTION DEVICE

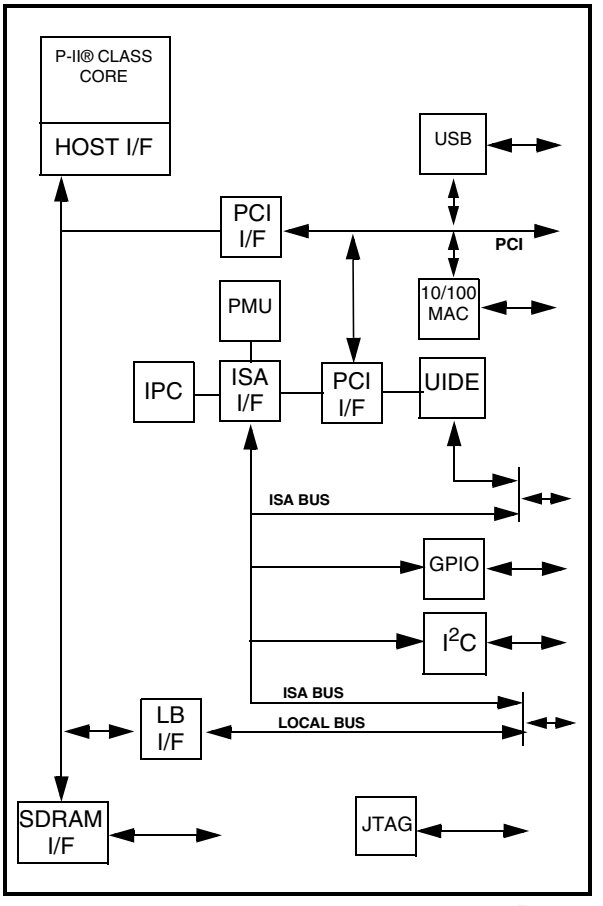
DESCRIPTION

The STPC VEGA integrates a fully static Pentium® II® Class processor, fully compatible with Industry Standards, and combines it with a powerful chipset to provide a general purpose PC compatible subsystem on a single device. The device is packaged in a 388 Ball Grid Array (PBGA).



PBGA388

Block Diagram



1- The usage of the internal MAC 10/100 is very restricted. For more information see 10/100 Ethernet Controller description.

Rev. 4

- **X86 Processor**
- x86 Pentium® II class processor running in X2 mode
  -3 Issue integer six-stage pipeline/clock
  -3 issue MMX®/clock
  -Pipelined FPU
- Bus clock with skew correction
- Internal core clocks generated as multiples of bus clock with multiplication factors of X2, X2.5, X3, X3.5

- **SDRAM Interface**
- 64-bit data bus
- 100 MHz maximum SDRAM clock
- 8 MByte to 256 MByte memory size (only the upper 128MByte cacheable)
- Supports 16 Mbit to 256 Mbit memories
- Support for -8 to -15 memory parts
- Supports buffered and non-buffered DIMMs
- Supports registered DIMMs
- Programmable latency

- **PCI Controller Master/Slave**
- Compatible with PCI Version 2.1 specification
- Integrated PCI arbitration interface. Up to three external masters can be directly connected
- Master/Slave Bridge to USB, LAN, UIDE & ISA cycles
- Support for burst read/write from PCI master
- 0.20X, 0.25X, 0.33X and 0.5X Host clock PCI clock. Automatically selected.

- **ISA Master/Slave**
- Generates the ISA clock from either 14.318 MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles
- Fast Gate A20 and Fast reset
- Supports Flash ROM
- Supports ISA hidden refresh
- Buffered DMA and ISA master cycles to reduce the bandwidth utilization of PCI and system bus

- **Local Bus**
- Multiplexed with ISA interface
- 16-bit bus data path with word steering capability
- Two cacheable banks of 32 Mbyte flash devices (boot block shadowed from 000C0000h to 000FFFFFh)
- Programmable timing with host clock granularity for flash accesses
- 32-bit flash burst support
- Two-level hardware key protection for flash boot block protection
- Up to eight IO devices (four Chipselects) supported with programmable start address & size
- IO device timing (setup & recovery time) programmable

- **Integrated Peripherals Controller**
- Interrupt Controller: 8259 compatible (two Interrupt controllers)
- DMA Controller: 8237 compatible (two DMA controllers)
- Page register
- Counter 0 and counter 1 gates are always on, counter 2 is controlled by writing to Port B
- Supports external RTC

- **Ultra DMA-66 IDE Controller**
- Supports IDE hard drives larger than 528 MBytes
- Support for two connectors to allow up to four drives
- Support for CD-ROM and tape peripherals
- Support for 11.1/16.6 Mbytes/second, I/O Channel Ready PIO data transfers
- Supports up to 66 Mbytes/second, UDMA data transfers
- Ultra DMA supports CRC-16 error checking protocol (no correction supported)
- PIO: 0 to 5, DMA: 0 to 2, UDMA: 0 to 4

- Backward compatibility with IDE (ATA-1)

- **8 GPIO**
- Individual pins programmable as either input or output
- Interrupt generation with selectable masking

■ **10/100 Ethernet Controller**

The usage of VEGA internal MAC is very restricted and tested only under Linux operating system with the specific configuration 100Mb/s Half and Full Duplex . Any other functional configuration is not guaranteed by STMicroelectronics.

Problem that maybe occur is a file transfer corruption , however the use of the internal MAC for browsing applications or http session does not causes problem.

- Compliant with IEEE 802.3, 802.3u specification
- Supports 10/100 Mb/s data transfer rates
- IEEE 802.3 compliant MII interface to talk to an external physical layer (PHY)
- VLAN support
- Supports both full-duplex and half-duplex operations
- Supports CSMA/CD Protocol for half-duplex
- Supports flow-control for full-duplex operation
- Collision detection and auto retransmission on collisions in half-duplex mode
- Management support using a variety of counters
- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- Optional insertion of PAD/CRC32 on transmit
- Options for Automatic Pad stripping on the receive packets
- Provides external and internal loop back capability on the MII Interface
- Contains a variety of flexible address filtering modes on the Ethernet side:
  - One 48-bit Perfect address
  - 64 hash-filtered multicast addresses
  - Pass all multicast addresses
  - Promiscuous Mode
  - Pass all incoming packets with a status report

■ **USB Host Controller**
- Open HCI Rev 1.1 compatible
- USB Rev 1.1 compatible
- Root hub with two down-stream ports with power switching control
- Support of both low & high speed USB devices
- Support of system management interupt (SMI)

■ **UART**
- One UART RxTx only
- Programmable word length, stop bits and parity
- Programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Scratch register
- Two 16-byte FIFOs

■ **Power Management Unit**
- Four power saving modes: On, Doze, Standby, Suspend
- Programmable system activity detector
- Supports STPCLK#

■ **I2C Bus Controller**
- One I2C compliant master/slave bus controller
- Slow and fast modes supported

■ **JTAG Function**
- Boundary Scan Chain function

Notes