



## Dual N-Channel 30 V (D-S) MOSFETs

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) (Max.)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
Channel-1	30	0.0058 at V <sub>GS</sub> = 10 V	40 <sup>a</sup>	12.5 nC
		0.0075 at V <sub>GS</sub> = 4.5 V	40 <sup>a</sup>	
Channel-2	30	0.0030 at V <sub>GS</sub> = 10 V	40 <sup>a</sup>	29 nC
		0.0035 at V <sub>GS</sub> = 4.5 V	40 <sup>a</sup>	

### FEATURES

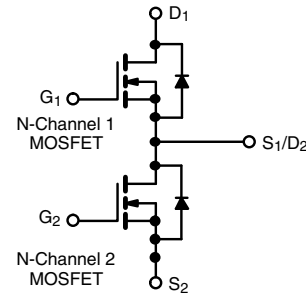
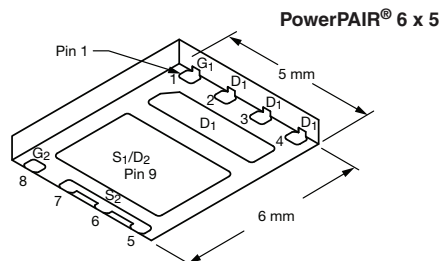
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### APPLICATIONS

- Notebook System Power
- POL
- Synchronous Buck Converter



Ordering Information: SiZ910DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Channel-1	Channel-2	Unit		
Drain-Source Voltage	V <sub>DS</sub>	30		V		
Gate-Source Voltage	V <sub>GS</sub>	± 20				
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	40 <sup>a</sup>	40 <sup>a</sup>		
		T <sub>C</sub> = 70 °C	40 <sup>a</sup>	40 <sup>a</sup>		
		T <sub>A</sub> = 25 °C	22 <sup>b, c</sup>	32 <sup>b, c</sup>		
		T <sub>A</sub> = 70 °C	17 <sup>b, c</sup>	26 <sup>b, c</sup>		
Pulsed Drain Current (t = 300 μs)	I <sub>DM</sub>	100	120	A		
Continuous Source Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	24 <sup>a</sup>		28 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	3.8 <sup>b, c</sup>	4.3 <sup>b, c</sup>		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	25	40		
Single Pulse Avalanche Energy	Maximum Power Dissipation	E <sub>AS</sub>	31	80		
Maximum Power Dissipation			P <sub>D</sub>	T <sub>C</sub> = 25 °C	48	100
				T <sub>C</sub> = 70 °C	31	64
				T <sub>A</sub> = 25 °C	4.6 <sup>b, c</sup>	5.2 <sup>b, c</sup>
	T <sub>A</sub> = 70 °C	3 <sup>b, c</sup>		3.3 <sup>b, c</sup>		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C		
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260				

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Channel-1		Channel-2		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	22	27	19	24	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	2.1	2.6	1	1.25	

Notes:

a. Package limited - T<sub>C</sub> = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 62 °C/W for channel-1 and 55 °C/W for channel-2.

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	30			V	
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-2	30				
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		33		mV/ $^\circ\text{C}$	
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		31			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		- 5.4			
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		- 6.1			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1.2		2.2	V	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-2	1		2.2		
Gate Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-1			$\pm 100$	nA	
			Ch-2			$\pm 100$		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			1	$\mu\text{A}$	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-2			1		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1			5		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-2			5		
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20			A	
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	25				
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-1		0.0048	0.0058	$\Omega$	
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		0.0025	0.0030		
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-1		0.0060	0.0075		
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-2		0.0029	0.0035		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-1		94		S	
		$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		140			
<b>Dynamic<sup>a</sup></b>								
Input Capacitance	$C_{iss}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		1500		pF	
			Ch-2		3600			
Output Capacitance	$C_{oss}$		Ch-1		285			
			Ch-2		660			
Reverse Transfer Capacitance	$C_{rss}$		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		125		
				Ch-2		305		
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		Ch-1		26	40	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		Ch-2		60	110	
		Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		Ch-1		12.5	19	
				Ch-2		29	51	
Gate-Source Charge	$Q_{gs}$	Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-1		4.7			
			Ch-2		10			
Gate-Drain Charge	$Q_{gd}$		Ch-1		4			
			Ch-2		9.5			
Gate Resistance	$R_g$		$f = 1\text{ MHz}$	Ch-1	0.5	2.6	5.2	$\Omega$
				Ch-2	0.1	0.6	1.2	

## Notes:

- a. Guaranteed by design, not subject to production testing.  
b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		20	40	ns
Rise Time	$t_r$		Ch-2		30	60	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		25	50	
			Ch-2		35	70	
Fall Time	$t_f$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		25	50	
			Ch-2		10	20	
Turn-On Delay Time	$t_{d(on)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		10	20	
			Ch-2		12	25	
Rise Time	$t_r$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		25	25	
			Ch-2		12	25	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		30	60	
			Ch-2		35	70	
Fall Time	$t_f$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		10	20	
			Ch-2		10	20	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			40	A
			Ch-2			40	
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		Ch-1			100	
			Ch-2			120	
Body Diode Voltage	$V_{SD}$	$I_S = 10\text{ A}$ , $V_{GS} = 0\text{ V}$	Ch-1		0.8	1.2	V
			Ch-2		0.8	1.2	
Body Diode Reverse Recovery Time	$t_{rr}$	Channel-1 $I_F = 10\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		26	50	ns
			Ch-2		36	70	
Body Diode Reverse Recovery Charge	$Q_{rr}$	Channel-2 $I_F = 10\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		25	50	nC
			Ch-2		36	70	
Reverse Recovery Fall Time	$t_a$	Channel-1 $I_F = 10\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		17		ns
			Ch-2		20		
Reverse Recovery Rise Time	$t_b$	Channel-2 $I_F = 10\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		9		
			Ch-2		16		

## Notes:

- a. Guaranteed by design, not subject to production testing.  
 b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

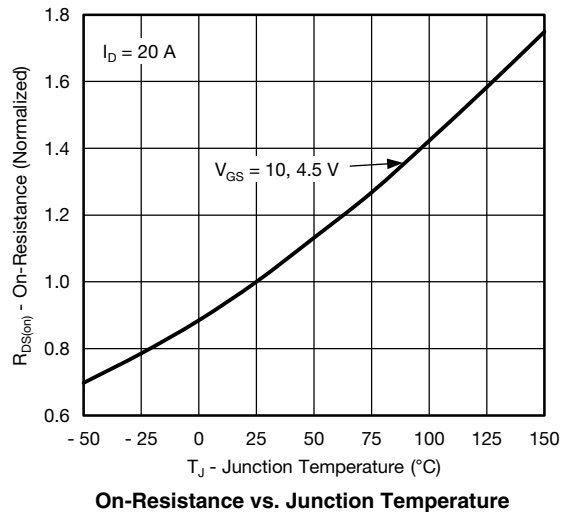
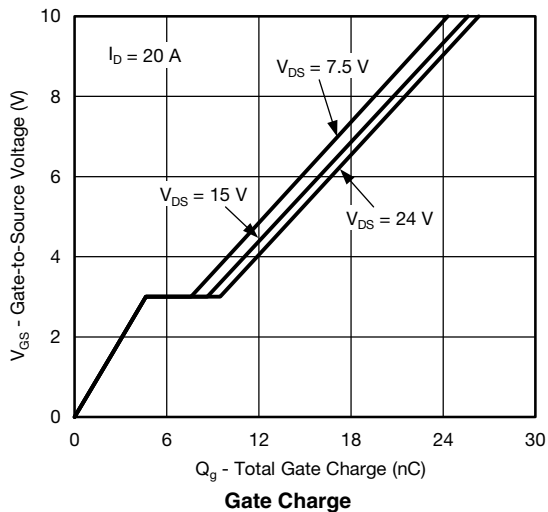
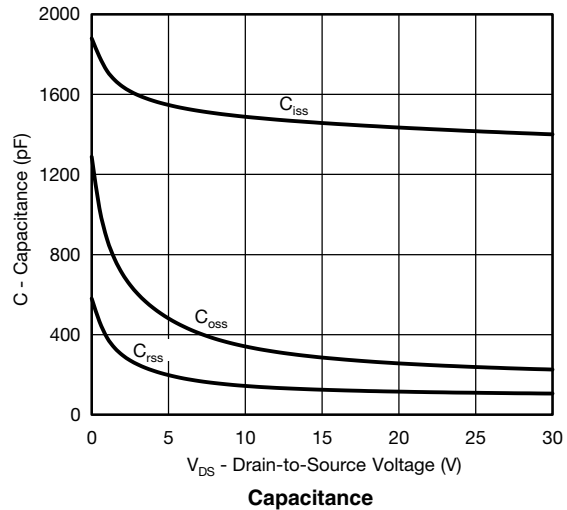
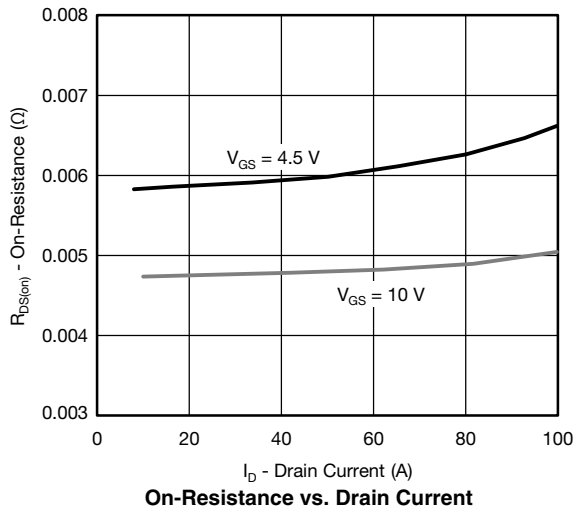
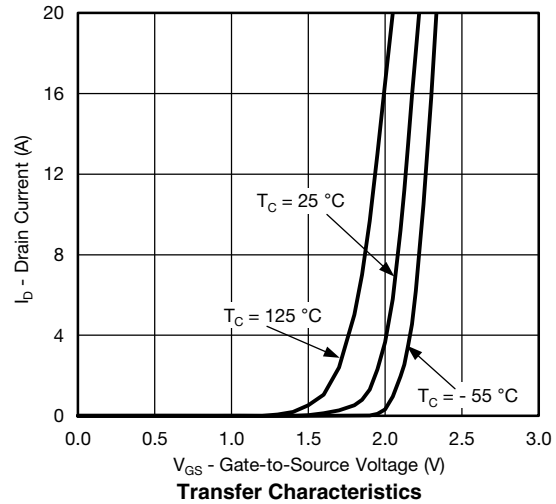
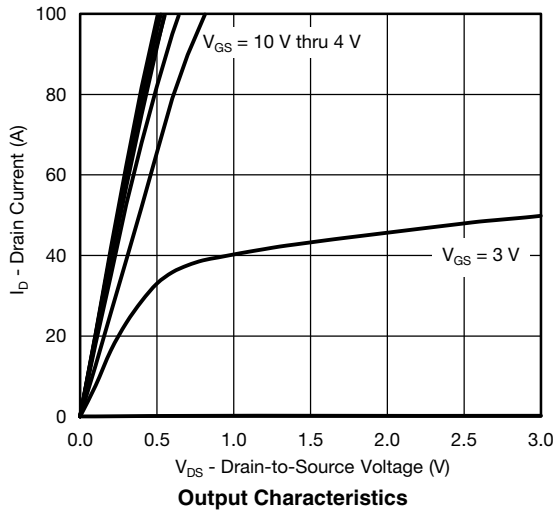
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# SiZ910DT

Vishay Siliconix

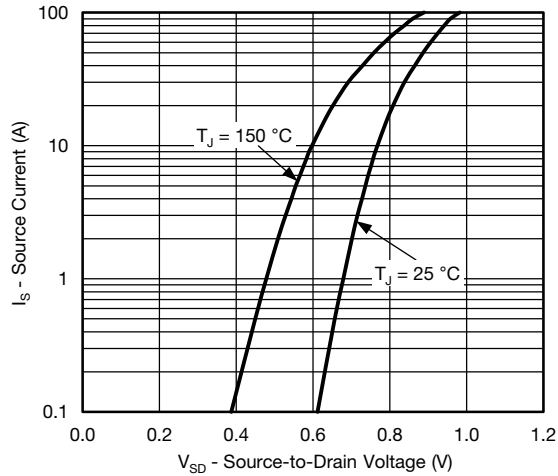


## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

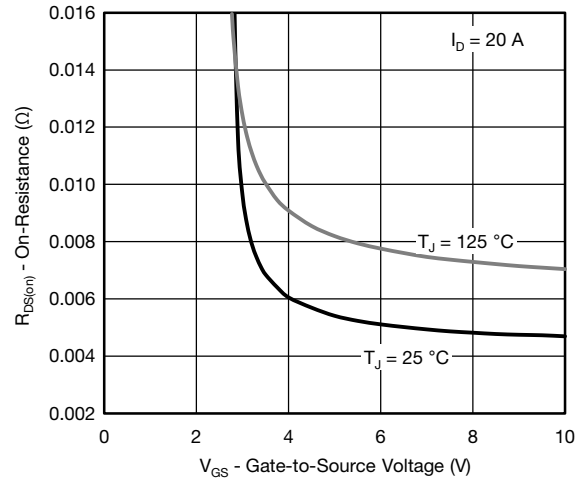




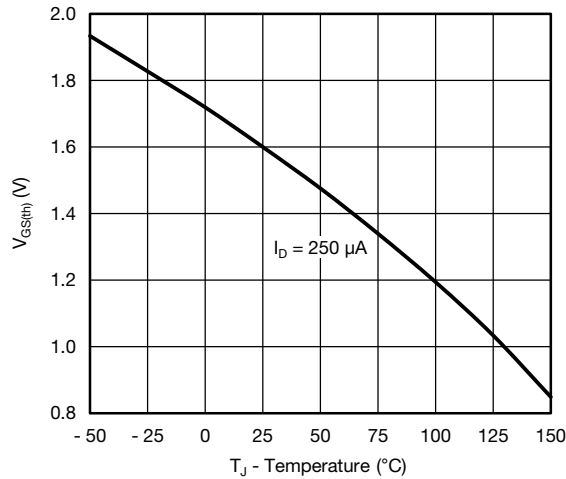
**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



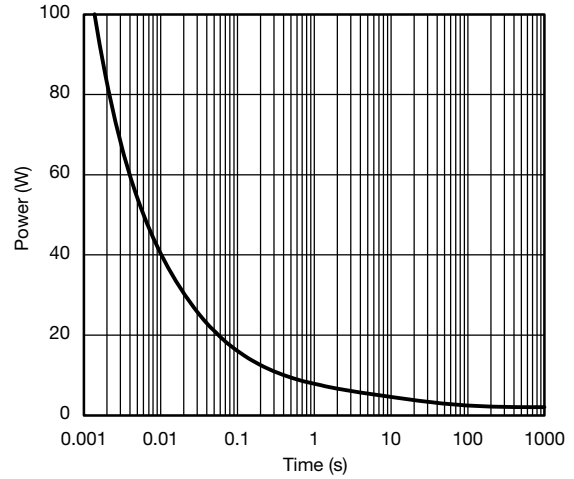
**Source-Drain Diode Forward Voltage**



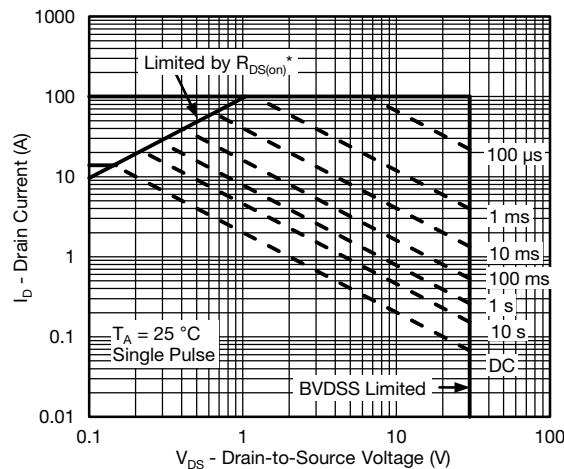
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power**



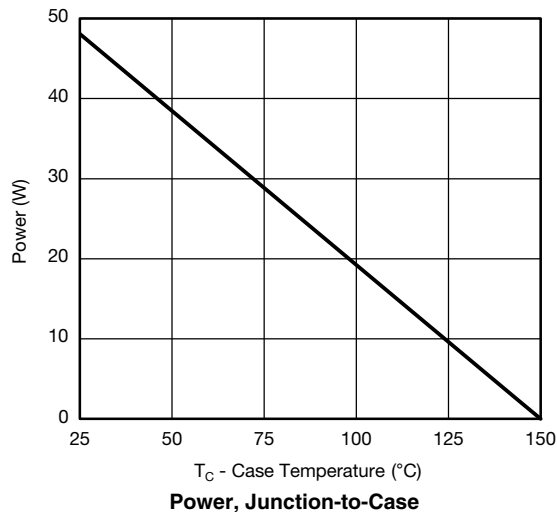
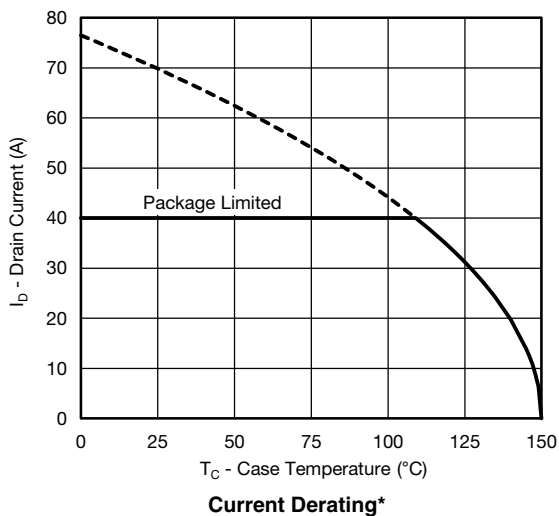
**Safe Operating Area, Junction-to-Ambient**

# SiZ910DT

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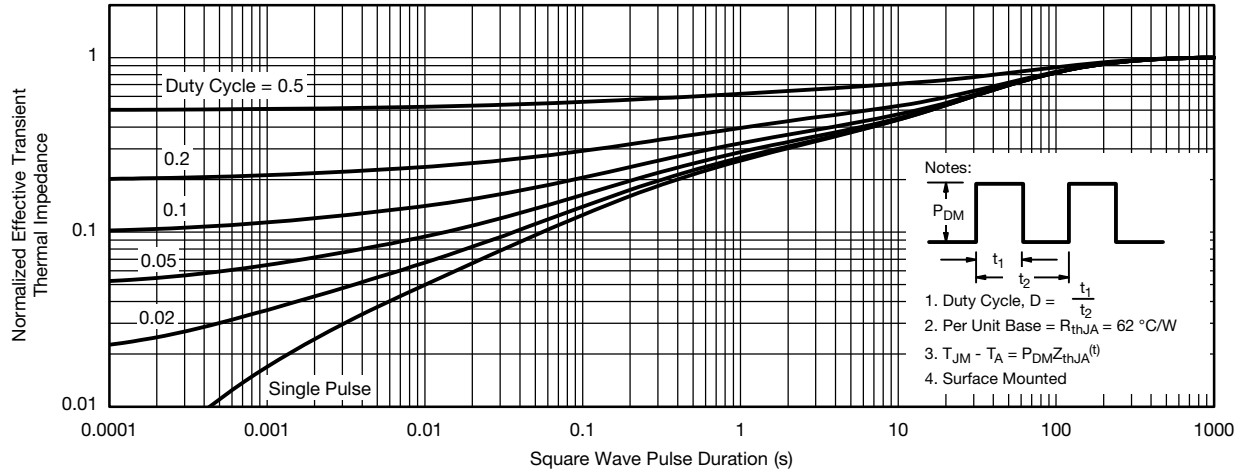
## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



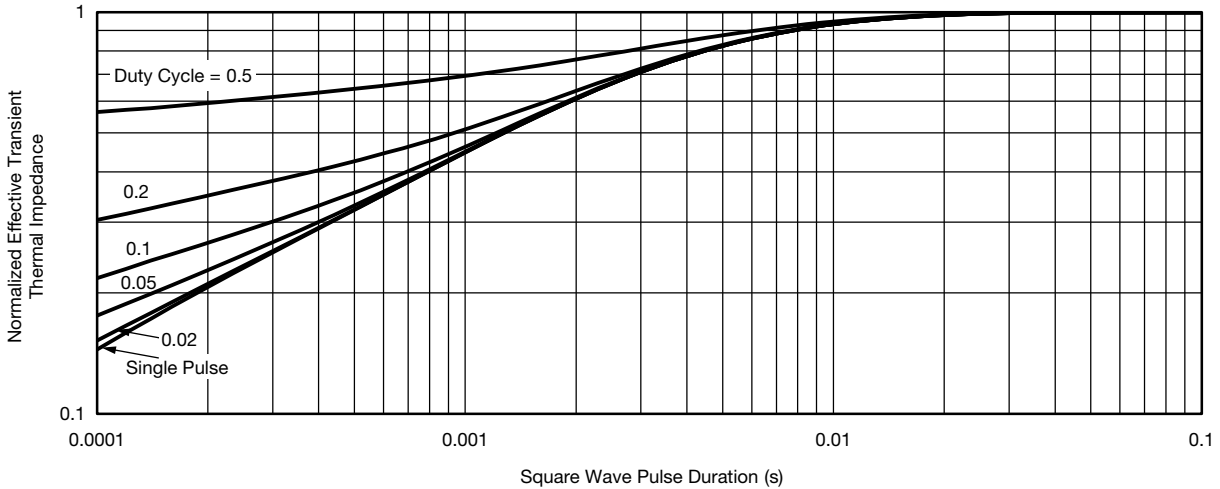
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



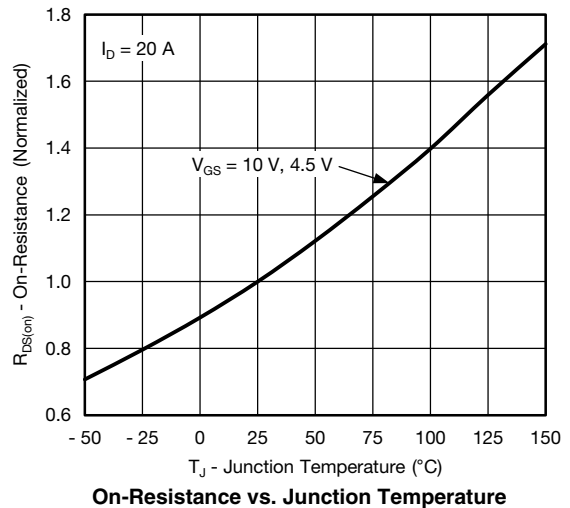
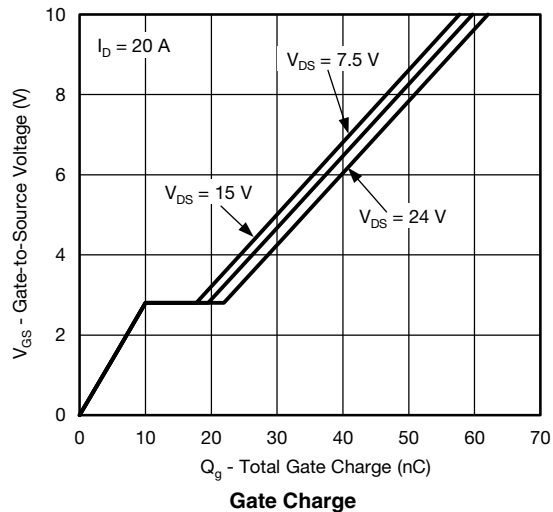
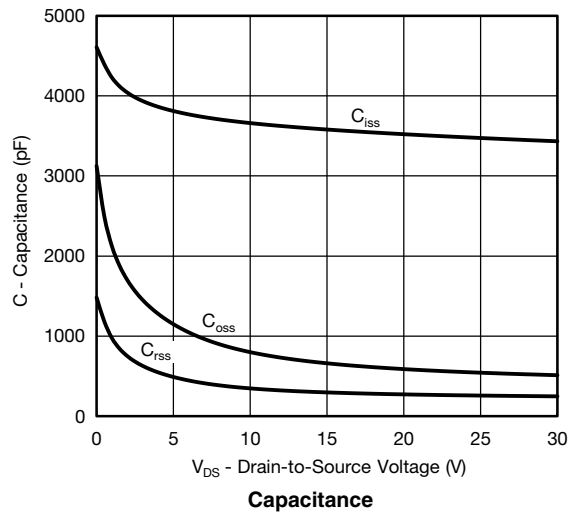
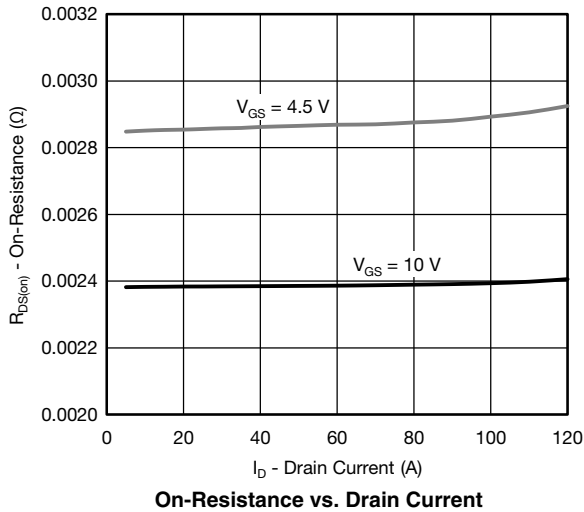
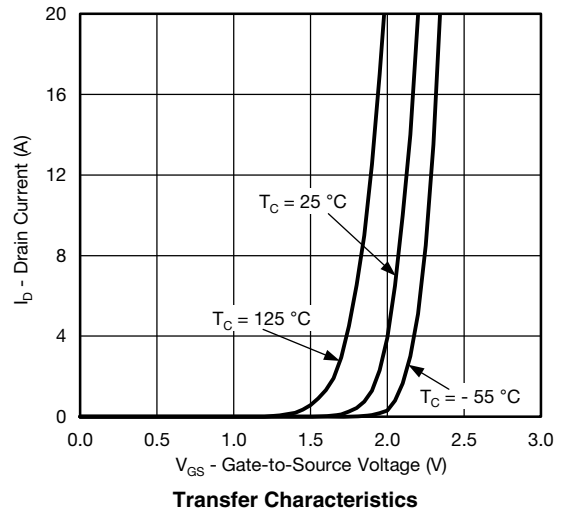
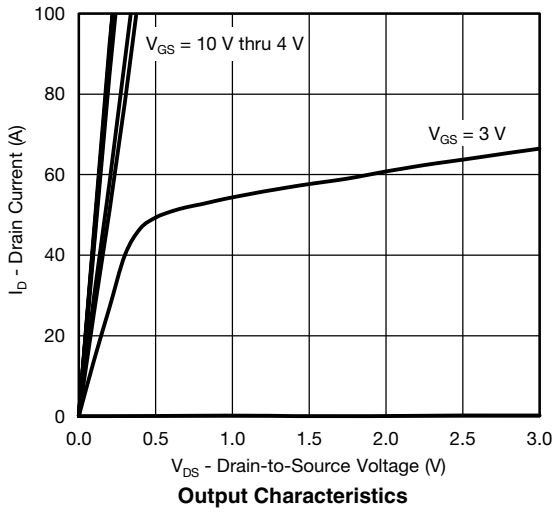
**Normalized Thermal Transient Impedance, Junction-to-Case**

# SiZ910DT

Vishay Siliconix



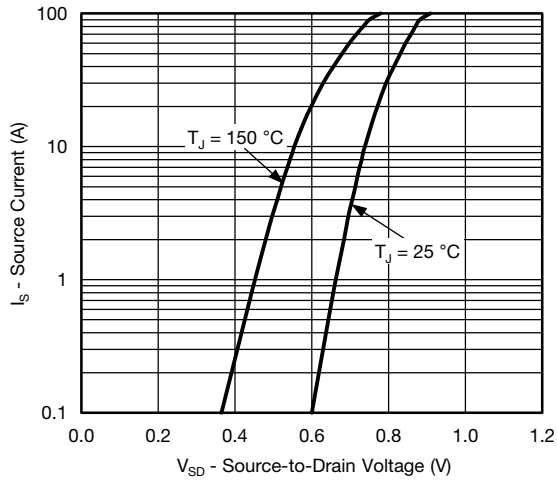
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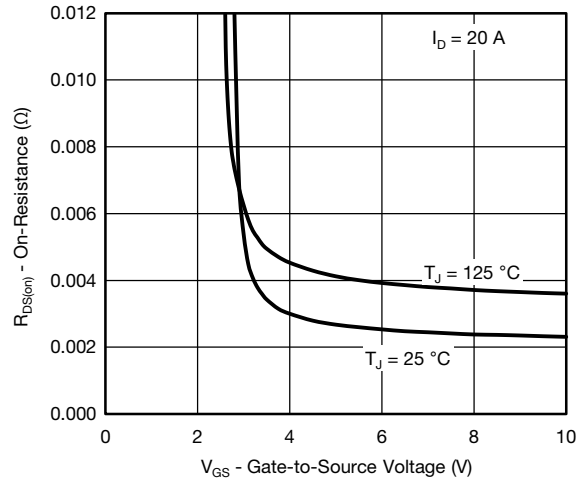




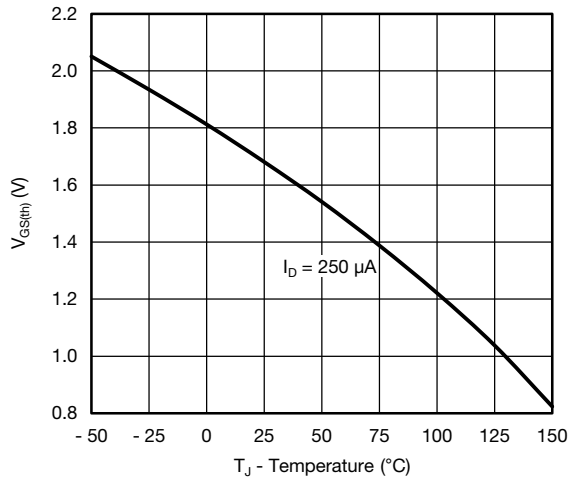
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



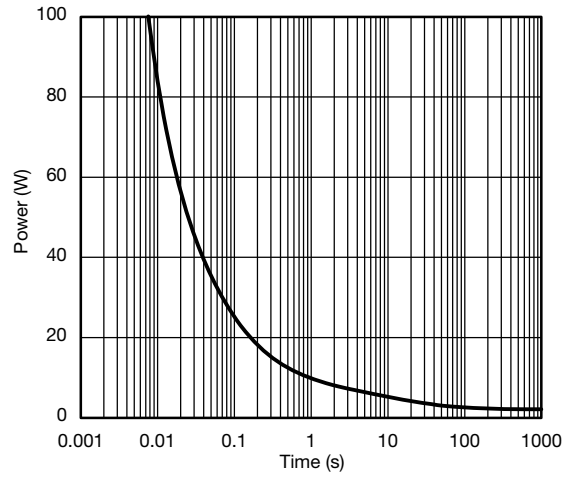
**Source-Drain Diode Forward Voltage**



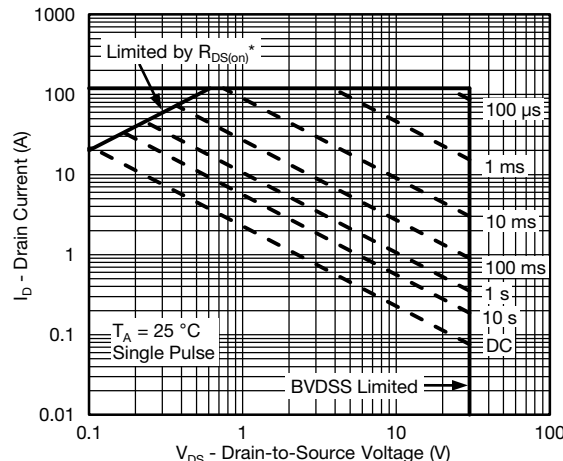
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



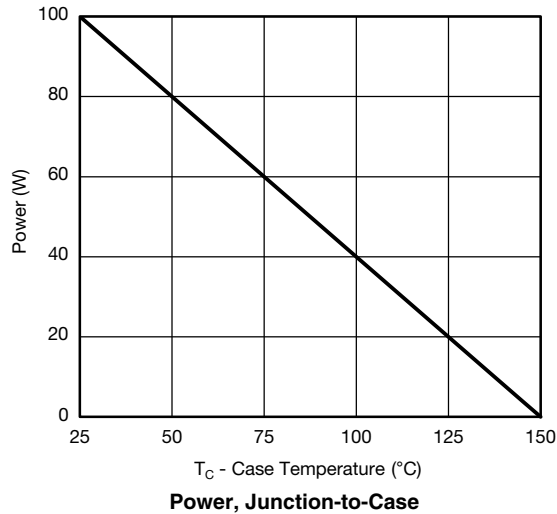
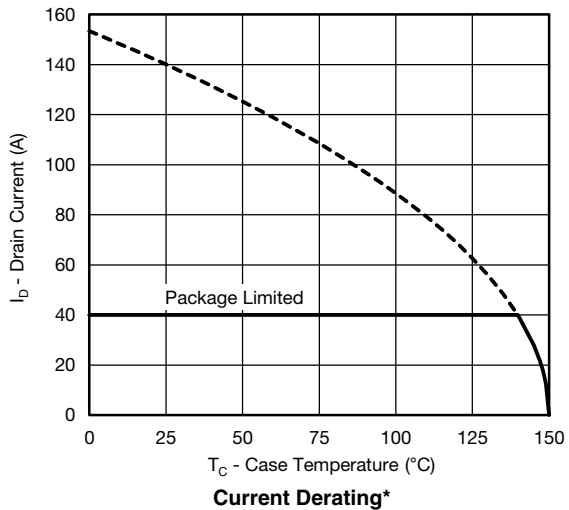
**Single Pulse Power**



**Safe Operating Area, Junction-to-Ambient**



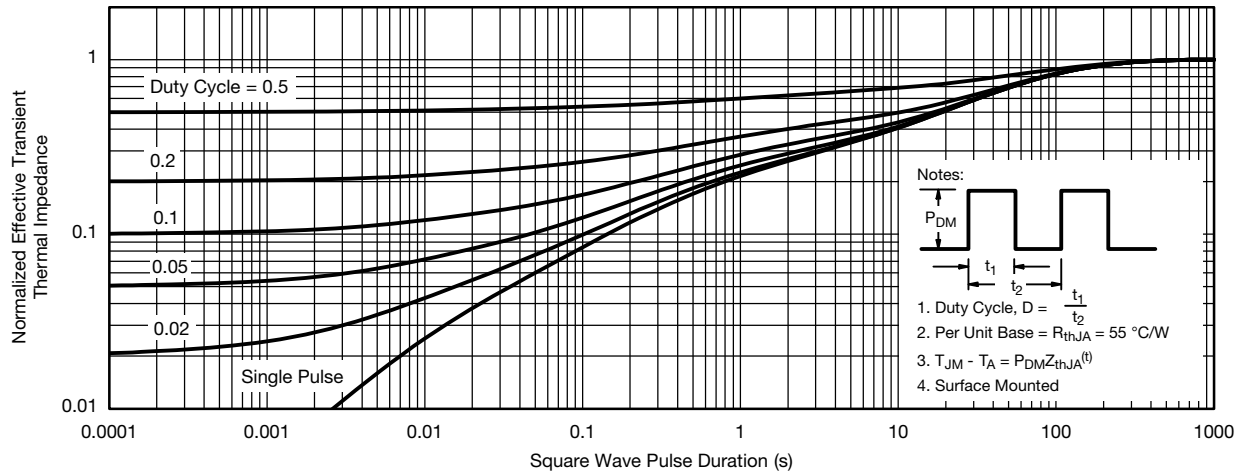
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



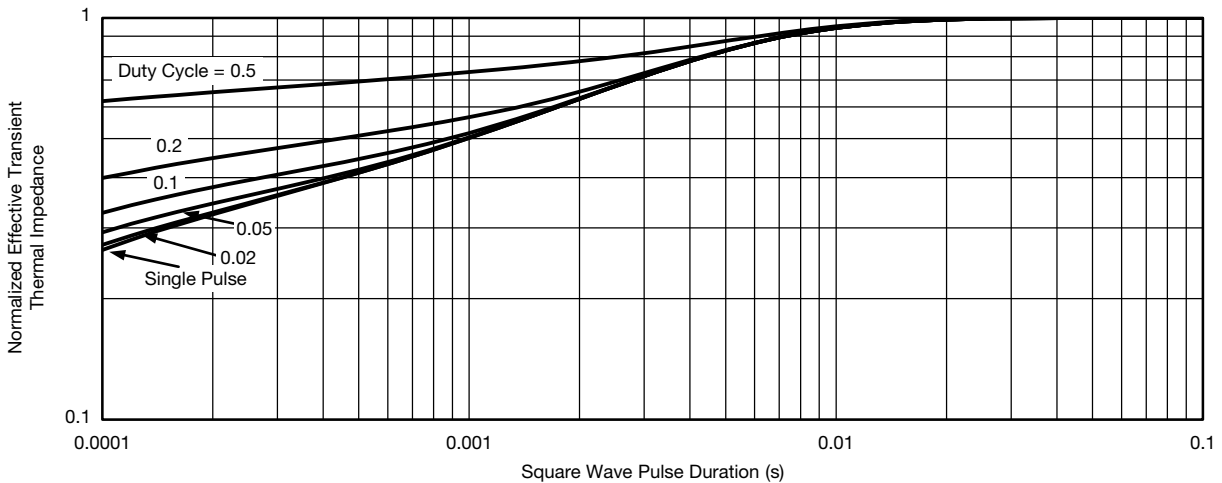
\* The power dissipation P<sub>D</sub> is based on T<sub>J(max)</sub> = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

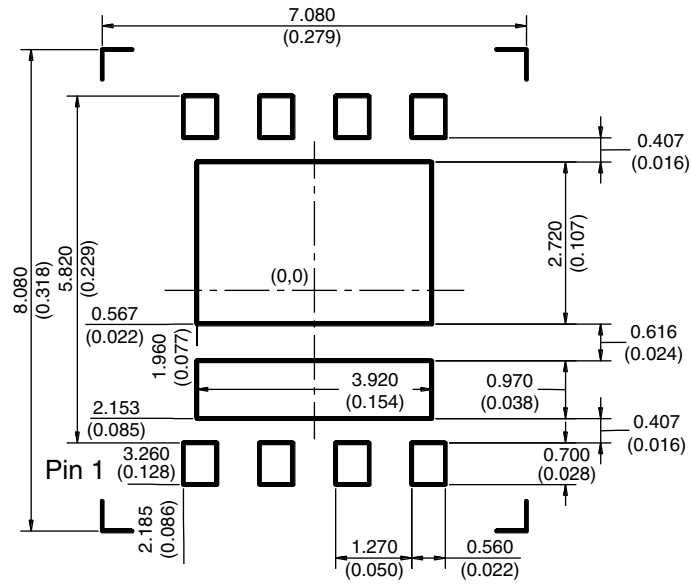
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## PowerPAIR® 6 x 5 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.10	0.000	-	0.004
A3	0.15	0.20	0.25	0.006	0.007	0.009
b	0.43	0.51	0.61	0.017	0.020	0.024
b1	0.25 BSC			0.010 BSC		
D	4.90	5.00	5.10	0.192	0.196	0.200
D1	3.75	3.80	3.85	0.148	0.150	0.152
E	5.90	6.00	6.10	0.232	0.236	0.240
E1 Option AA (for W/B)	2.62	2.67	2.72	0.103	0.105	0.107
E1 Option AB (for BWL)	2.42	2.47	2.52	0.095	0.097	0.099
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.005 BSC		
K Option AA (for W/B)	0.45 typ.			0.018 typ.		
K Option AB (for BWL)	0.65 typ.			0.025 typ.		
K1	0.66 typ.			0.025 typ.		
L	0.33	0.43	0.53	0.013	0.017	0.020
L3	0.23 BSC			0.009 BSC		
z	0.34 BSC			0.013 BSC		
ECN: T13-0354-Rev. B, 20-May-13						
DWG: 6005						

**RECOMMENDED MINIMUM PAD FOR PowerPAIR® 6 x 5**



Recommended Minimum Pad  
Dimensions in mm (inches)



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