# EN55022B Compliant 36V, 2A DC/DC µModule Regulator

## FEATURES

- **Complete Step-Down Switch Mode Power Supply**
- **Wide Input Voltage Range: 3.6V to 36V**
- **2A Output Current**
- **0.8V to 10V Output Voltage**
- **Selectable Switching Frequency: 200kHz to 2.4MHz**
- **EN55022 Class B Compliant**
- Current Mode Control
- Programmable Soft-Start
- SnPb (BGA) or RoHS Compliant (LGA and BGA) Finish
- Low Profile, Surface Mount LGA (9mm × 15mm × 2.82mm) and BGA (9mm × 15mm × 3.42mm) Packages

## APPLICATIONS

- Automotive Battery Regulation
- Power for Portable Products
- Distributed Supply Regulation
- Industrial Supplies
- Wall Transformer Regulation

## DESCRIPTION

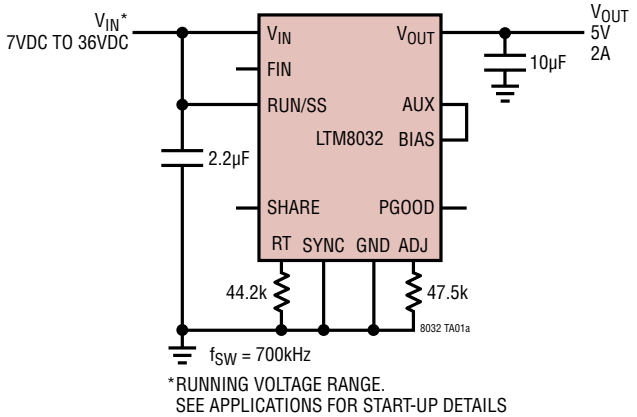
The LTM®8032 is an electromagnetic compatible (EMC) 36V, 2A DC/DC step-down µModule® regulator designed to meet the radiated emissions requirements of EN55022. Conducted emission requirements can be met by adding standard filter components. Included in the package are the switching controller, power switches, inductor, filters and all support components. Operating over an input voltage range of 3.6V to 36V, the LTM8032 supports an output voltage range of 0.8V to 10V, and a switching frequency range of 200kHz to 2.4MHz, each set by a single resistor. Only the bulk input and output filter capacitors are needed to finish the design. The low profile package enables utilization of unused space on the bottom of PC boards for high density point of load regulation.

The LTM8032 is packaged in a thermally enhanced, compact and low profile overmolded land grid array (LGA) and ball grid array (BGA) packages suitable for automated assembly by standard surface mount equipment. The LTM8032 is available with SnPb (BGA) or RoHS compliant terminal finish.



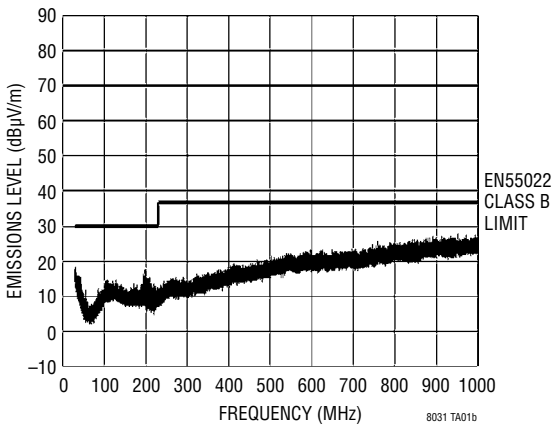
## TYPICAL APPLICATION

**Ultralow Noise 5V/2A DC/DC µModule Regulator**




*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

**LTM8032 EMI Performance**



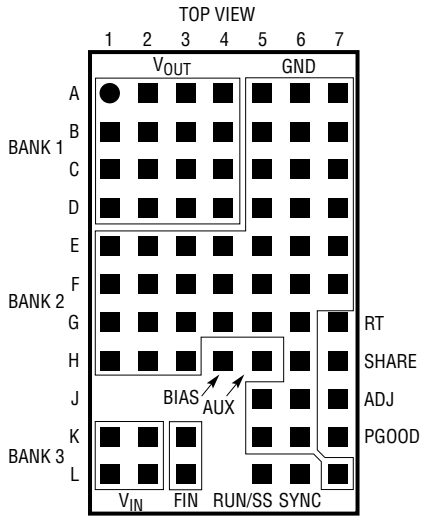
## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$, FIN, RUN/SS Voltage .....40V
ADJ, RT, SHARE Voltage.....5V
$V_{OUT}$, AUX.....10V
Current from AUX .....100mA

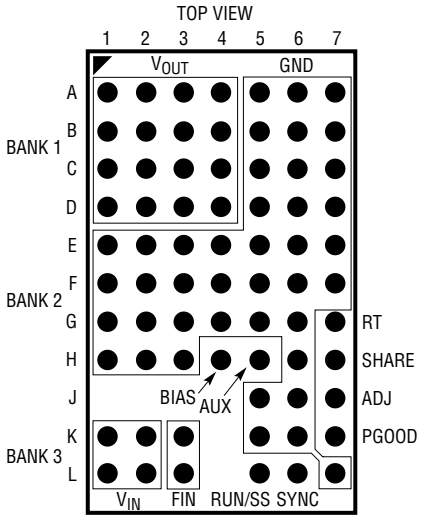
PGOOD, SYNC.....30V
BIAS.....25V
$V_{IN}$ + BIAS.....56V
Maximum Junction Temperature (Note 2) ..... 125°C
Solder Temperature..... 245°C

## PIN CONFIGURATION




LGA PACKAGE
71-LEAD (9mm × 15mm × 2.82mm)

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 25.2°C/W, $\theta_{JCbottom}$ = 10.3°C/W, $\theta_{JCtop}$ = 15.8°C/W, $\theta_{JB}$ = 11.4°C/W, WEIGHT = 1.2g
θ VALUES DETERMINED PER JESD51-9




BGA PACKAGE
71-LEAD (9mm × 15mm × 3.42mm)

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 25.6°C/W, $\theta_{JCbottom}$ = 11.0°C/W, $\theta_{JCtop}$ = 15.8°C/W, $\theta_{JB}$ = 11.4°C/W, WEIGHT = 1.2g
θ VALUES DETERMINED PER JEDEC 51-9, 51-12

## ORDER INFORMATION

| PART NUMBER | PAD OR BALL FINISH | PART MARKING* | | PACKAGE TYPE | MSL RATING | TEMPERATURE RANGE (Note 2) |
|---|---|---|---|---|---|---|
| | | DEVICE | CODE | | | |
| LTM8032EV#PBF | Au (RoHS) | LTM8032V | e4 | LGA | 3 | –40°C to 125°C |
| LTM8032IV#PBF | Au (RoHS) | LTM8032V | e4 | LGA | 3 | –40°C to 125°C |
| LTM8032MPV#PBF | Au (RoHS) | LTM8032MPV | e4 | LGA | 3 | –55°C to 125°C |
| LTM8032EY#PBF | SAC305 (RoHS) | LTM8032Y | e1 | BGA | 3 | –40°C to 125°C |
| LTM8032IY#PBF | SAC305 (RoHS) | LTM8032Y | e1 | BGA | 3 | –40°C to 125°C |
| LTM8032MPY#PBF | SAC305 (RoHS) | LTM8032Y | e1 | BGA | 3 | –55°C to 125°C |
| LTM8032MPY | SnPb (63/37) | LTM8032Y | e0 | BGA | 3 | –55°C to 125°C |

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Pb-free and Non-Pb-free Part Markings: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 10V, $V_{RUN/SS}$ = 10V, $V_{BIAS}$ = 3V, unless otherwise specified.**

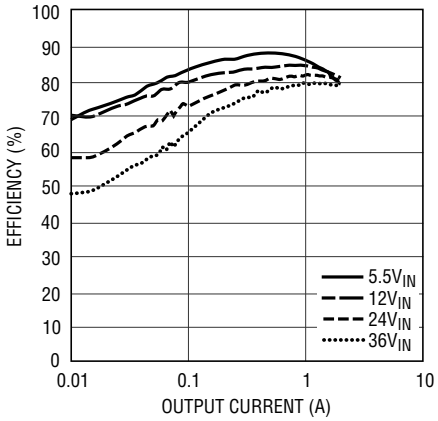
| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input DC Voltage | | ● | 3.6 | | 36 | V |
| $V_{OUT}$ | Output DC Voltage | 0.2A < $I_{OUT}$ ≤ 2A, $R_{ADJ}$ Open<br>0.2A < $I_{OUT}$ ≤ 2A, $R_{ADJ}$ = 21.6k | | | 0.8<br>10 | | V<br>V |
| $I_{OUT}$ | Continuous Output DC Current | $V_{IN}$ = 24V | | | | 2 | A |
| $I_{Q(VIN)}$ | $V_{IN}$ Quiescent Current | $V_{RUN/SS}$ = 0.2V<br>$V_{BIAS}$ = 3V, Not Switching<br>$V_{BIAS}$ = 0V, Not Switching | <br>●<br> | | 0.6<br>25<br>88 | <br>60<br>120 | µA<br>µA<br>µA |
| $I_{Q(BIAS)}$ | BIAS Quiescent Current | $V_{RUN/SS}$ = 0.2V<br>$V_{BIAS}$ = 3V, Not Switching<br>$V_{BIAS}$ = 0V, Not Switching | <br>●<br> | | 0.03<br>60<br>1 | <br>120<br>5 | µA<br>µA<br>µA |
| $\frac{\Delta V_{OUT}}{V_{OUT}}$ | Line Regulation | 10V ≤ $V_{IN}$ ≤ 36V, $I_{OUT}$ = 1A, $V_{OUT}$ = 3.3V | | | 0.1 | | % |
| | Load Regulation | $V_{IN}$ = 24V, 0.2A ≤ $I_{OUT}$ ≤ 2A, $V_{OUT}$ = 3.3V | | | 0.3 | | % |
| $V_{OUT(AC\_RMS)}$ | Output Ripple (RMS) | $V_{IN}$ = 24V, $I_{OUT}$ = 2A, $V_{OUT}$ = 3.3V | | | 6 | | mV |
| $f_{SW}$ | Switching Frequency | $R_T$ = 113k | | | 325 | | kHz |
| $V_{ADJ}$ | Voltage at ADJ Pin | | ● | 765 | 790 | 815 | mV |
| $V_{BIAS(MIN)}$ | Minimum BIAS Voltage for Proper Operation | | | | 1.9 | 2.8 | V |
| $I_{ADJ}$ | Current Out of ADJ Pin | $V_{RUN/SS}$ = 0V, $V_{ADJ}$ = 0V, $V_{OUT}$ = 1V | | | 4 | | µA |
| $I_{RUN/SS}$ | RUN/SS Pin Current | $V_{RUN/SS}$ = 2.5V | | | 5 | 10 | µA |
| $V_{IH(RUN/SS)}$ | RUN/SS Input High Voltage | | | 2.5 | | | V |
| $V_{IL(RUN/SS)}$ | RUN/SS Input Low Voltage | | | | | 0.2 | V |
| $V_{PG(TH)}$ | ADJ Voltage Threshold for PGOOD to Switch | | | | 730 | | mV |
| $I_{PGO}$ | PGOOD Leakage | $V_{PG}$ = 30V | | | 0.1 | 1 | µA |
| $I_{PGSINK}$ | PGOOD Sink Current | $V_{PG}$ = 0.4V | | 200 | 800 | | µA |
| $V_{SYNCIL}$ | SYNC Input Low Threshold | $f_{SYNC}$ = 550kHz | | | | 0.5 | V |
| $V_{SYNCIH}$ | SYNC Input High Threshold | $f_{SYNC}$ = 550kHz | | 0.7 | | | V |
| $I_{SYNC(BIAS)}$ | SYNC Pin Bias Current | $V_{SYNC}$ = 0V, $V_{BIAS}$ = 0V | | | 0.1 | | µA |
| $V_{IN(RIPPLE)}$ | 550kHz Narrowband Conducted Emission<br>1MHz Narrowband Conducted Emission<br>3MHz Narrowband Conducted Emission | $V_{IN}$ = 24V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 2A, $f_{SW}$ = 550kHz, 5µH LISN | | | 89<br>69<br>51 | | dBµV<br>dBµV<br>dBµV |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

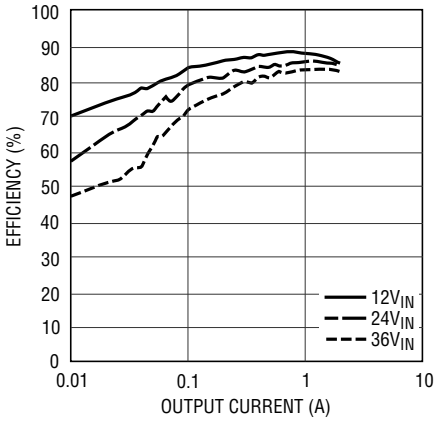
**Note 2:** The LTM8032E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the –40°C to 125°C internal temperature range are assured by design, characterization and correlation with statistical process controls. LTM8032I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8032MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

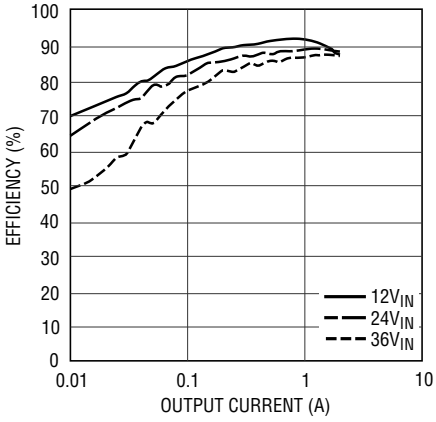
### 3.3$V_{OUT}$ Efficiency



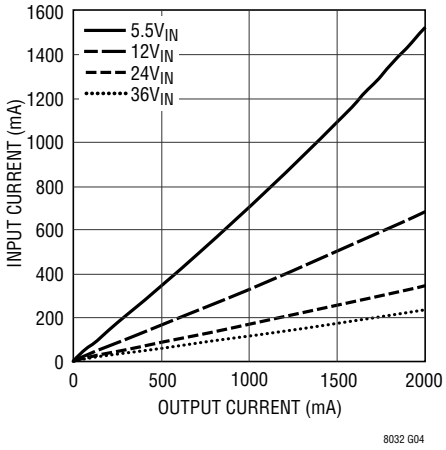

### 5$V_{OUT}$ Efficiency



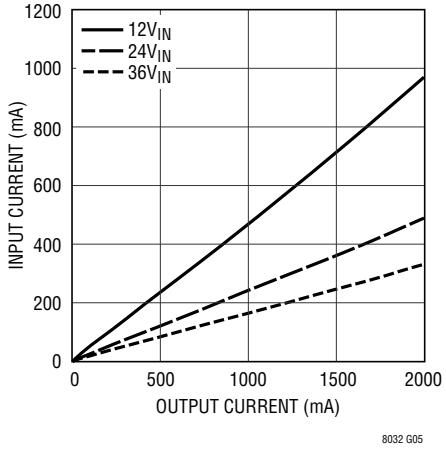

### 8$V_{OUT}$ Efficiency



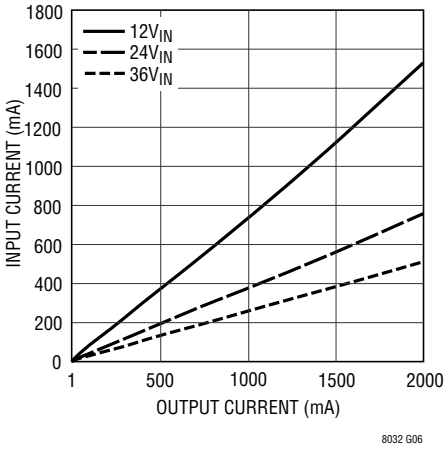

### Input Current vs Output Current, 3.3$V_{OUT}$



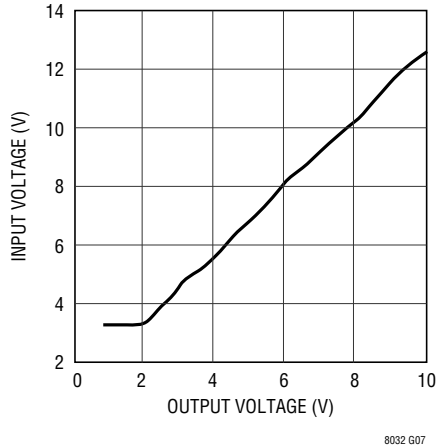

### Input Current vs Output Current, 5$V_{OUT}$



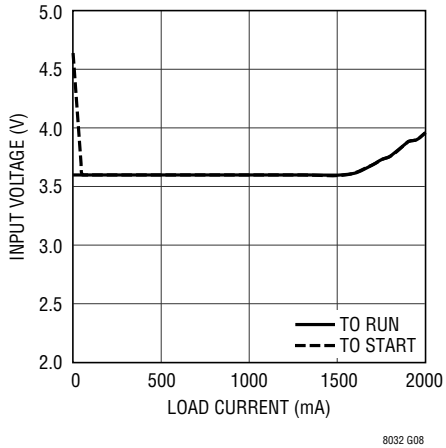

### Input Current vs Output Current, 8$V_{OUT}$



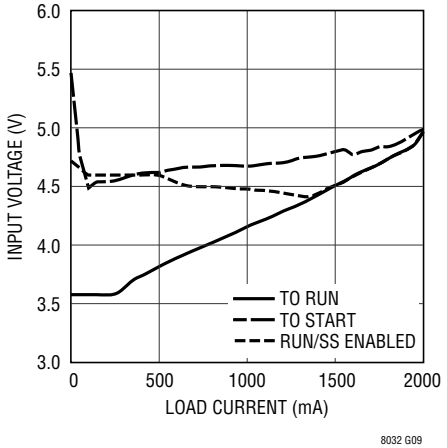

### Minimum Required Input Voltage vs Output Voltage, $I_{OUT}$ = 2A




### Minimum Required Input Voltage vs Load Current, $V_{OUT}$ = 2.5V

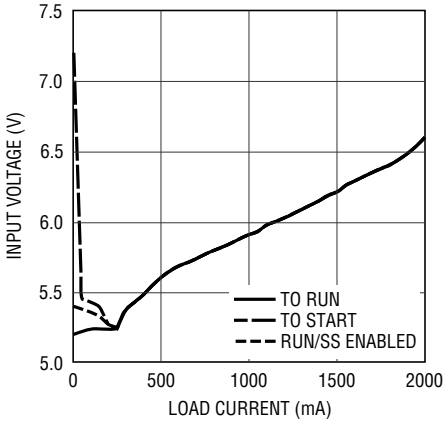



### Minimum Required Input Voltage vs Load Current, $V_{OUT}$ = 3.3V

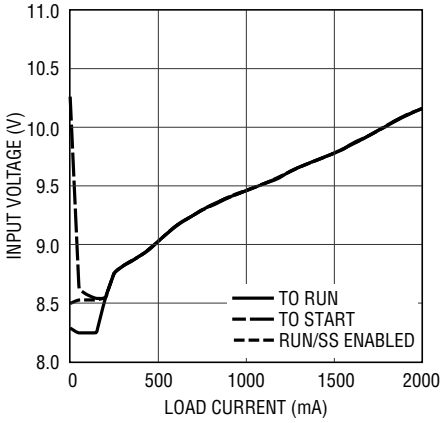


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

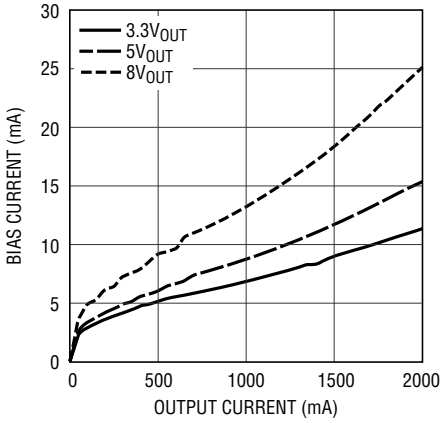
**Minimum Required Input Voltage vs Load Current, $V_{OUT}$ = 5V**



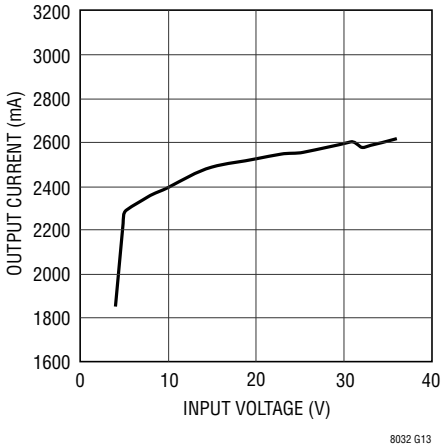

**Minimum Required Input Voltage vs Load Current, $V_{OUT}$ = 8V**



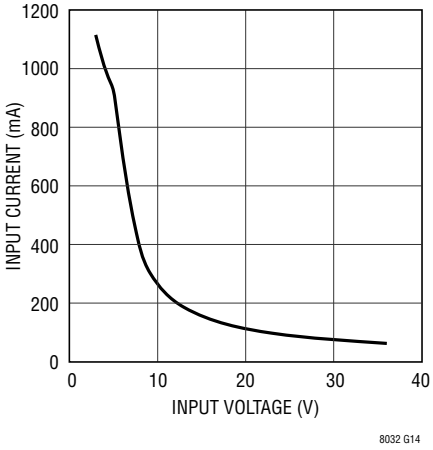

**Bias Current vs Output Current**



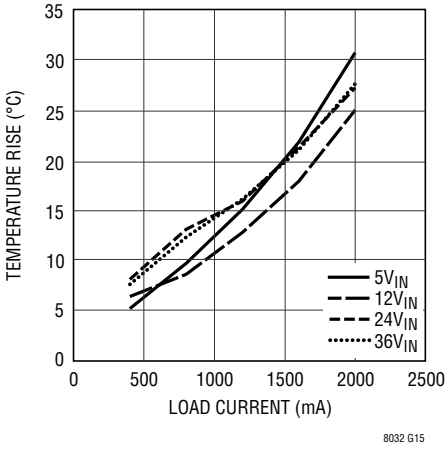

**Output Current vs Input Voltage (Output Shorted)**



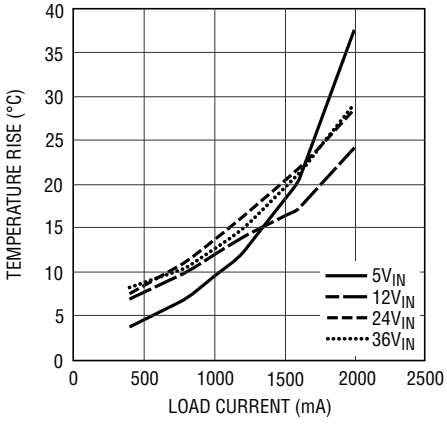

**Input Current vs Input Voltage (Output Shorted)**



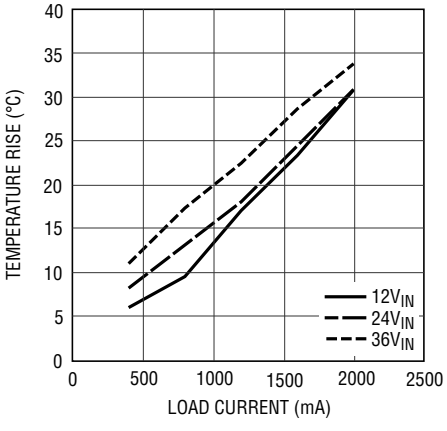

**Temperature Rise vs Load Current, $V_{OUT}$ = 2.5V (LGA)**



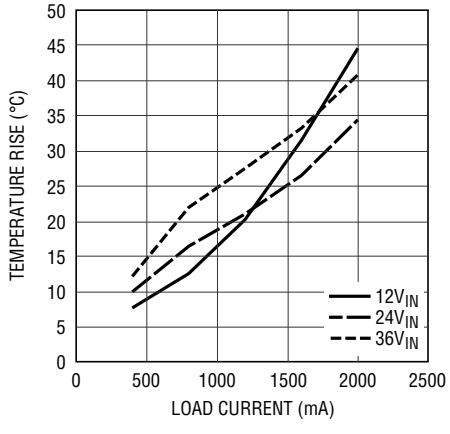

**Temperature Rise vs Load Current, $V_{OUT}$ = 3.3V (LGA)**




**Temperature Rise vs Load Current, $V_{OUT}$ = 5V (LGA)**

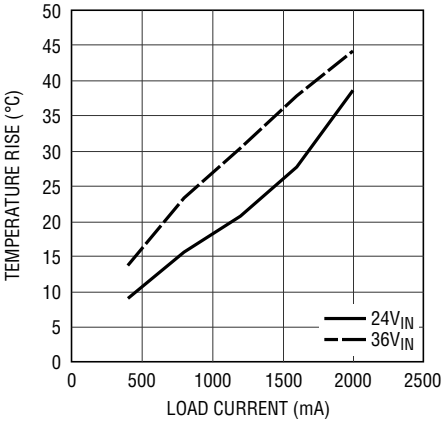



**Temperature Rise vs Load Current, $V_{OUT}$ = 8V (LGA)**

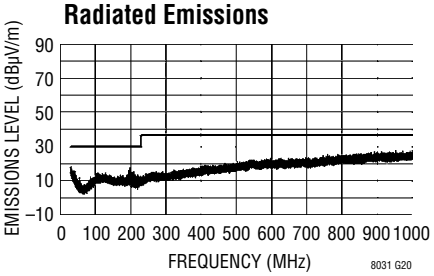


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

**Temperature Rise vs Load Current, $V_{OUT}$ = 10V (LGA)**

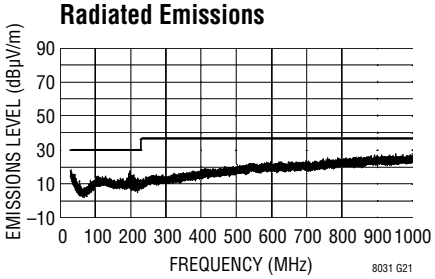



**Radiated Emissions**



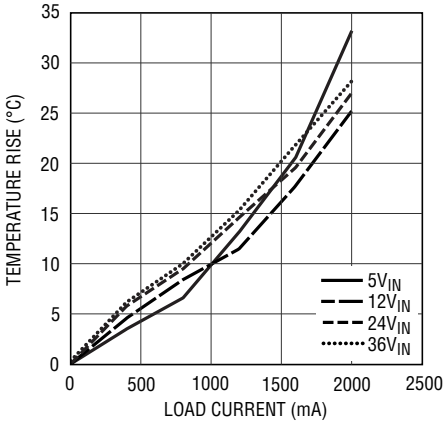

$V_{IN}$ = 36V
$V_{OUT}$ = 10V AT 2A

**Radiated Emissions**

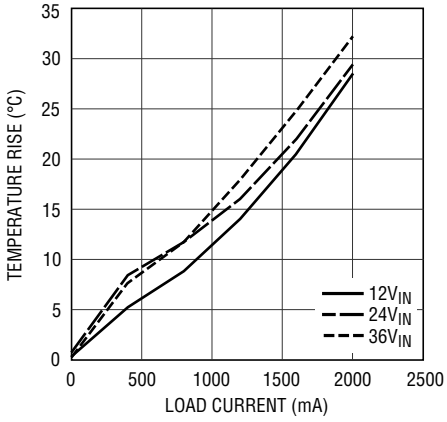



$V_{IN}$ = 13V
$V_{OUT}$ = 10V AT 2A

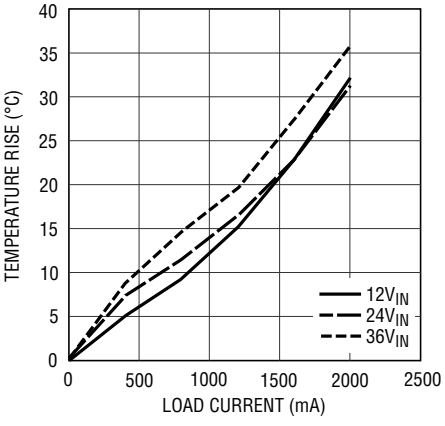
**Temperature Rise vs Load Current, $V_{OUT}$ = 2.5V (BGA)**



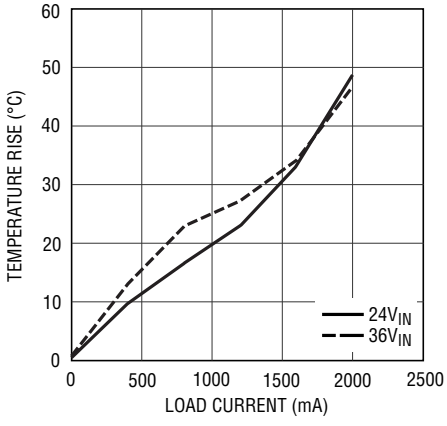

**Temperature Rise vs Load Current, $V_{OUT}$ = 3.3V (BGA)**




**Temperature Rise vs Load Current, $V_{OUT}$ = 5V (BGA)**




**Temperature Rise vs Load Current, $V_{OUT}$ = 10V (BGA)**



## PIN FUNCTIONS

**$V_{IN}$ (Bank 3):** The $V_{IN}$ pin supplies current to the LTM8032's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor of at least 2.2µF.

**FIN (K3, L3):** Filtered Input. This is the node after the input EMI filter. Use this only if there is a need to modify the behavior of the integrated EMI filter or if $V_{IN}$ rises or falls rapidly; otherwise, leave these pins unconnected. See the Applications Information section for more details.

**GND (Bank 2):** Tie these GND pins to a local ground plane below the LTM8032 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8032 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider ($R_{ADJ}$) to this net.

**$V_{OUT}$ (Bank 1):** Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

**AUX (Pin H5):** Low Current Voltage Source for BIAS. The AUX pin is internally connected to $V_{OUT}$ and is placed adjacent to the BIAS pin to ease printed circuit board routing. Although this pin is internally connected to $V_{OUT}$, **do not** connect this pin to the load. If this pin is not tied to BIAS, leave it floating.

**BIAS (Pin H4):** The BIAS pin connects to the internal power bus. Connect to a power source greater than 2.8V. If the output is greater than 2.8V, connect this pin to AUX. If the output voltage is less, connect this to a voltage source between 2.8V and 25V. Also, make sure that BIAS + $V_{IN}$ is less than 56V.

**RUN/SS (Pin L5):** Pull RUN/SS pin to less than 0.2V to shut down the LTM8032. Tie to 2.5V or more for normal operation. If the shutdown feature is not used, tie this pin to the $V_{IN}$ pin. RUN/SS also provides a soft-start function; see the Applications Information section.

**RT (Pin G7):** The RT pin is used to program the switching frequency of the LTM8032 by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin.

**SHARE (Pin H7):** Tie this to the SHARE pin of another LTM8032 when paralleling the outputs. Otherwise, do not connect (leave floating).

**SYNC (Pin L6):** This is the external clock synchronization input. Ground this pin for low ripple Burst Mode® operation at low output loads. Tie to a stable voltage source greater than 0.7V to disable Burst Mode operation. Do not leave this pin floating. Tie to a clock source for synchronization. Clock edges should have rise and fall times faster than 1µs. See synchronization section in Applications Information.

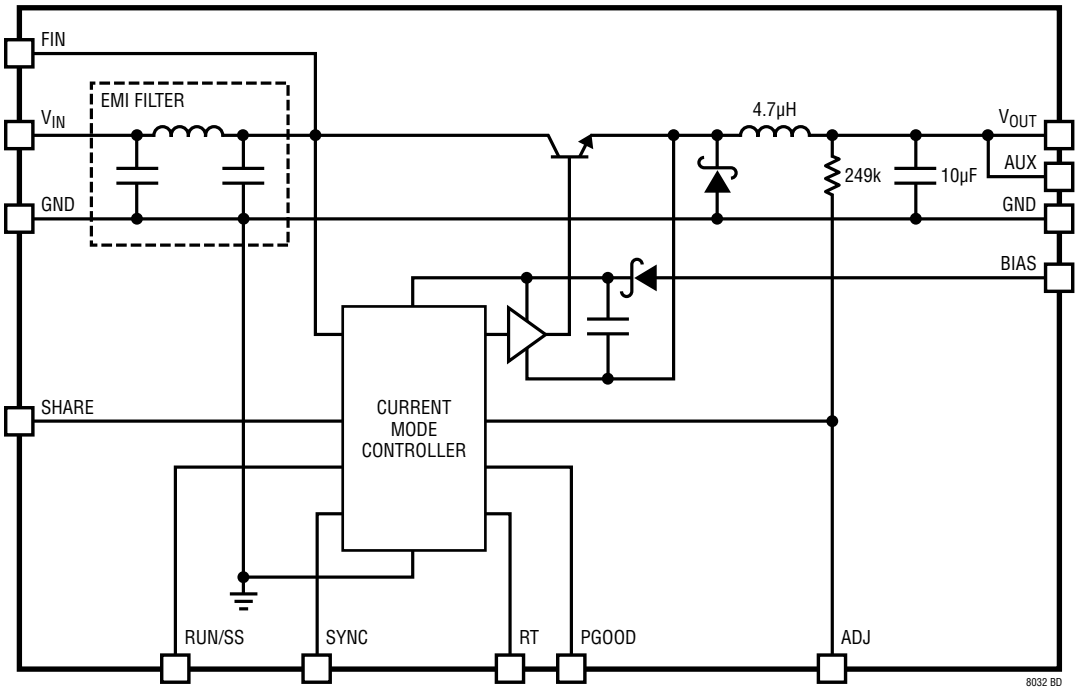
**PGOOD (Pin K7):** The PGOOD pin is the open-collector output of an internal comparator. PGOOD remains low until the ADJ pin is within 10% of the final regulation voltage. The PGOOD output is valid when $V_{IN}$ is above 3.6V and RUN/SS is high. If this function is not used, leave this pin floating.

**ADJ (Pin J7):** The LTM8032 regulates its ADJ pin to 0.79V. Connect the adjust resistor from this pin to ground. The value of $R_{ADJ}$ is given by the equation:

$$R_{ADJ} = \frac{196.71}{V_{OUT} - 0.79}$$

where $R_{ADJ}$ is in kΩ.

## BLOCK DIAGRAM



## OPERATION

The LTM8032 is a standalone nonisolated step-down switching DC/DC power supply. It can deliver up to 2A of DC output current with only bulk external input and output capacitors. This module provides a precisely regulated output voltage programmable via one external resistor from 0.8VDC to 10VDC. The input voltage range is 3.6V to 36V. Given that the LTM8032 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. A simplified Block Diagram is given on the previous page.

The LTM8032 is designed with an input EMI filter and other features to make its radiated emissions compliant with several EMC specifications including EN55022 class B. Compliance with conducted emissions requirements may be obtained by adding a standard input filter.

The LTM8032 contains a current mode controller, power switching element, power inductor, power Schottky diode and a modest amount of input and output capacitance. The LTM8032 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to GND.

An internal regulator provides power to the control circuitry. The bias regulator can draw power from the $V_{IN}$ pin, but if the BIAS pin is connected to an external voltage higher than 2.8V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN/SS pin is used to place the LTM8032 in shutdown, disconnecting the output and reducing the input current to less than 1µA.

To further optimize efficiency, the LTM8032 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 50µA in a typical application. The oscillator reduces the LTM8032's operating frequency when the voltage at the ADJ pin is low. This frequency foldback helps to control the output current during start-up and overload.

The LTM8032 contains a power good comparator which trips when the ADJ pin is at 90% of its regulated value. The PGOOD output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PGOOD pin high. Power good is valid when the LTM8032 is enabled and $V_{IN}$ is above 3.6V.

## APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended $C_{IN}$, $C_{OUT}$, $R_{ADJ}$ and $R_T$ values.
3. Connect BIAS as indicated.

As the integrated input EMI filter may ring in response to an application of a step input voltage, a bulk capacitance, series resistance or some clamping mechanism may be required. See the Hot-Plugging Safely section for details.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

### Capacitor Selection Considerations

The $C_{IN}$ and $C_{OUT}$ capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application

## APPLICATIONS INFORMATION

**Table 1. Recommended Component Values and Configuration**

| $V_{IN}$ | $V_{OUT}$ | $C_{IN}$ | $C_{OUT}$ | $R_{ADJ}$ | BIAS | $f_{OPTIMAL}$ | $R_{T(OPTIMAL)}$ | $f_{MAX}$ | $R_{T(MIN)}$ |
|---|---|---|---|---|---|---|---|---|---|
| 3.6V to 36V | 0.82V | 2.2µF | 200µF 1206 | 5.62M | ≥2.8V, <25V | 250k | 150k | 250k | 150k |
| 3.6V to 36V | 1.00V | 2.2µF | 200µF 1206 | 953k | ≥2.8V, <25V | 300k | 124k | 300k | 124k |
| 3.6V to 36V | 1.20V | 2.2µF | 147µF 1206 | 487k | ≥2.8V, <25V | 350k | 105k | 350k | 105k |
| 3.6V to 36V | 1.50V | 2.2µF | 147µF 1206 | 280k | ≥2.8V, <25V | 400k | 88.7k | 400k | 88.7k |
| 3.6V to 36V | 1.80V | 2.2µF | 100µF 1206 | 196k | ≥2.8V, <25V | 450k | 78.7k | 450k | 78.7k |
| 3.6V to 36V | 2.00V | 2.2µF | 68µF 1206 | 165k | ≥2.8V, <25V | 450k | 78.7k | 450k | 78.7k |
| 4.0V to 36V | 2.20V | 2.2µF | 68µF 1206 | 140k | ≥2.8V, <25V | 500k | 69.8k | 500k | 69.8k |
| 4.3V to 36V | 2.50V | 2.2µF | 47µF 1206 | 115k | ≥2.8V, <25V | 550k | 61.9k | 600k | 54.9k |
| 5.5V to 36V | 3.30V | 2.2µF | 22µF 1206 | 78.7k | AUX | 600k | 54.9k | 700k | 44.2k |
| 7V to 36V | 5.00V | 2.2µF | 10µF 1206 | 47.5k | AUX | 700k | 44.2k | 1M | 29.4k |
| 10.5V to 36V | 8.00V | 2.2µF | 10µF 1206 | 27.4k | AUX | 800k | 39.2k | 1.5M | 16.2k |
| 3.6V to 15V | 0.82V | 2.2µF | 200µF 1206 | 5.62M | $V_{IN}$ | 250k | 150k | 600k | 54.9k |
| 3.6V to 15V | 1.00V | 2.2µF | 200µF 1206 | 953k | $V_{IN}$ | 300k | 124k | 700k | 44.2k |
| 3.6V to 15V | 1.20V | 2.2µF | 147µF 1206 | 487k | $V_{IN}$ | 350k | 105k | 800k | 39.2k |
| 3.6V to 15V | 1.50V | 2.2µF | 147µF 1206 | 280k | $V_{IN}$ | 400k | 88.7k | 900k | 34.0k |
| 3.6V to 15V | 1.80V | 2.2µF | 100µF 1206 | 196k | $V_{IN}$ | 450k | 78.7k | 1M | 29.4k |
| 3.6V to 15V | 2.00V | 2.2µF | 68µF 1206 | 165k | $V_{IN}$ | 450k | 78.7k | 1.1M | 26.1k |
| 4.0V to 15V | 2.20V | 2.2µF | 68µF 1206 | 140k | $V_{IN}$ | 500k | 69.8k | 1.25M | 22.1k |
| 4.3V to 15V | 2.50V | 2.2µF | 47µF 1206 | 115k | $V_{IN}$ | 550k | 61.9k | 1.3M | 21.0k |
| 5.5V to 15V | 3.30V | 2.2µF | 22µF 1206 | 78.7k | AUX | 600k | 54.9k | 1.7M | 14.0k |
| 7V to 15V | 5.00V | 2.2µF | 10µF 1206 | 47.5k | AUX | 700k | 44.2k | 2M | 10.0k |
| 9V to 24V | 0.82V | 2.2µF | 200µF 1206 | 5.62M | ≥2.8V, <25V | 250k | 150k | 400k | 88.7k |
| 9V to 24V | 1.00V | 2.2µF | 200µF 1206 | 953k | ≥2.8V, <25V | 300k | 124k | 450k | 79.0k |
| 9V to 24V | 1.20V | 2.2µF | 147µF 1206 | 487k | ≥2.8V, <25V | 350k | 105k | 500k | 69.8k |
| 9V to 24V | 1.50V | 2.2µF | 147µF 1206 | 280k | ≥2.8V, <25V | 400k | 88.7k | 550k | 61.9k |
| 9V to 24V | 1.80V | 2.2µF | 100µF 1206 | 196k | ≥2.8V, <25V | 450k | 78.7k | 650k | 49.9k |
| 9V to 24V | 2.00V | 2.2µF | 68µF 1206 | 165k | ≥2.8V, <25V | 450k | 78.7k | 700k | 44.2k |
| 9V to 24V | 2.20V | 2.2µF | 47µF 1206 | 140k | ≥2.8V, <25V | 500k | 69.8k | 750k | 42.2k |
| 9V to 24V | 2.50V | 2.2µF | 22µF 1206 | 115k | ≥2.8V, <25V | 550k | 61.9k | 800k | 39.2k |
| 9V to 24V | 3.30V | 2.2µF | 22µF 1206 | 78.7k | AUX | 600k | 54.9k | 1M | 29.4k |
| 9V to 24V | 5.00V | 2.2µF | 10µF 1206 | 47.5k | AUX | 700k | 44.2k | 1.5M | 16.2k |
| 10.5V to 24V | 8.00V | 2.2µF | 10µF 1206 | 27.4k | AUX | 800k | 39.2k | 1.5M | 16.2k |
| 13V to 24V | 10.00V | 2.2µF | 10µF 1206 | 21.5k | AUX | 900k | 34.0k | 1.3M | 21.0k |
| 18V to 36V | 0.82V | 2.2µF | 200µF 1206 | 5.62M | ≥2.8V, <25V | 250k | 150k | 250k | 150k |
| 18V to 36V | 1.00V | 2.2µF | 200µF 1206 | 953k | ≥2.8V, <25V | 300k | 124k | 300k | 124k |
| 18V to 36V | 1.20V | 2.2µF | 147µF 1206 | 487k | ≥2.8V, <25V | 350k | 105k | 350k | 105k |
| 18V to 36V | 1.50V | 2.2µF | 147µF 1206 | 280k | ≥2.8V, <25V | 400k | 88.7k | 400k | 88.7k |
| 18V to 36V | 1.80V | 2.2µF | 100µF 1206 | 196k | ≥2.8V, <25V | 450k | 78.7k | 450k | 78.7k |
| 18V to 36V | 2.00V | 2.2µF | 68µF 1206 | 165k | ≥2.8V, <25V | 450k | 78.7k | 450k | 78.7k |
| 18V to 36V | 2.20V | 2.2µF | 47µF 1206 | 140k | ≥2.8V, <25V | 500k | 69.8k | 500k | 69.8k |
| 18V to 36V | 2.50V | 2.2µF | 22µF 1206 | 115k | ≥2.8V, <25V | 550k | 61.9k | 600k | 54.9k |
| 18V to 36V | 3.30V | 2.2µF | 22µF 1206 | 78.7k | AUX | 600k | 54.9k | 700k | 44.2k |
| 18V to 36V | 5.00V | 2.2µF | 10µF 1206 | 47.5k | AUX | 700k | 44.2k | 1M | 29.4k |
| 18V to 36V | 8.00V | 2.2µF | 10µF 1206 | 27.4k | AUX | 800k | 39.2k | 1.5M | 16.2k |
| 18V to 36V | 10.00V | 2.2µF | 10µF 1206 | 21.5k | AUX | 900k | 34.0k | 1.3M | 21.0k |

Note: An input bulk capacitor is required. 200µF is 2 × 100µF, 147 is 100µF||47µF

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circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected. Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8032's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8032 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. The input capacitor can be a parallel combination of a 2.2µF ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8032. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8032 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

### Electromagnetic Compliance

The LTM8032 is compliant with the radiated emissions requirements of EN55022 class B. Graphs of the LTM8032's EMC performance are given in the Typical Performance Characteristics section. Further data, operating conditions and test setup are detailed in an EMI Test report available from the Linear Technology website.

### Frequency Selection

The LTM8032 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.4MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of $R_T$ resistor values and their resultant frequencies.

### Operating Frequency Trade-Offs

It is recommended that the user apply the optimal $R_T$ value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8032 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8032 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output cap. The maximum frequency (and attendant $R_T$ value) at which the LTM8032 should be allowed to switch is given in Table 1 in the $f_{MAX}$ column, while the recommended frequency (and $R_T$ value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

**Table 2. Switching Frequency vs $R_T$ Value**

| SWITCHING FREQUENCY (MHz) | $R_T$ VALUE (kΩ) |
|---|---|
| 0.2 | 187 |
| 0.3 | 124 |
| 0.4 | 88.7 |
| 0.5 | 69.8 |
| 0.6 | 54.9 |
| 0.7 | 44.2 |
| 0.8 | 39.2 |
| 0.9 | 34 |
| 1.0 | 29.4 |
| 1.2 | 23.7 |
| 1.4 | 19.1 |
| 1.5 | 16.2 |
| 1.8 | 13.3 |
| 2 | 11.5 |
| 2.2 | 9.76 |
| 2.4 | 8.66 |

### BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate internal circuitry. For proper operation, it must be powered by at least 2.8V. If the output voltage is programmed to be 2.8V or higher, simply tie BIAS to AUX. If $V_{OUT}$ is less than 2.8V, BIAS can be tied to $V_{IN}$ or some other voltage source. In all cases, ensure that the maximum voltage at the BIAS pin is both less than 25V and the sum of $V_{IN}$ and BIAS is less

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than 56V. If BIAS power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the LTM8032.

### Load Sharing

Two or more LTM8032s may be paralleled to produce higher currents. This may, however, alter the EMI performance of the LTM8032s. To do this, tie the $V_{IN}$, ADJ, $V_{OUT}$ and SHARE pins of all the paralleled LTM8032s together. To ensure that paralleled modules start up together, the RUN/SS pins may be tied together, as well. Synchronize the LTM8032s to an external clock to eliminate beat frequencies, if required. If the RUN/SS pins are not tied together, make sure that the same valued soft-start capacitors are used for each module. An example of two LTM8032 modules configured for load sharing is given in the Typical Applications section.

For current sharing applications using multiple LTM8032s, the ADJ pins for all regulators may be combined using one resistor to ground as determined by:

$$R_{ADJ} = \frac{\frac{196.71}{N}}{V_{OUT} - 0.79}$$

where N is the number of paralleled modules and $R_{ADJ}$ is in kΩ.

### Burst Mode Operation

To enhance efficiency at light loads, the LTM8032 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8032 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. In addition, $V_{IN}$ and BIAS quiescent currents are reduced to typically 25µA and 60µA respectively during the sleep time. As the load current decreases towards a no-load condition, the percentage of time that the LTM8032 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher efficiency. Burst Mode operation is enabled by tying SYNC to GND.

To disable Burst Mode operation, tie SYNC to a stable voltage above 0.7V or synchronize to an external clock. Do not leave the SYNC pin floating.

### Minimum Input Voltage

The LTM8032 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. In addition, the input voltage required to turn on is higher than that required to run, and depends upon whether the RUN/SS is used. As shown in Figure 1, it takes only about $3.6V_{IN}$ for the LTM8032 to run a 3.3V output at light load. If RUN/SS is tied directly to $V_{IN}$, a 5.5V input voltage is required to start. If $V_{IN}$ is allowed to settle in the operating region first then the RUN/SS pin is enabled, the minimum input voltage to start at light load is lower, about 4.7V. A similar curve for $5V_{OUT}$ operation is also provided in Figure 1.

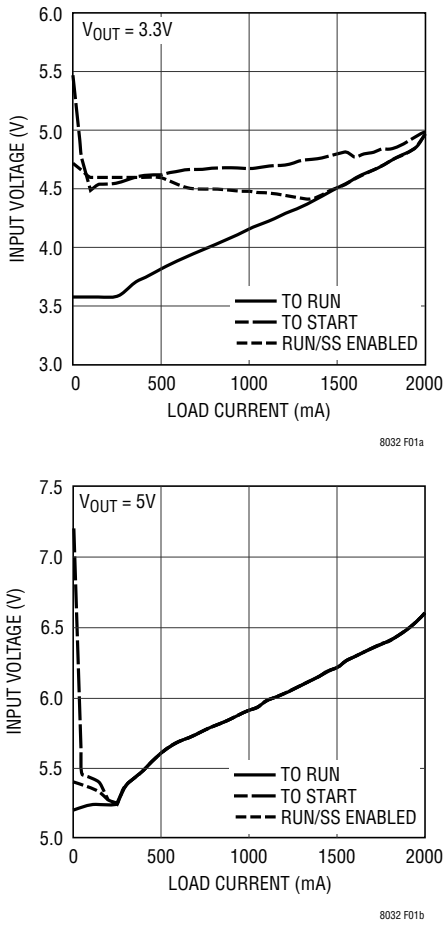


**Figure 1. The LTM8032 Needs More Voltage to Start Than Run**

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## Soft-Start

The RUN/SS pin can be used to soft-start the LTM8032, reducing the maximum input current during start-up. The RUN/SS pin is driven through an external RC network to create a voltage ramp at this pin. Figure 2 shows the start-up and shutdown waveforms with the soft-start circuit. By choosing an appropriate RC time constant, the peak start-up current can be reduced to the current that is required to regulate the output, with no overshoot. Choose the value of the resistor so that it can supply at least 20µA when the RUN/SS pin reaches 2.5V.

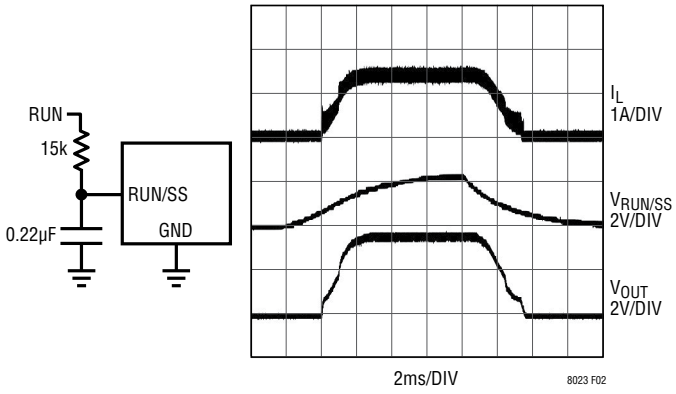


**Figure 2. To Soft-Start the LTM8032, Add a Resistor and Capacitor to the RUN/SS Pin**

## Synchronization

The internal oscillator of the LTM8032 can be synchronized by applying an external 250kHz to 2MHz clock to the SYNC pin. Do not leave this pin floating. The resistor tied from the RT pin to ground should be chosen such that the LTM8032 oscillates 20% lower than the intended synchronization frequency (see the Frequency Selection section). The LTM8032 will not enter Burst Mode operation while synchronized to an external clock, but will instead skip pulses to maintain regulation.

## Shorted Input Protection

Care needs to be taken in systems where the output will be held high when the input to the LTM8032 is absent. This may occur in battery charging applications or in battery back-up systems where a battery or some other supply is diode ORed with the LTM8032's output. If the $V_{IN}$ pin is allowed to float and the RUN/SS pin is held high (either by a logic signal or because it is tied to $V_{IN}$), then the LTM8032's internal circuitry will pull its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN/SS pin, the internal switch current will drop to essentially zero. However, if the $V_{IN}$ pin is grounded while the output is held high, then parasitic diodes inside the LTM8032 can pull large currents from the output through the $V_{IN}$ pin, potentially damaging the device. Figure 3 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

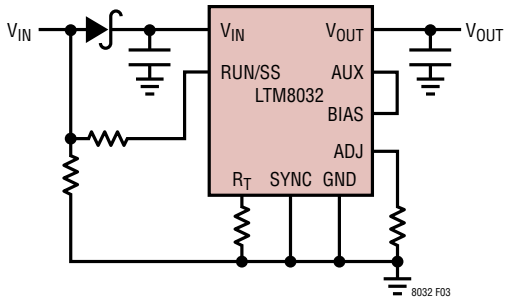


**Figure 3. The Input Diode Prevents a Shorted Input from Discharging a Back-Up Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8032 Runs Only When the Input is Present**

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### PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8032. The LTM8032 is nevertheless a switching power supply and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 4 for a suggested layout.

Ensure that the grounding and heat sinking are acceptable. A few rules to keep in mind are:

1. Place the $R_{ADJ}$ and $R_T$ resistors as close as possible to their respective pins.
2. Place the $C_{IN}$ capacitor as close as possible to the $V_{IN}$ and GND connection of the LTM8032. If a capacitor is connected to the FIN terminals, place it as close as possible to the FIN terminals, such that its ground connection is as close as possible to that of the $C_{IN}$ capacitor.
3. Place the $C_{OUT}$ capacitor as close as possible to the $V_{OUT}$ and GND connection of the LTM8032.
4. Place the $C_{IN}$ and $C_{OUT}$ capacitors such that their ground currents flow directly adjacent or underneath the LTM8032.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8032.
6. Use vias to connect the GND copper area to the board's internal ground plane. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board.

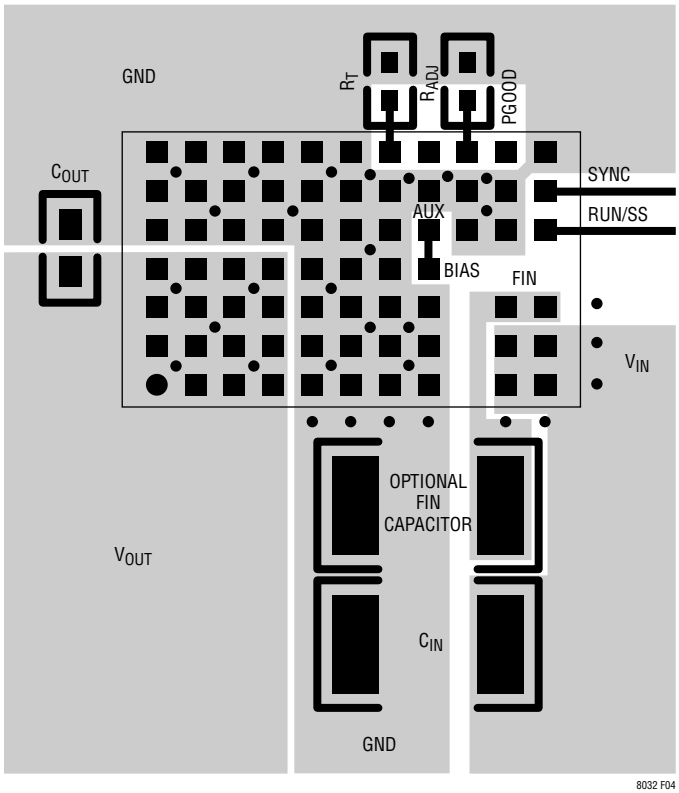


**Figure 4. Layout Showing Suggested External Components, GND Plane and Thermal Vias (LGA Package)**

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### Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8032. However, these capacitors can cause problems if the LTM8032 is plugged into a live or fast rising or falling supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an under-damped tank circuit, and the voltage at the $V_{IN}$ pin of the LTM8032 can ring to twice the nominal input voltage, possibly exceeding the LTM8032's rating and damaging the part. A similar phenomenon can occur inside the LTM8032 module, at the output of the integrated EMI filter, with the same potential of damaging the part.

If the input supply is poorly controlled or the user will be plugging the LTM8032 into an energized supply, the input network should be designed to prevent this overshoot. Figure 5 shows the waveforms that result when an LTM8032 circuit is connected to a 24V supply through six feet of 24-gauge twisted pair. The first plot (5a) is the response with a 2.2µF ceramic capacitor at the input. The input voltage rings as high as 35V and the input current peaks at 20A. One method of damping the tank circuit is to add another capacitor with a series resistor to the circuit. An alternative solution is shown in Figure 5b. A 0.7Ω resistor is added in series with the input to eliminate the voltage overshoot (it also reduces the peak input current). A 0.1µF capacitor improves high frequency filtering. For high input voltages its impact on efficiency is minor, reducing efficiency less than one-half percent for a 5V output at full load operating from 24V. By far the most popular method of controlling overshoot is shown in Figure 5c, where an aluminum electrolytic capacitor has been connected to FIN. This capacitor's high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit. Figure 5c shows the capacitor added to the $V_{IN}$ terminals, but placing the electrolytic capacitor at the FIN terminals can improve the LTM8032's EMI filtering as well as guard against overshoots caused by the Q of the integrated filter.

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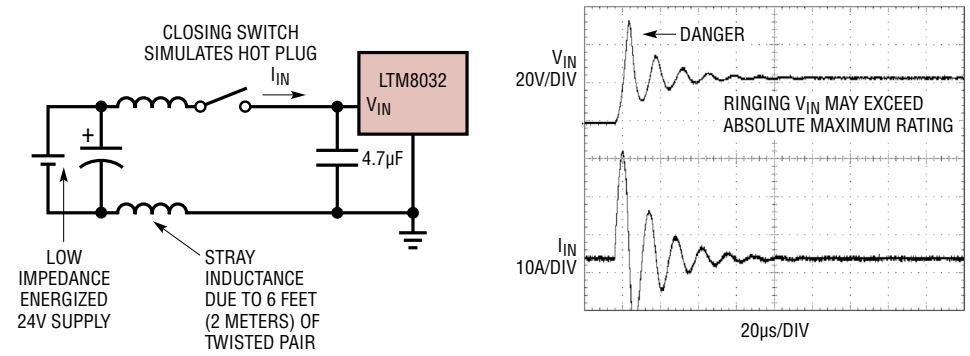
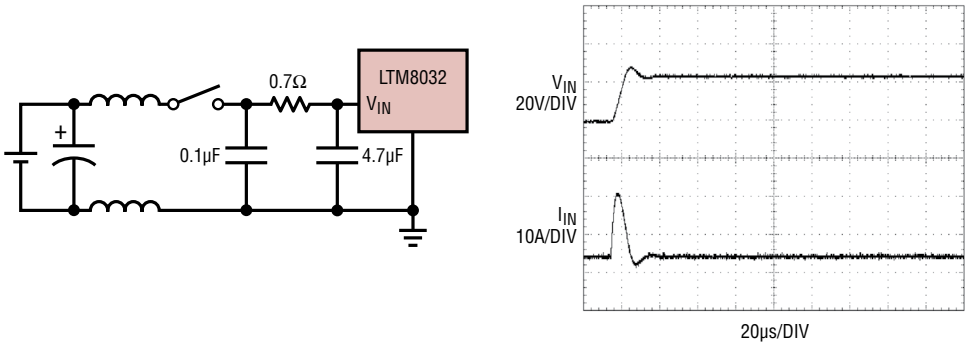
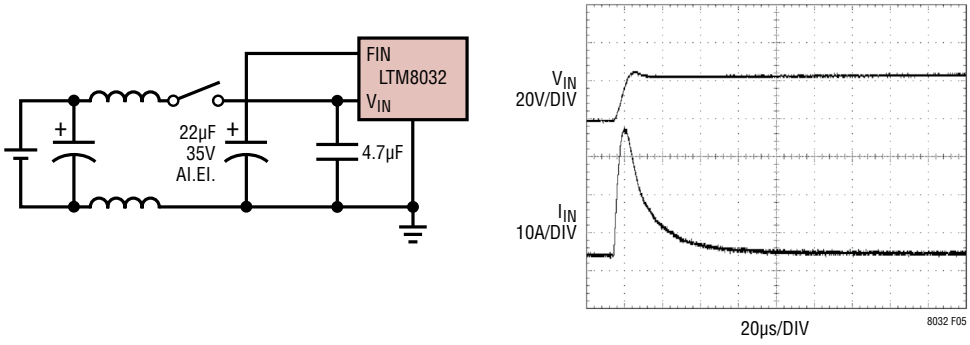



**(5a)**




**(5b)**




**(5c)**

**Figure 5. A Well Chosen Input Network Prevents Input Voltage Overshoot and Ensures Reliable Operation When the LTM8032 is Hot-Plugged to a Live Supply**

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### Thermal Considerations

The LTM8032 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by an LTM8032 mounted to a 36cm$^2$ 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The thermal resistance numbers listed in the Pin Configuration are based on modeling the µModule package mounted on a test board specified per JESD51-9 "Test Boards for Area Array Surface Mount Package Thermal Measurements." The thermal coefficients provided in this page are based on JESD 51-12 "Guidelines for Reporting and Using Electronic Package Thermal Information."

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, the Pin Configuration typically gives four thermal coefficients:

- $\theta_{JA}$ – Thermal resistance from junction to ambient.
- $\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case.
- $\theta_{JCtop}$ – Thermal resistance from junction to top of the product case.
- $\theta_{JB}$ – Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased in the following:

- $\theta_{JA}$ is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
- $\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
- $\theta_{JCtop}$ is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
- $\theta_{JB}$ is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

## APPLICATIONS INFORMATION

The most appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously. None of them can be individually used to accurately predict the thermal performance of the product, so it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature versus load graphs given in the LTM8032 data sheet.

A graphical representation of these thermal resistances is given in Figure 6.

The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM8032 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8032. The bulk of the heat flow out of the LTM8032 is through the bottom of the module and the pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

Finally, be aware that at high ambient temperatures the internal Schottky diode will have significant leakage current increasing the quiescent current of the LTM8032.

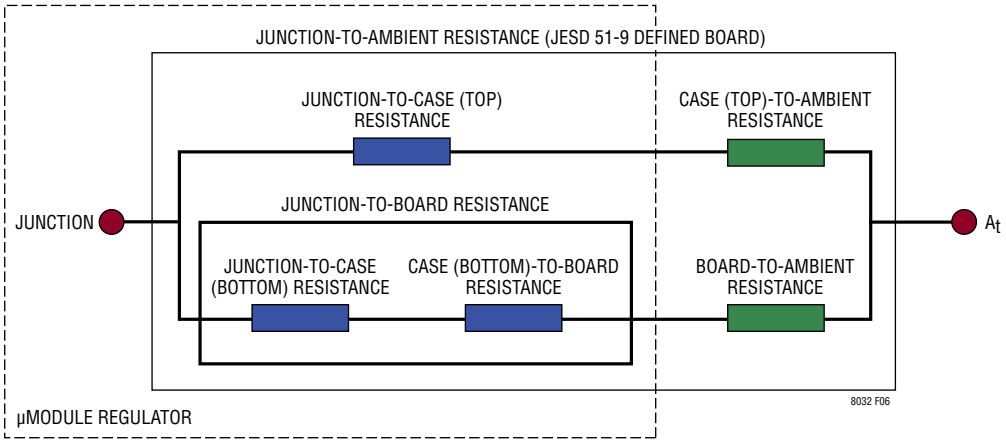
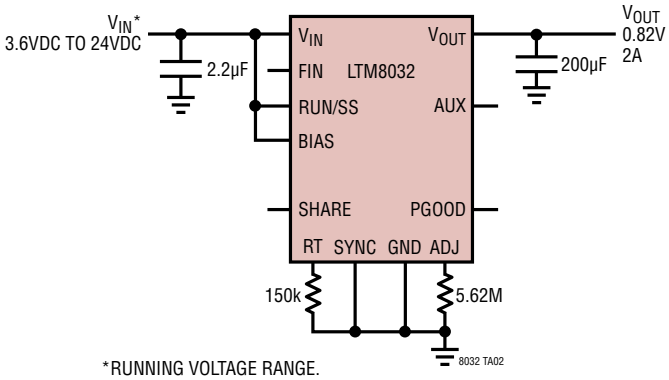



**Figure 6**

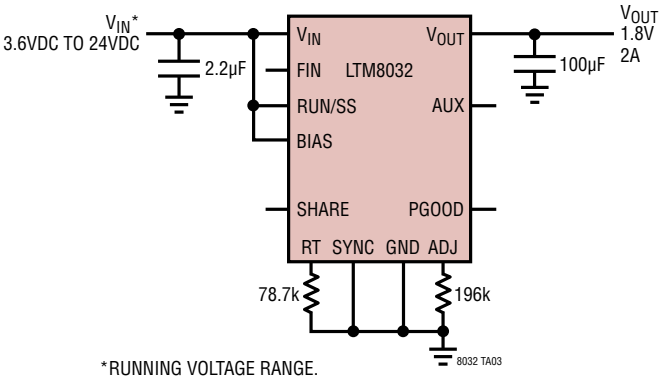
# TYPICAL APPLICATIONS

### 0.82V Step-Down Converter




*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

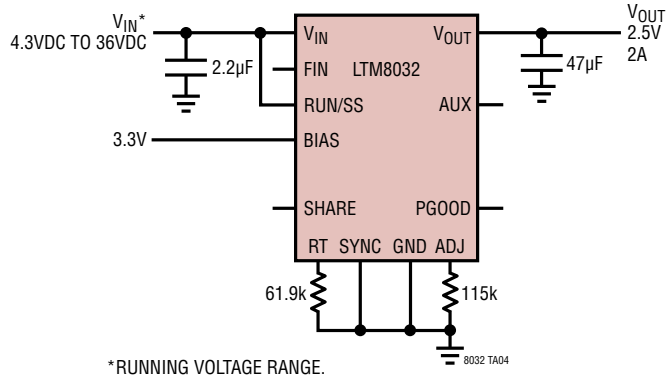
### 1.8V Step-Down Converter




*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

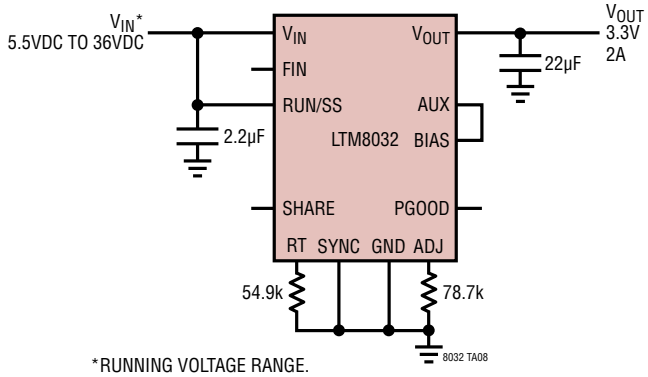
## TYPICAL APPLICATIONS

### 2.5V Step-Down Converter



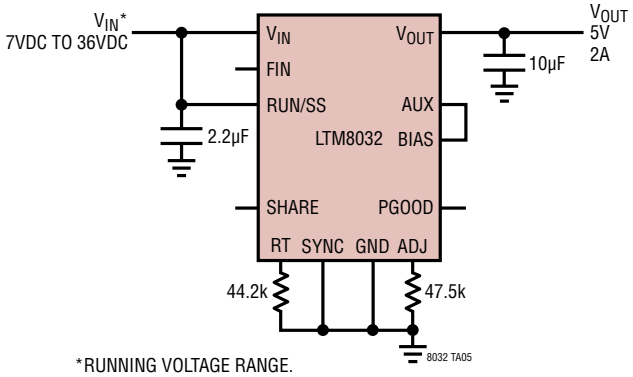

*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

### 3.3V Step-Down Converter




*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

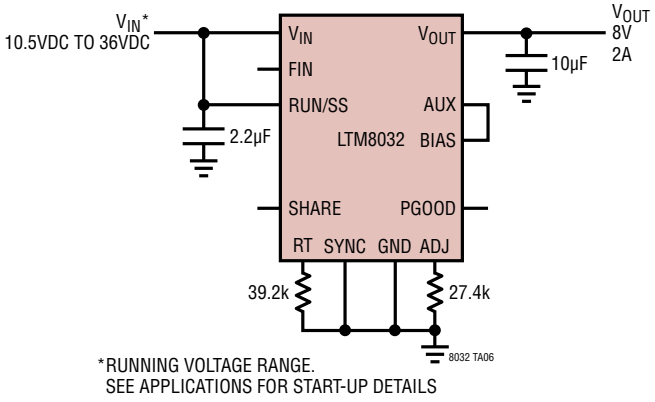
### 5V Step-Down Converter




*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

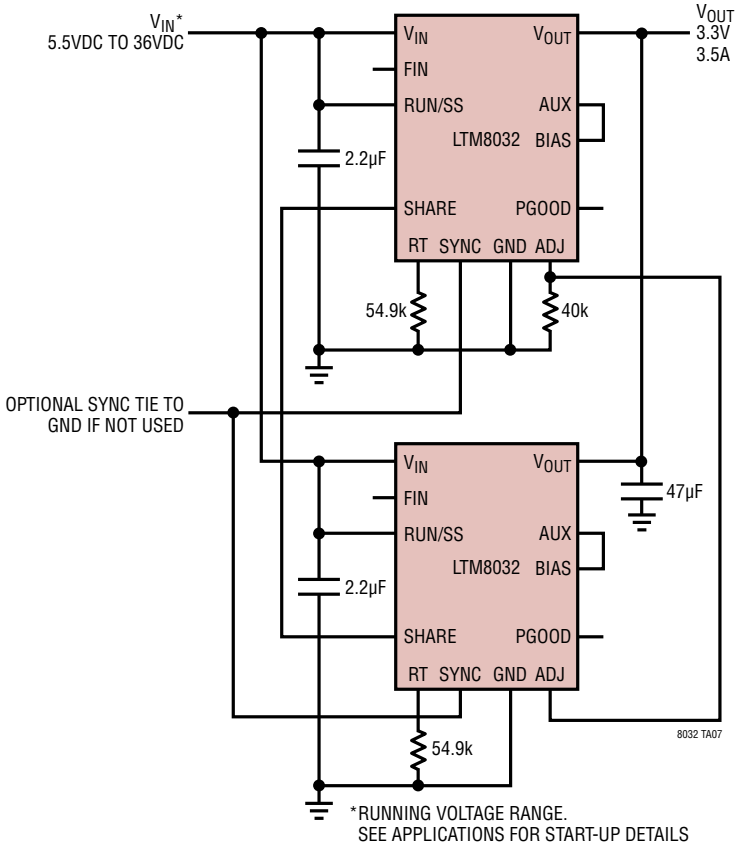
# TYPICAL APPLICATIONS

### 8V Step-Down Converter




*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

### Two LTM8032s Operating in Parallel

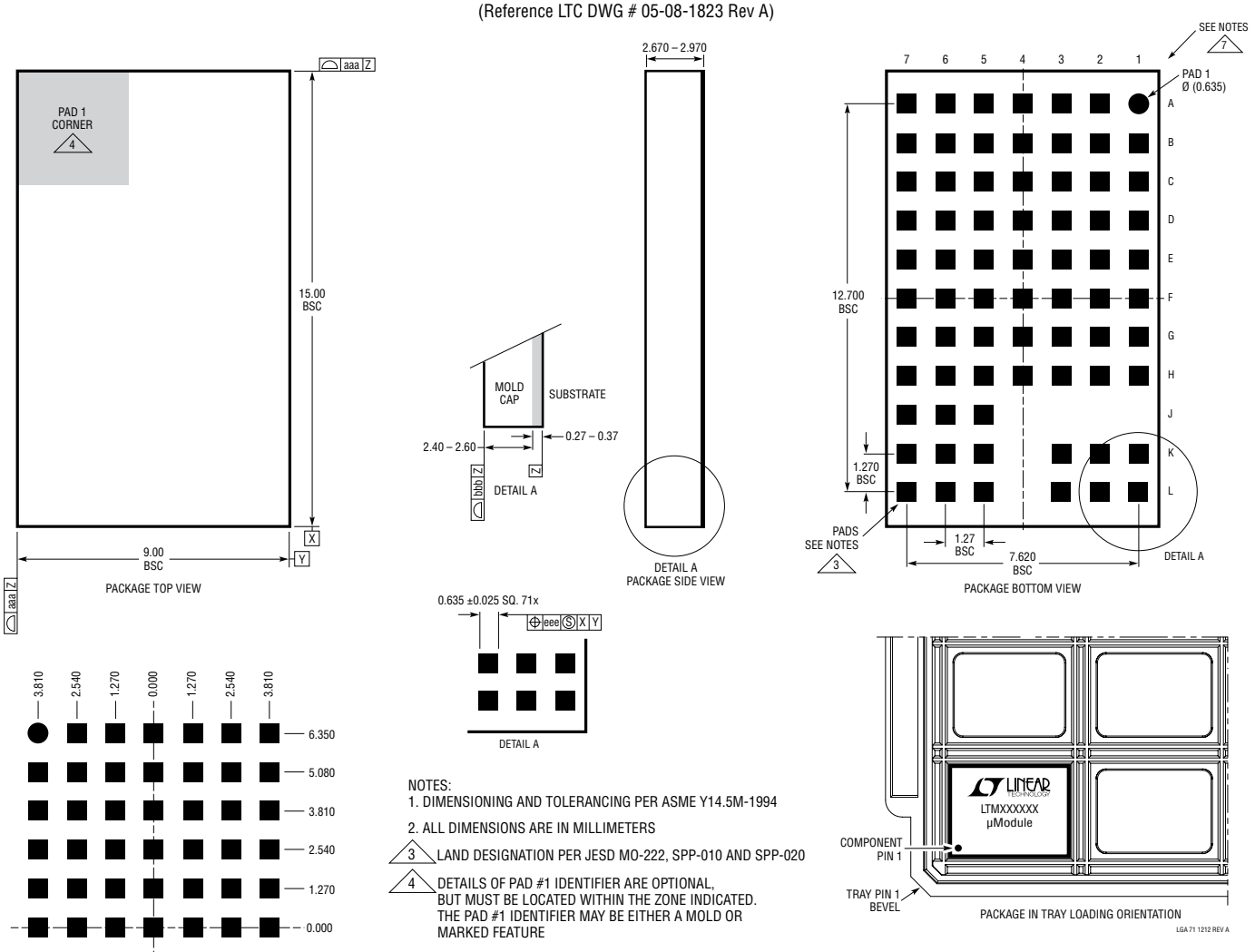



*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**LGA Package**
**71-Lead (15mm × 9mm × 2.82mm)**
(Reference LTC DWG # 05-08-1823 Rev A)



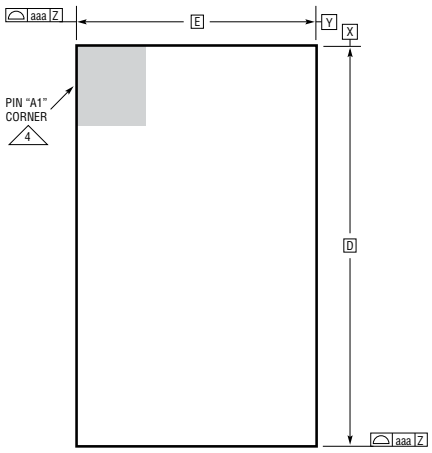

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010 AND SPP-020
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 71
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

| SYMBOL | TOLERANCE |
|---|---|
| aaa | 0.15 |
| bbb | 0.10 |
| eee | 0.05 |

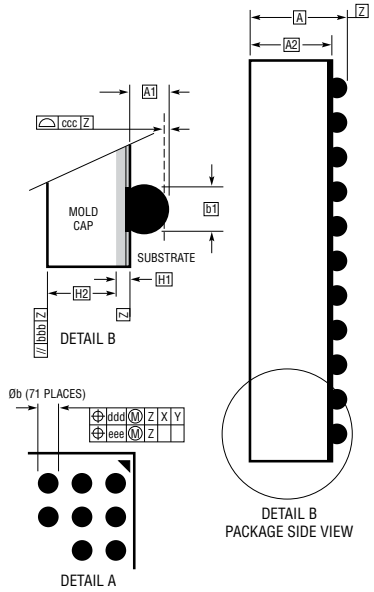
# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

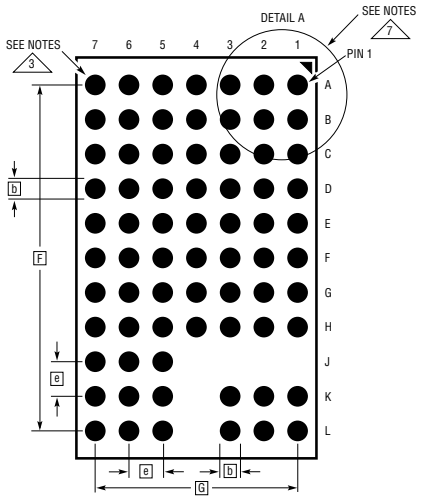
**BGA Package**
**71-Lead (15mm × 9.00mm × 3.42mm)**
(Reference LTC DWG # 05-08-1885 Rev A)



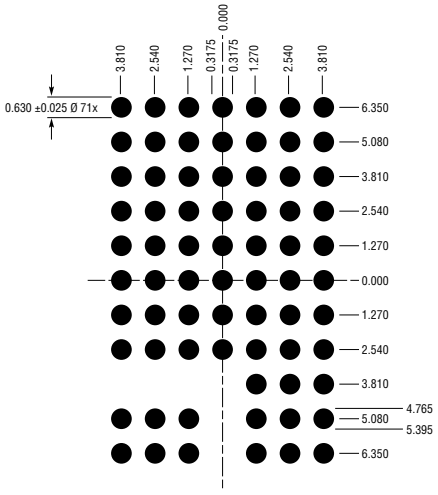

PACKAGE TOP VIEW




DETAIL B
PACKAGE SIDE VIEW



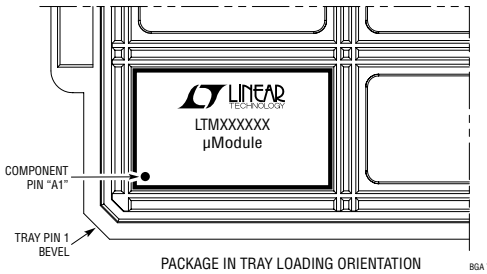

PACKAGE BOTTOM VIEW




SUGGESTED PCB LAYOUT
TOP VIEW

| DIMENSIONS | | | | |
|---|---|---|---|---|
| **SYMBOL** | **MIN** | **NOM** | **MAX** | **NOTES** |
| A | 3.22 | 3.42 | 3.62 | |
| A1 | 0.50 | 0.60 | 0.70 | |
| A2 | 2.72 | 2.82 | 2.92 | |
| b | 0.71 | 0.78 | 0.85 | |
| b1 | 0.60 | 0.63 | 0.66 | |
| D | | 15.0 | | |
| E | | 9.0 | | |
| e | | 1.27 | | |
| F | | 12.7 | | |
| G | | 7.62 | | |
| H1 | 0.27 | 0.32 | 0.37 | |
| H2 | 2.45 | 2.50 | 2.55 | |
| aaa | | | 0.15 | |
| bbb | | | 0.10 | |
| ccc | | | 0.20 | |
| ddd | | | 0.30 | |
| eee | | | 0.15 | |
| TOTAL NUMBER OF BALLS: 71 | | | | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION CAN BE 96.5% Sn/3.0% Ag/0.5% Cu OR Sn Pb EUTECTIC
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY




PACKAGE IN TRAY LOADING ORIENTATION

BGA 71 1212 REV A

# PACKAGE DESCRIPTION

**Table 3. LTM8032 Pinout (Sorted by Pin Number)**

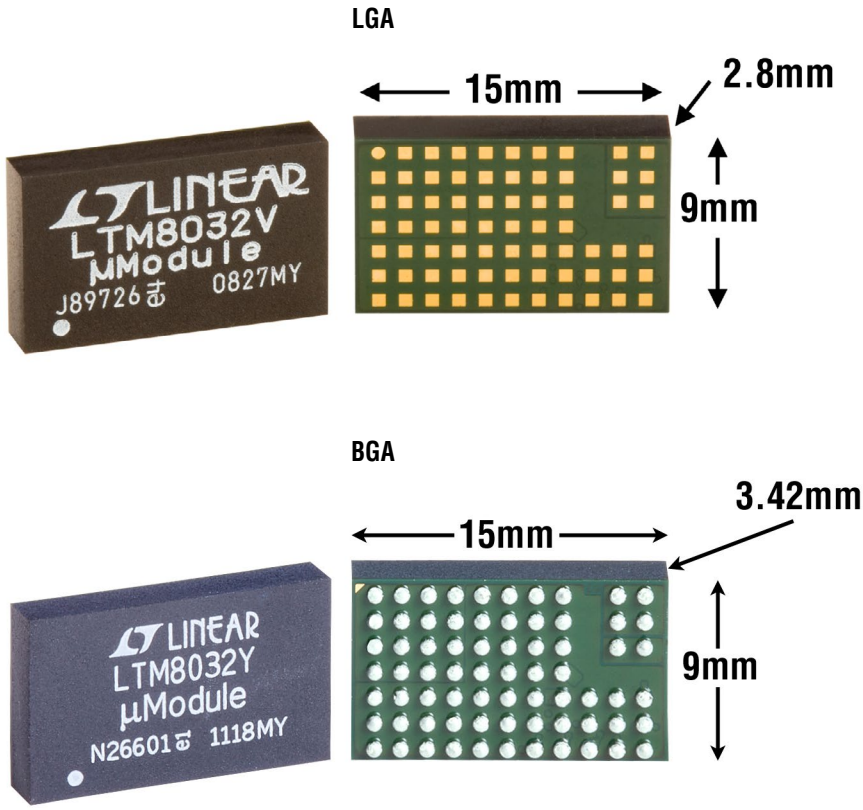
| PIN | SIGNAL DESCRIPTION |
|---|---|
| A1 | $V_{OUT}$ |
| A2 | $V_{OUT}$ |
| A3 | $V_{OUT}$ |
| A4 | $V_{OUT}$ |
| A5 | GND |
| A6 | GND |
| A7 | GND |
| B1 | $V_{OUT}$ |
| B2 | $V_{OUT}$ |
| B3 | $V_{OUT}$ |
| B4 | $V_{OUT}$ |
| B5 | GND |
| B6 | GND |
| B7 | GND |
| C1 | $V_{OUT}$ |
| C2 | $V_{OUT}$ |
| C3 | $V_{OUT}$ |
| C4 | $V_{OUT}$ |
| C5 | GND |
| C6 | GND |
| C7 | GND |
| D1 | $V_{OUT}$ |
| D2 | $V_{OUT}$ |
| D3 | $V_{OUT}$ |
| D4 | $V_{OUT}$ |
| D5 | GND |
| D6 | GND |
| D7 | GND |
| E1 | GND |
| E2 | GND |
| E3 | GND |
| E4 | GND |
| E5 | GND |
| E6 | GND |

| PIN | SIGNAL DESCRIPTION |
|---|---|
| E7 | GND |
| F1 | GND |
| F2 | GND |
| F3 | GND |
| F4 | GND |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| G1 | GND |
| G2 | GND |
| G3 | GND |
| G4 | GND |
| G5 | GND |
| G6 | GND |
| G7 | RT |
| H1 | GND |
| H2 | GND |
| H3 | GND |
| H4 | BIAS |
| H5 | AUX |
| H6 | GND |
| H7 | SHARE |
| J5 | GND |
| J6 | GND |
| J7 | ADJ |
| K1 | $V_{IN}$ |
| K2 | $V_{IN}$ |
| K3 | FIN |
| K5 | GND |
| K6 | GND |
| K7 | PGOOD |
| L1 | $V_{IN}$ |
| L2 | $V_{IN}$ |
| L3 | FIN |
| L5 | RUN/SS |
| L6 | SYNC |
| L7 | GND |

## REVISION HISTORY (Revision history begins at Rev D)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| D | 8/11 | Added BGA package. Changes reflected throughout the data sheet. | 1 to 26 |
| E | 9/11 | Updated BGA Pin Configuration diagram. | 2 |
| F | 2/12 | Indicate Figure 4 is Layout Example for LGA Package<br>Consolidate BGA and LGA Pinout Table | 14<br>24 |
| G | 1/14 | Added SnPb terminal finish product option | 1, 2 |

## PACKAGE PHOTOGRAPHS




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTM8033 | EN55022B Certified 36V, 3A Step-Down µModule Regulator | $0.8V \le V_{OUT} \le 24V$, Synchronizable, 11.25mm × 15mm × 4.3mm LGA |
| LTM4606 | EN55022B Certified 28V, 6A Step-Down µModule Regulator | $0.6V \le V_{OUT} \le 5V$, Synchronizable, 15mm × 15mm × 2.8mm LGA |
| LTM4612 | EN55022B Certified 36V, 5A Step-Down µModule Regulator | $3.3V \le V_{OUT} \le 15V$, Synchronizable, 15mm × 15mm × 2.8mm LGA |
| LTM4613 | EN55022B Certified 36V, 8A Step-Down µModule Regulator | $3.3V \le V_{OUT} \le 15V$, Synchronizable, 15mm × 15mm × 4.3mm LGA |
| LTM8023 | 36V, 2A Step-Down µModule Regulator | $0.8V \le V_{OUT} \le 10V$, Synchronizable, 9mm × 11.25mm × 2.8mm LGA |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