CMOS LSI ΣDECO SM5871A

Digital Audio D/A Converter

OVERVIEW

The ΣDECO SM5871A D/A converter is a high-speed converter for digital audio systems fabricated in Molybdenum-gate CMOS. It incorporates a two-channel, 16-bit D/A converter and a digital eight-times oversampling filter.

The ΣDECO SM5871A can operate at three different sampling frequencies and incorporates de-emphasis and soft mute functions. Double-speed dubbing is supported without any change in clock frequency.

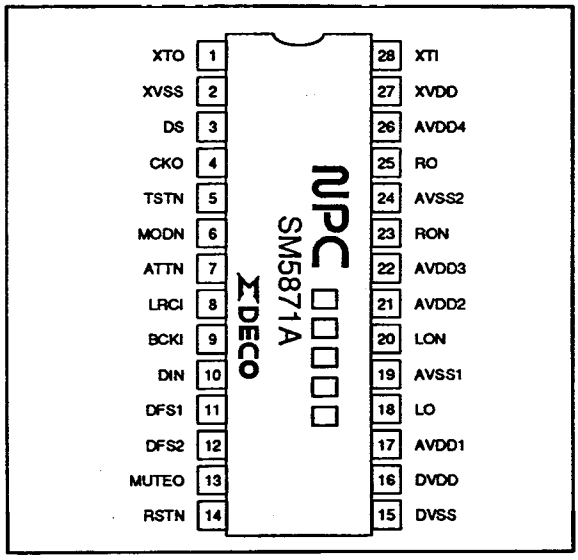
The ΣDECO SM5871A linearly interpolates the input signal at a high multiple of the original sampling frequency, and then requantizes the resulting signal. A third-order noise shaper is used to remove most of the quantizing noise before the signal is output as a pulsewidth-modulated waveform.

The ΣDECO SM5871A operates from a 3.2 to 5.5 V supply and is available in 28-pin shrink DIPs, SOPs and SSOPs.

FEATURES

- Two-channel sigma delta D/A converter
- 32-times oversampling FIR filter
  - 45 + 9 + 5 tap, 8fs FIR filter
  - 40 dB stopband attenuation
  - ±0.15 dB passband ripple
- Third-order zero-shift noise shaper
- Digital deemphasis
- Attenuator
- Soft muting
- 11-level, quasi-symmetrical PWM outputs
- Normal- and double-speed operation (CD only)
- 16.9344 MHz system clock frequency
  - 192fs when fs = 88.2 kHz
  - 384fs when fs = 44.1 kHz
- On-chip crystal oscillator circuit
- 2s complement, msb-first, 16-bit serial input data format
- Single 5 V supply in normal- and double-speed modes
- Low-voltage operation—3.2 V minimum supply voltage operation in normal-speed mode
- 4.5 V minimum supply voltage operation in double-speed mode
- Molybdenum-gate CMOS process
- 28-pin shrink DIP (SM5871AN), 28-pin SOP (SM5871AS) and 28-pin SSOP (SM5871AM)

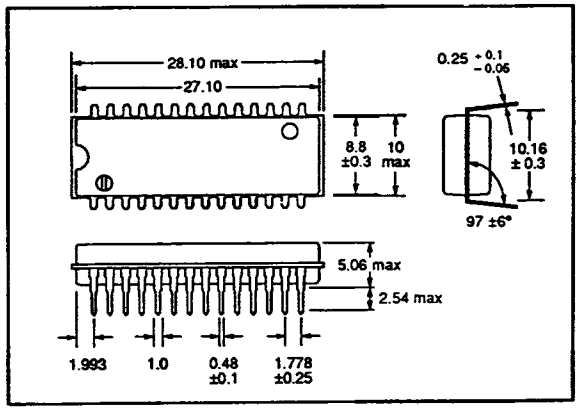
PINOUT



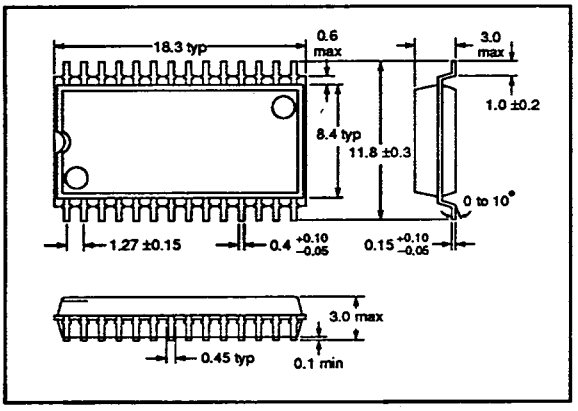
PACKAGE DIMENSIONS

Unit: mm

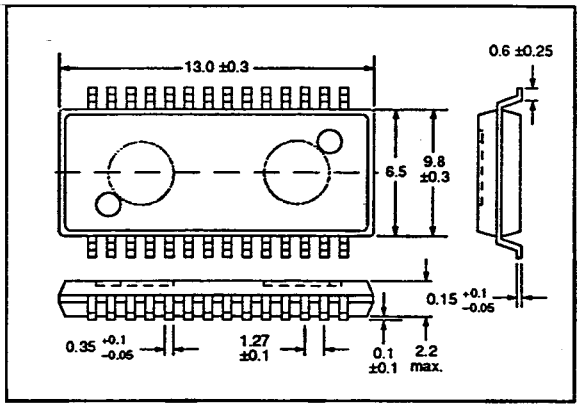
28-pin shrink DIP (SM5871AN)



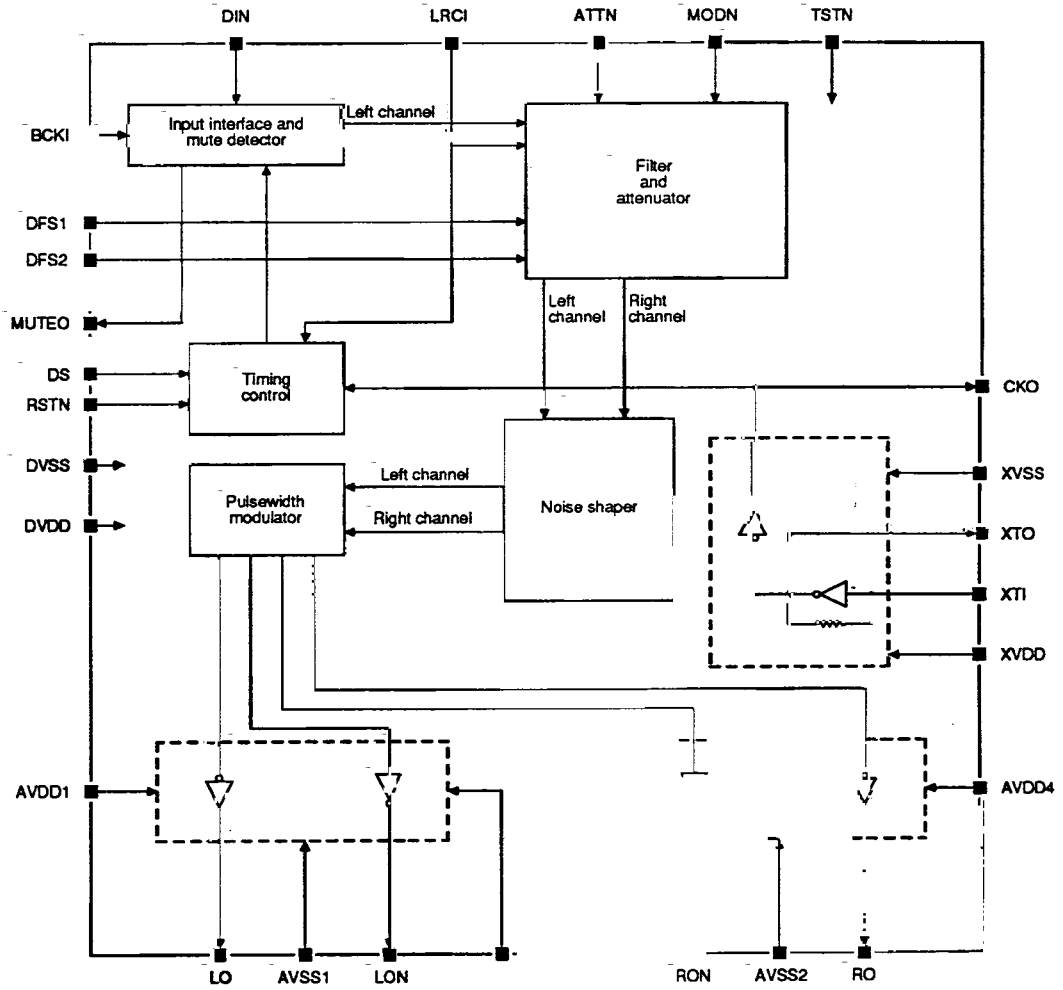
28-pin SOP (SM5871AS)



28-pin SSOP (SM5871AM)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	XTO	Crystal oscillator output
2	XVSS	Clock ground
3	DS	Normal-/double-speed select input. Internal pull-up resistor
4	CKO	Clock output
5	TSTN	Test input. This pin should be tied HIGH for normal operation. Internal pull-up resistor
6	MODN	Mode select input. Internal pull-up resistor
7	ATTN	Soft mute control input. Internal pull-up resistor
8	LRCI	Data sample rate clock input. Internal pull-up resistor
9	BCKI	Bit clock input. Internal pull-up resistor
10	DIN	Serial data input. Internal pull-up resistor
11	DFS1	Deemphasis select input. Internal pull-up resistor
12	DFS2	Deemphasis select input. Internal pull-up resistor
13	MUTEO	Mute detect output
14	RSTN	Reset input. Internal pull-up resistor
15	DVSS	Digital ground
16	DVDD	5 V digital supply
17	AVDD1	Analog supply 1
18	LO	Left-channel positive PWM output
19	AVSS1	Analog ground 1
20	LON	Left-channel negative PWM output
21	AVDD2	Analog supply 2
22	AVDD3	Analog supply 3
23	RON	Right-channel negative PWM output
24	AVSS2	Analog ground 2
25	RO	Right-channel positive PWM output.
26	AVDD4	Analog supply 4
27	XVDD	Clock supply
28	XTI	Crystal oscillator or external clock input

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	−0.3 to 7.0	V
Input voltage range for all inputs except XTI	V_{I1}	DV_{SS} − 0.3 to DV_{DD} + 0.3	V
XTI input voltage range	V_{I2}	XV_{SS} − 0.3 to XV_{DD} + 0.3	V
Power dissipation	P_D	250	mW
Operating temperature range	T_{opr}	−20 to 80	deg. C
Storage temperature range	T_{stg}	−40 to 125	deg. C
Soldering temperature	T_{SLD}	255	deg. C
Soldering time	t_{SLD}	10	s

Recommended Operating Conditions

T_a = 25 deg. C

Parameter	Symbol	Rating	Unit
Supply voltage	DV_{DD}, AV_{DD}, XV_{DD}	5	V
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	3.2 to 5.5	V

Note
All power supply pins (VDD and VSS) must be connected to the same external power supply unit.

DC Electrical Characteristics

Normal supply voltage operation

DV_{DD} = AV_{DD} = XV_{DD} = 4.5 to 5.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, T_a = −20 to 80 deg. C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Digital circuitry supply current	I_{DDD}	DV_{DD} = AV_{DD} = XV_{DD} = 5 V, f_{XTI} = 192fs = 16.9 MHz, no load, double-speed mode. DS is HIGH.	−	25	35	mA
Analog circuitry supply current	I_{DDA}		−	1	2	mA
Clock circuitry supply current	I_{DDX}		−	8	12	mA
LOW-level input voltage	V_{IL2}	See note 1.	−	−	0.5	V
HIGH-level input voltage	V_{IH2}		2.4	−	−	V
XTI LOW-level input voltage	V_{IL1}	External clock input	−	−	0.3XV_{DD}	V
XTI HIGH-level input voltage	V_{IH1}		0.7XV_{DD}	−	−	V
XTI AC input voltage	V_{INAC}	AC coupled input	0.3XV_{DD}	−	−	V_{P-P}
LOW-level output voltage	V_{OLA}	I_{OL} = 1 mA. See note 2.	−	−	0.3	V
HIGH-level output voltage	V_{OHA}	I_{OH} = −1 mA. See note 2.	AV_{DD} − 0.3	−	−	V
CKO LOW-level output voltage	V_{OLC}	I_{OL} = 2 mA	−	−	0.5	V
CKO HIGH-level output voltage	V_{OHC}	I_{OH} = −1 mA	4	−	−	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
MUTEO LOW-level output voltage	V_{OLM}	I_{OL} = 2 mA	–	–	0.4	V
MUTEO HIGH-level output voltage	V_{OHM}	I_{OH} = –1 mA	4	–	–	V
XTI LOW-level input current	I_{IL1}	V_I = 0 V	–	10	20	µA
LOW-level input current	I_{IL2}	V_I = 0 V. See note 1.	–	10	20	µA
XTI HIGH-level input current	I_{IH1}	V_I = XV_{DD}	–	10	20	µA
Input leakage current	I_{LH}	V_I = DV_{DD}. See note 1.	–	–	1	µA

Notes

1. LRCI, BCKI, DIN, DFS1, DFS2, RSTN, DS, TSTN, MODN, ATTN
2. LO, LON, RO, RON

Low supply voltage operation

DV_{DD} = AV_{DD} = XV_{DD} = 3.2 to 4.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, T_a = –20 to 70 deg. C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Digital circuitry supply current	I_{DDD}	DV_{DD} = AV_{DD} = XV_{DD} = 3.4 V, f_{XTI} = 16.9 MHz, no load, normal speed mode. DS is LOW.	–	8	12	mA
Analog circuitry supply current	I_{DDA}		–	0.5	1	mA
Clock circuitry supply current	I_{DDX}		–	2	3	mA
LOW-level input voltage	V_{IL2}	See note 1.	–	–	0.5	V
HIGH-level input voltage	V_{IH2}		2.4	–	–	V
XTI LOW-level input voltage	V_{IL1}	External clock input	–	–	0.3XV_{DD}	V
XTI HIGH-level input voltage	V_{IH1}		0.7XV_{DD}	–	–	V
XTI AC input voltage	V_{INAC}	AC coupled input	0.3XV_{DD}	–	–	V_{P-P}
LOW-level output voltage	V_{OLA}	I_{OL} = 1 mA. See note 2.	–	–	0.3	V
HIGH-level output voltage	V_{OHA}	I_{OH} = –1 mA. See note 2.	AV_{DD} – 0.3	–	–	V
CKO LOW-level output voltage	V_{OLC}	I_{OL} = 0.8 mA	–	–	0.4	V
CKO HIGH-level output voltage	V_{OHC}	I_{OH} = –0.4 mA	2.5	–	–	V
MUTEO LOW-level output voltage	V_{OLM}	I_{OL} = 0.8 mA	–	–	0.4	V
MUTEO HIGH-level output voltage	V_{OHM}	I_{OH} = –0.4 mA	2.5	–	–	V
XTI LOW-level input current	I_{IL1}	V_I = 0 V	–	–	10	µA
LOW-level input current	I_{IL2}	V_I = 0 V. See note 1.	–	–	10	µA
XTI HIGH-level input current	I_{IH1}	V_I = XV_{DD}	–	–	10	µA
Input leakage current	I_{LH}	V_I = DV_{DD}. See note 1.	–	–	1	µA

Notes

1. LRCI, BCKI, DIN, DFS1, DFS2, RSTN, DS, TSTN, MODN, ATTN
2. LO, LON, RO, RON

AC Digital Characteristics

The conditions for normal supply voltage operation are DV_{DD} = AV_{DD} = XV_{DD} = 4.5 to 5.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, T_a = –20 to 80 deg. C unless otherwise noted.
The conditions for low supply voltage operation are DV_{DD} = AV_{DD} = XV_{DD} = 3.2 to 4.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, T_a = –20 to 70 deg. C unless otherwise noted.

System clock

Normal-speed mode (384fs)

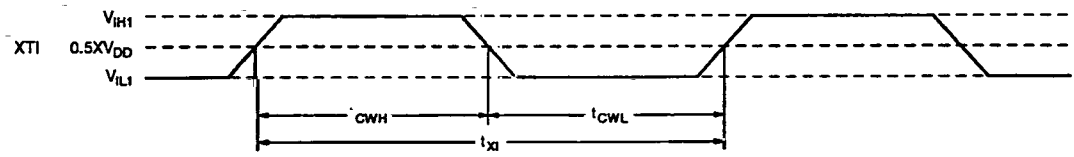
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock frequency	f_{OSC}	fs = 44.1 kHz	4.0	16.9	19.3	MHz
		fs = 48 kHz	4.0	18.4	19.3	
External clock LOW-level pulsewidth	t_{CWL}	fs = 44.1 kHz	21.7	29.5	125	ns
		fs = 48 kHz	21.7	27.1	125	
External clock HIGH-level pulsewidth	t_{CWH}	fs = 44.1 kHz	21.7	29.5	125	ns
		fs = 48 kHz	21.7	27.1	125	
External clock period	t_{XI}	fs = 44.1 kHz	51.7	59.0	250	ns
		fs = 48 kHz	51.7	54.3	250	

Double-speed mode (192fs)

DV_{DD} = AV_{DD} = XV_{DD} = 4.5 to 5.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, T_a = –20 to 70 deg. C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock frequency	f_{OSC}	4.0	16.9	18.5	MHz
External clock LOW-level pulsewidth	t_{CWL}	23.0	29.5	125	ns
External clock HIGH-level pulsewidth	t_{CWH}	23.0	29.5	125	ns
External clock period	t_{XI}	54.0	59.0	250	ns

System clock timing waveform

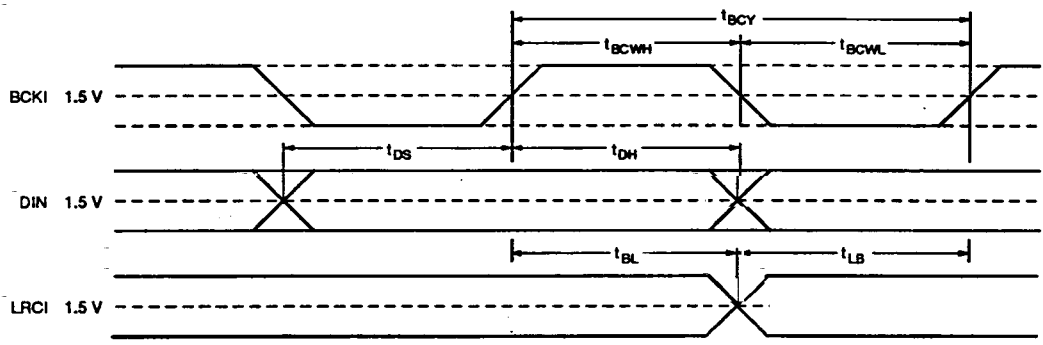


Serial input timing

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI period	t_{BCY}	100	–	–	ns

Parameter	Symbol	Rating			Unit
		min	typ	max	
DIN setup time	t_{DS}	50	–	–	ns
DIN hold time	t_{DH}	50	–	–	ns
BCKI to LRCI delay time	t_{BL}	50	–	–	ns
LRCI to BCKI delay time	t_{LB}	50	–	–	ns

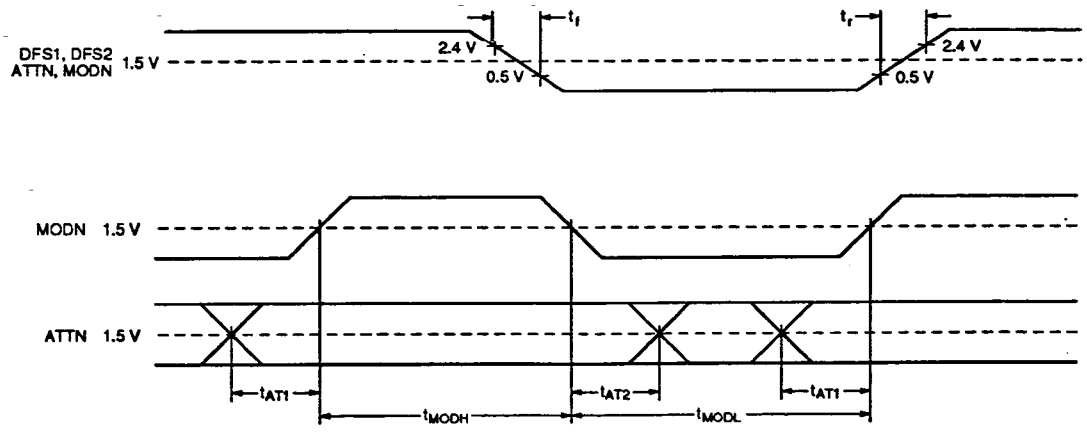
Serial input timing waveform



Control input timing (DFS1, DFS2, ATTN and MODN)

Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock signal rise time	t_r	–	–	100	ns
Clock signal fall time	t_f	–	–	100	ns
ATTN to rising edge of MODN	t_{AT1}	1.5/fs	–	–	ms
Failing edge of MODN to ATTN	t_{AT2}	1.5/fs	–	–	ms
MODN LOW-level pulsewidth	t_{MODL}	4.5/fs	–	–	ms
MODN HIGH-level pulsewidth	t_{MODH}	4.5/fs	–	–	ms

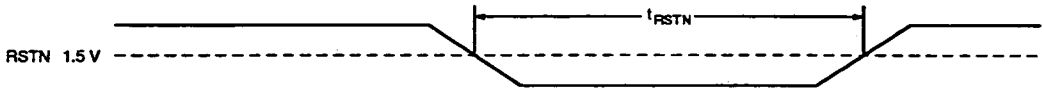
Control input timing waveform



Reset input timing

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
RSTN LOW-level pulsewidth	t_{RSTN}	After power-up	20	–	–	ns

Reset input timing waveform



AC Analog Characteristics

DV_{DD} = AV_{DD} = XV_{DD} = 5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, DS is LOW, external clock input, f_{osc} = 16.9344 MHz, T_a = 25 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion and noise	THD + N	f = 1 kHz, V_I = 0 dB	–	0.0022	0.0035	%
Output level	V_O	f = 1 kHz, V_I = 0 dB	1.8	2.0	2.2	V_{rms}
Dynamic range	D.R	f = 1 kHz, V_I = –60 dB	90	94	–	dB
Signal-to-noise ratio	S/N	f = 1 kHz, V_I = 0 to –∞ dB	104	108	–	dB
Channel separation	Ch. Sep	f = 1 kHz, V_I = –∞ dB	85	95	–	dB

Note

Parameters are measured in accordance with EIAJ Standard CP-307.

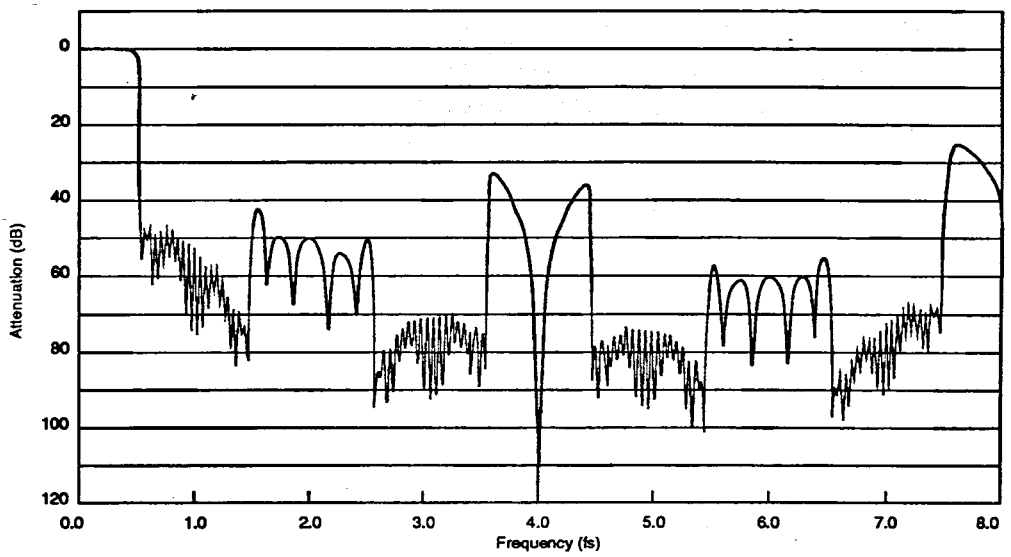
Theoretical Filter Characteristics

The overall frequency characteristics of the IIR deemphasis filter, the eight-times oversampling FIR filter, and the 32fs sample-and-hold circuit are shown in the following tables and graphs.

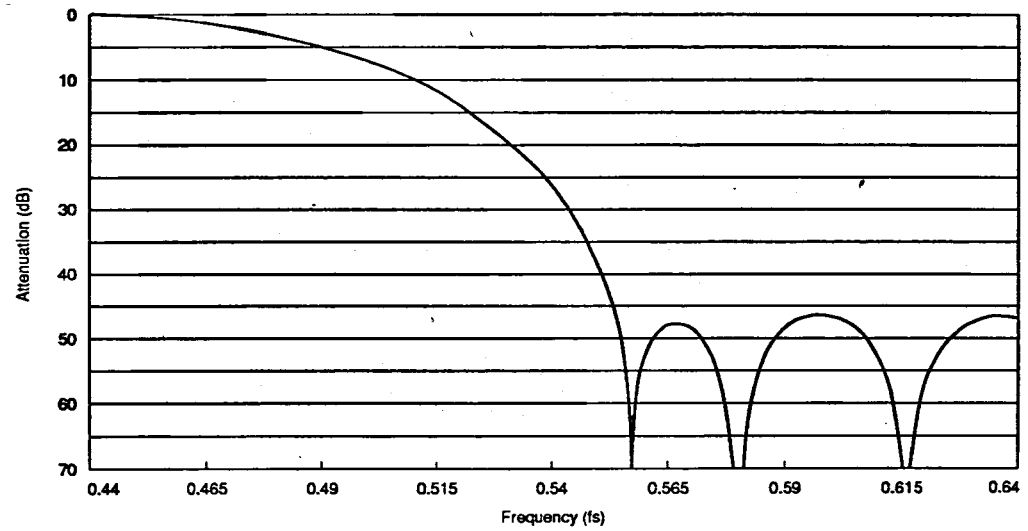
Deemphasis disabled

Parameter	Frequency range		Rating			Unit
	fs	kHz	min	typ	max	
Passband ripple	0 to 0.445	0 to 19.2	0.25 – 0.15	0.25	0.25 + 0.15	dB
Attenuation relative to 1 kHz signal	0.4535	20.0	–	–	0.58	dB
	0.5465	24.1	32	–	–	
Stopband attenuation	0.555 to 1.475	24.5 to 65.05	45	–	–	dB
	1.475 to 1.575	65.05 to 69.5	40	–	–	
	1.575 to 3.45	69.5 to 152.1	45	–	–	
	3.475 to 4.55	152.1 to 200.6	32	–	–	
	4.55 to 7.45	200.6 to 328.5	54	–	–	

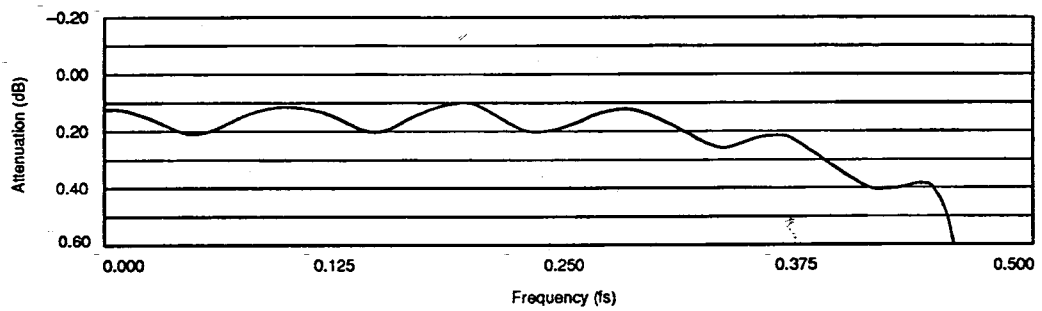
Overall frequency characteristic



Transition band characteristic



Passband characteristic



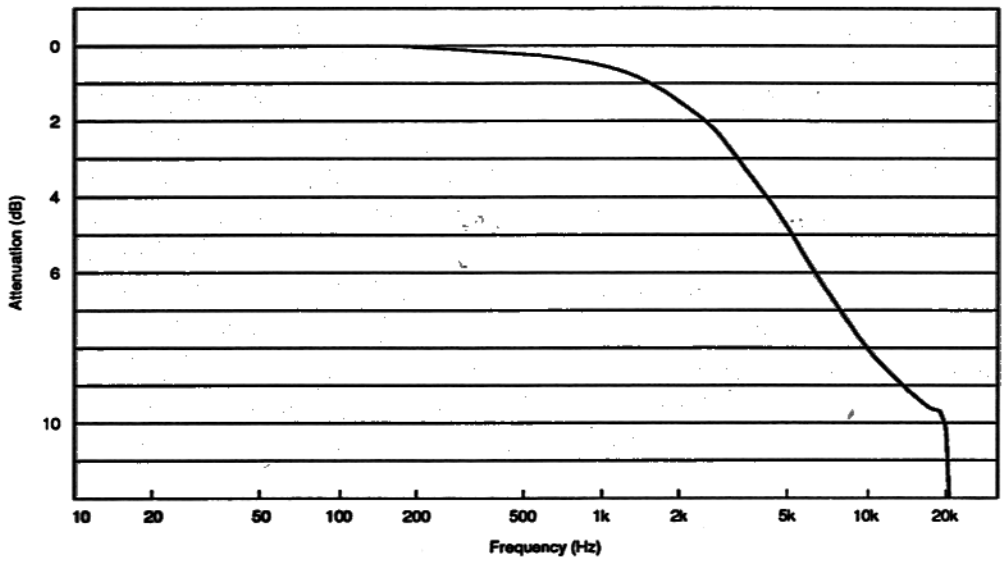
Deemphasis enabled

Parameter	Sampling frequency	Passband	Rating			Unit
			min	typ	max	
Deviation from ideal characteristics	44.1 kHz	0 to 19.2 kHz	0.0	–	0.3	dB
	48.0 kHz	0 to 21.0 kHz	–0.1	–	0.35	dB
	32.0 kHz	0 to 14.0 kHz	–0.35	–	0.7	dB

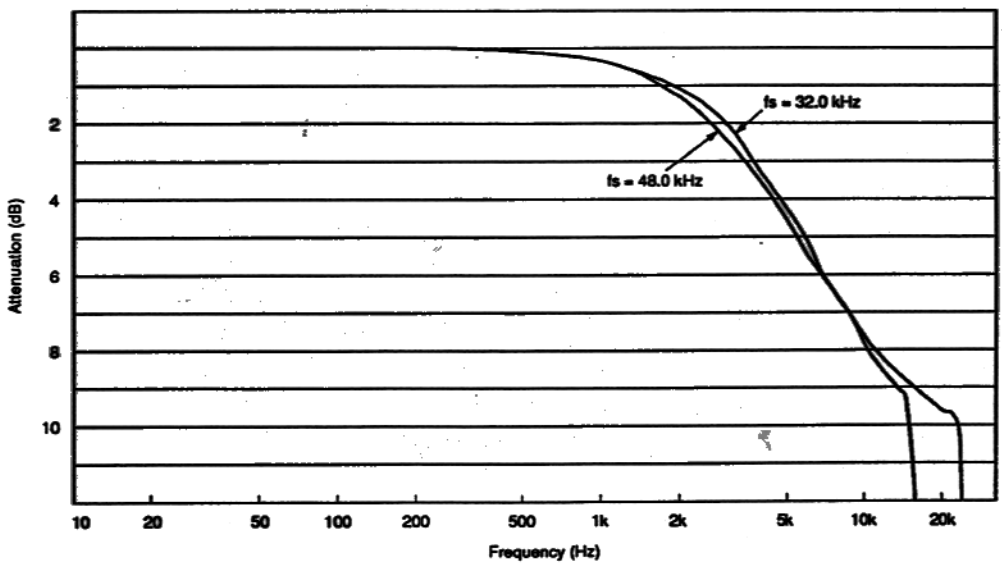
Note
All frequency characteristics are doubled in double-speed mode.

Overall frequency characteristic

fs = 44.1 kHz

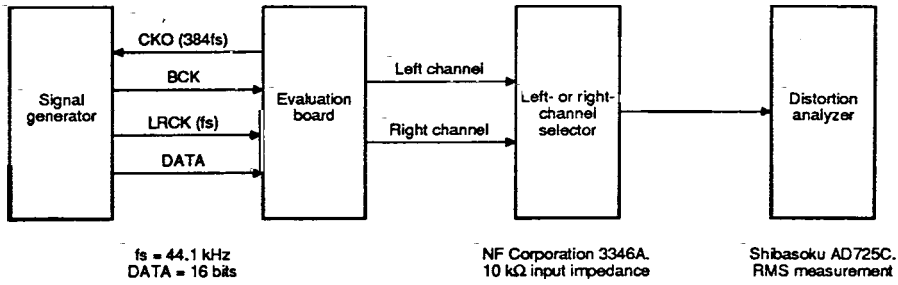


fs = 32 or 48 kHz

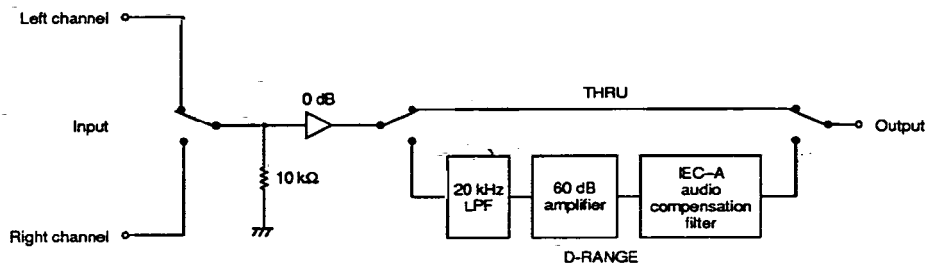


Measurement Circuits

Measurement circuit block diagram



Channel selector internal circuit

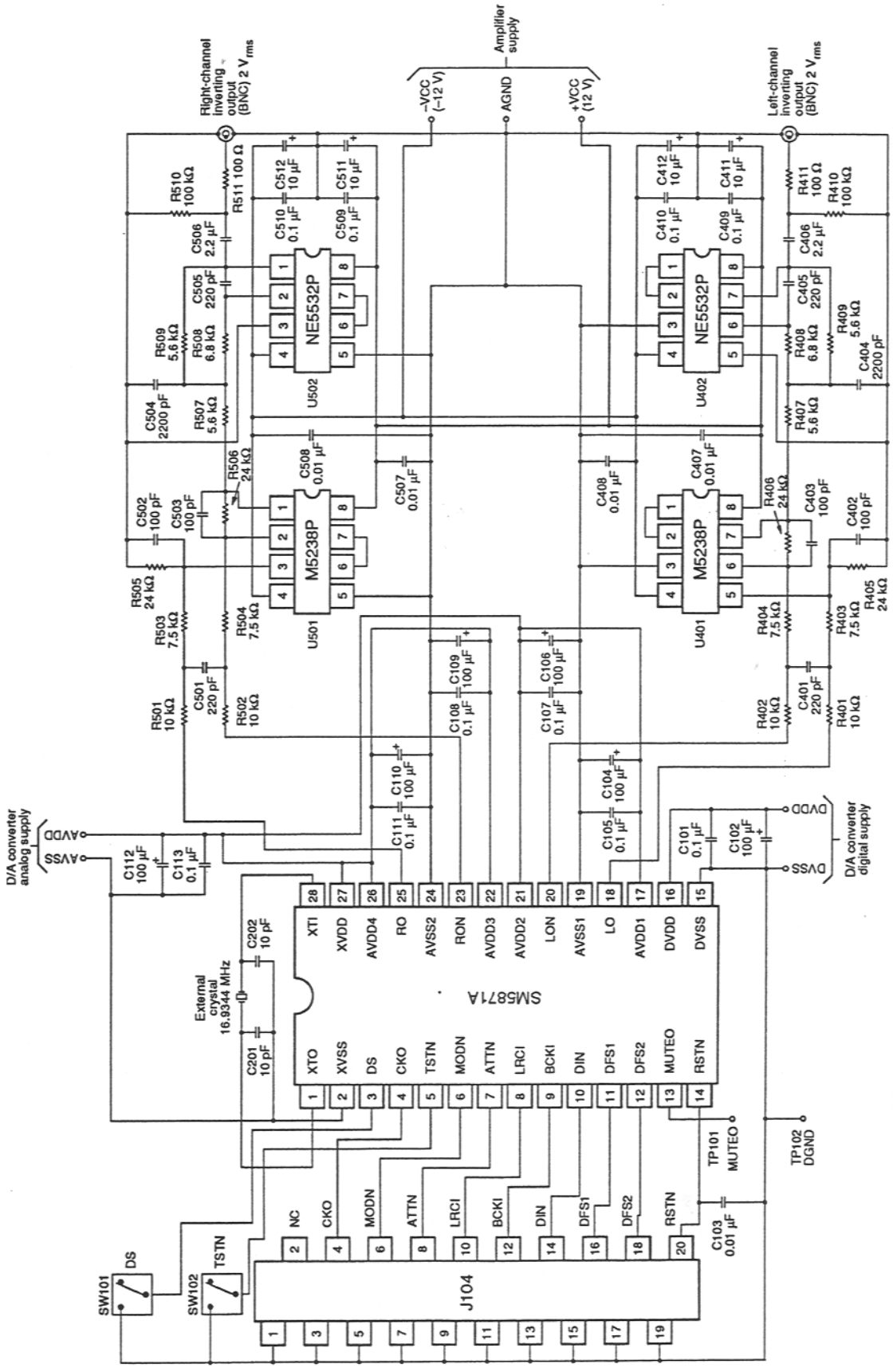


Measurement conditions

Parameter	Symbol	3346A channel selector position	AD725C distortion analyzer setting
Total harmonic distortion and noise	THD + N	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF.
Output level	V_{OUT}		
Dynamic range	D.R	D-RANGE	
Signal-to-noise ratio	S/N	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF. JIS* A-weighted filter is ON.
Channel separation	Ch. Sep	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF.

Japanese Industrial Standard

Measurement circuit



FUNCTIONAL DESCRIPTION

Functional Block Diagram

The basic arithmetic operation of the ΣDECO SM5871A is shown in figure 1.

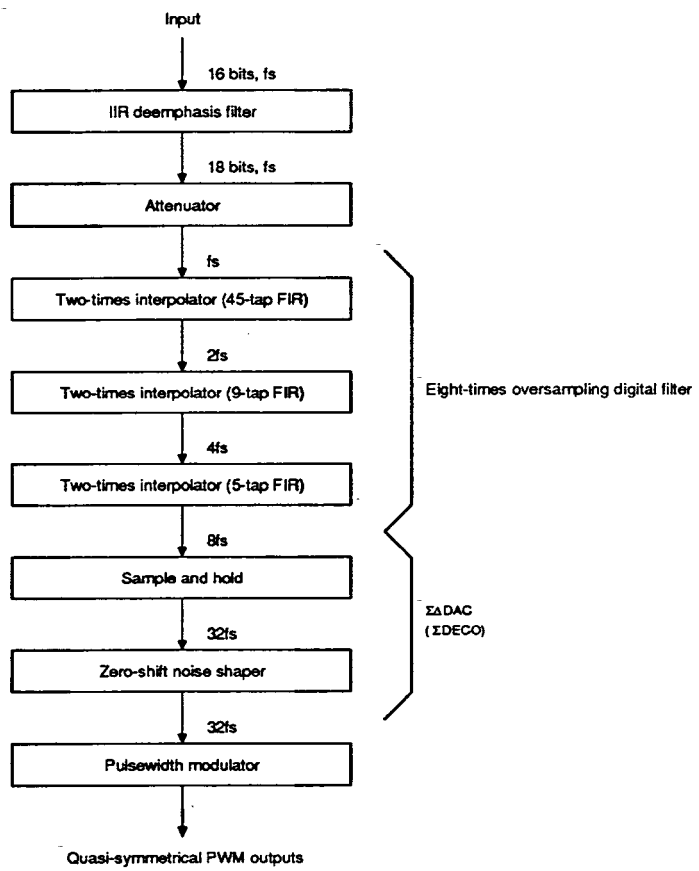


Figure 1. Arithmetic operation

Oversampling Filter

The oversampling filter comprises three, two-times oversampling filters—a 45-tap finite impulse response (FIR) filter, a nine-tap FIR filter and a five-tap FIR filter. These filters raise the sample rate of the input signal to 8fs and attenuate quantization noise between 0.5465fs and 7.4535fs. The signal is oversampled again to 32fs by the sample-and-hold circuit and then input to the zero-shift noise shaper.

Deemphasis Filter

The deemphasis filter is an infinite impulse response (IIR) filter with variable filter coefficients that can be selected by DFS1 and DFS2. The effect of DFS1 and DFS2 on the deemphasis for different sampling rates is shown in table 1.

Table 1. Deemphasis selection

Deemphasis selection		Deemphasis frequency
DFS1	DFS2	
LOW	LOW	44.1 kHz
LOW	HIGH	48.0 kHz
HIGH	HIGH	32.0 kHz
HIGH	LOW	Deemphasis is OFF.

Attenuator and Soft Mute Operation

The ΣDECO SM5871A has an attenuator that is used for both the soft mute and fade in/out functions. The functions are selected by ATTN and MODN as shown in table 2.

Table 2. Attenuation function selection

ATTN	MODN	Selected function
×	LOW	Hold attenuation level
LOW	HIGH	Increase attenuation
HIGH	HIGH	Decrease attenuation

Note
× = don't care

Attenuator

The level of attenuation is determined by the value of the internal 8-bit attenuation counter, DATT. The audio data is multiplied by DATT giving a gain calculated with the following equation.

$$\text{Gain} = 20 \times \log_{10}(1 - \text{DATT}/255) \text{ (dB)}$$

Both channels are muted completely when the value in DATT is 255. Upon reset, DATT is set to zero, corresponding to the maximum gain of 0 dB.

Soft mute

To enable the soft mute function, ATTN is taken LOW, and MODN is held HIGH. DATT is incremented every four LRCI cycles, gradually increasing the attenuation. The signal is completely muted after 1024/fs seconds, which corresponds to 23.2 ms for a 44.1 kHz sampling rate (fs).

Soft muting is cancelled by taking both MODN and ATTN HIGH or by the method shown in figure 3.

Fade in/out attenuation

By controlling MODN and ATTN as described in table 2, the level of attenuation can be adjusted continuously to give a fade in/out function. An example of attenuation control is shown in figure 2.

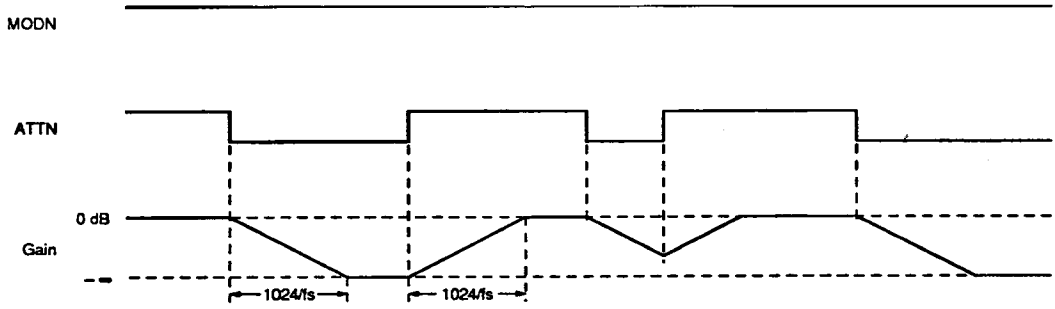


Figure 2. Fade in/out control

ATTN and MODN timing

When MODN is HIGH, the attenuation counter counts up or down when ATTN is held LOW or HIGH, respectively. MODN should be HIGH for at least 4.5/fs for each up/down step. The timing of ATTN and MODN is shown in figure 3.

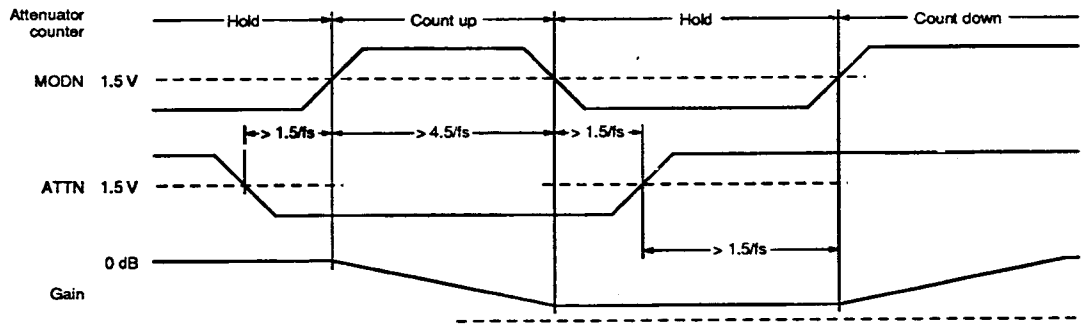


Figure 3. ATTN and MODN timing

System Clock

The system clock oscillates at either 192fs or 384fs, selected by the level on DS. This feature allows double-speed playback selection where the sampling frequency is 88.2 kHz. The effect of DS on the system parameters is shown in table 3, and the internal clock switching circuit, in figure 4.

Table 3. System clock selection

Parameter	Symbol	Condition	Rating	Unit
XTI input frequency	F_{XI}	DS is HIGH. fs = 88.2 kHz	16.9344	MHz
		DS is LOW. fs = 44.1 kHz	16.9344	
CKO output frequency	F_{CO}	DS is HIGH.	192	fs
		DS is LOW.	384	
Internal system clock period	T_{SYS}	DS is HIGH.	t_{XI}	s
		DS is LOW.	t_{XI}	

Note

t_{XI} is the input clock period.

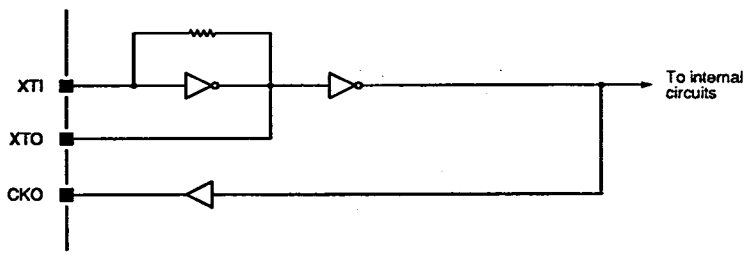


Figure 4. System clock circuit

As the stability and signal-to-noise ratio of the system clock greatly affects the AC analog characteristics, care should be taken to ensure that the clock is free from jitter.

The system clock can be controlled by a crystal oscillator, connected as shown in figure 5. Capacitors C1 and C2 should be chosen to match the crystal oscillator used.

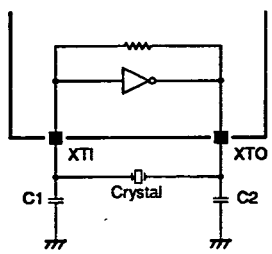


Figure 5. External crystal oscillator connection

The system clock can also be supplied externally as shown in figure 6. When using this method, XTO should be left unconnected. As the system clock inverter has an internal feedback resistor, the external clock input can be AC-coupled.

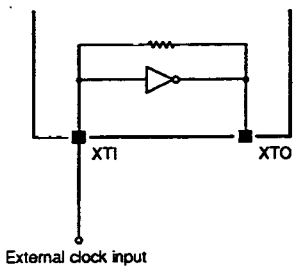


Figure 6. External system clock connection

To optimize the AC analog characteristics, use an external crystal oscillator based on a 74HCU04 inverter to drive XTI.

Audio Data Input

The digital audio data is input on DIN in 2s complement, msb-first, 16-bit serial data format. Bits are clocked into the input shift register on the rising edge of BCKI. The data in the input shift register is latched into the left- and right-channel input data latches on the falling and rising edges of LRCI, respectively.

The timing of the arithmetic and output circuits is independent of the input circuits to isolate them from jitter or skew on the input circuit clocks. As a result, phase differences between LRCI, BCKI and XTI that may occur after a reset do not affect the correct operation of the device, however, the correct frequency ratio between LRCI and XTI must be maintained. The ΣDECO SM5871A should be reset if either of the LRCI or XTI clocks stop. If a reset is not performed, the device may not function correctly and produce unwanted noise at the outputs.

Zero-shift Noise Shaper

The third-order zero-shift noise shaper (ZSNS) reduces the noise in the 11-level quantized signal by altering the noise characteristic. The characteristic is altered by shifting the zeros in the z-plane, moving the noise out of the audio band where it is then removed by the output filters. A theoretical characteristic is shown in figure 7, calculated by converting the data back into its original form, before the PWM output stage.

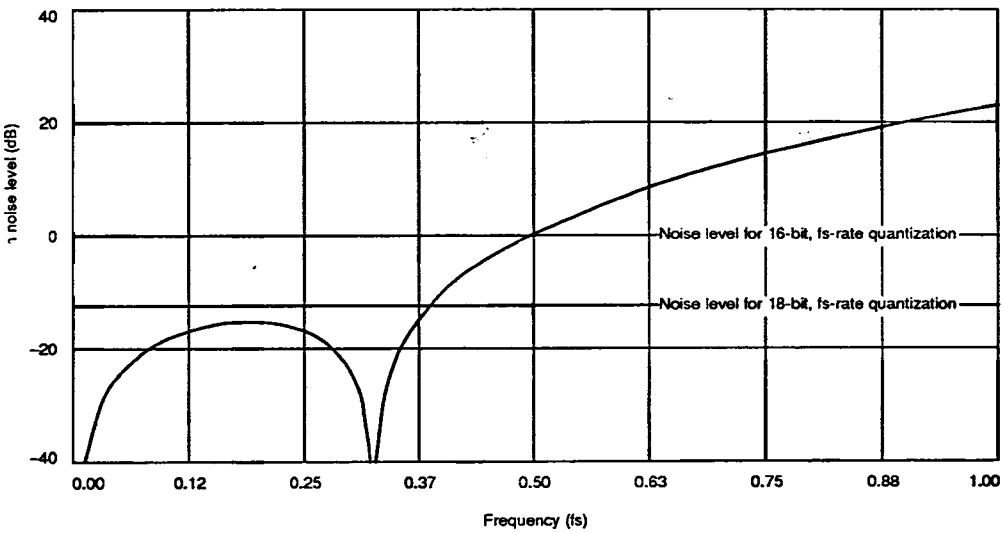


Figure 7. Requantizer noise characteristic

Pulsewidth Modulation Waveforms

The signals output by the ΣDECO SM5871A are quasi-symmetrical. When the PWM outputs produce odd-valued output levels, the individual output signals are not symmetrical about the center of the output pulses, however the difference signals (LO – LON) and (RO – RON) are symmetrical as shown in figure 8. Even-valued output signals have symmetrical waveforms.

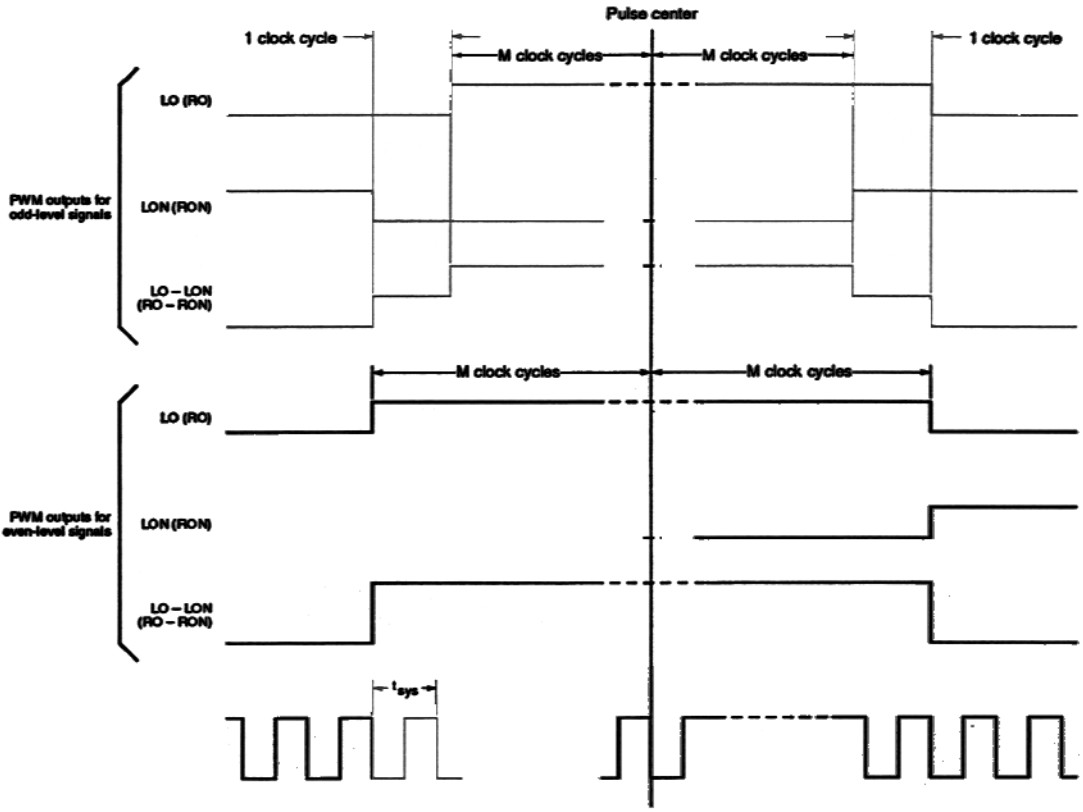


Figure 8. Pulsewidth modulation waveforms

Reset

The ΣDECO SM5871A should be reset after power-up, when DS changes state or when either of the LRCI or XTI clocks stop. A LOW-level pulse on RSTN will resynchronize the ΣDECO SM5871A internal arithmetic and output clocks on the first rising edge of LRCI after RSTN returns HIGH.

A reset can be performed automatically if a capacitor is connected between RSTN and VSS. If the XTI and LRCI clocks are stable on power-up, then a value of 300 pF is sufficient to satisfy the reset timing requirements. If the XTI and LRCI clocks are not stable on power-up, then a value should be chosen such that RSTN goes HIGH only after both clocks have stabilized.

Upon reset, the PWM outputs are muted with a 50% duty cycle signal from the time when RSTN goes LOW until the 12th rising edge of LRCI after RSTN goes HIGH.

Mute Detection

The ΣDECO SM5871A monitors the digital audio bit stream from the signal processor for a muted signal, indicated by a continuous stream of zero bits in 2s complement format. DIN must be LOW for all cycles of the bit clock, BCKI, if the number of cycles per word exceeds the number of bits per word.

When both channels contain zeros for 2^{19} consecutive bits, an internal zero counter overflows and its carry bit is output on MUTEO. When a one is input, MUTEO is cleared and the zero counter is reset. The time to overflow the zero counter can be calculated using the following equation.

$$t_z = 2^{19}/(NB \times fs)$$

where NB = Number of bit cycles per sample period (typically 32 or 48).

For a 44.1 kHz sampling rate and 32 bits per sampling period, 2^{19} bits corresponds to a mute detect time of 372 ms. When there are 48 bits per sampling period, the mute detect time becomes 248 ms as shown in table 4.

Table 4. Mute detect time

Bit clock frequency	Mute detect time	Unit
32fs	372	ms
48fs	248	ms

Note
fs = 44.1 kHz

TIMING DIAGRAMS

Digital Audio Input Formats

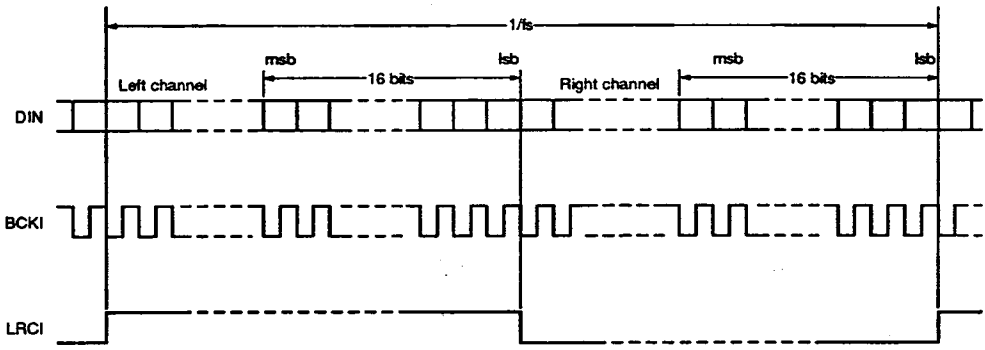


Figure 9. Audio data format 1

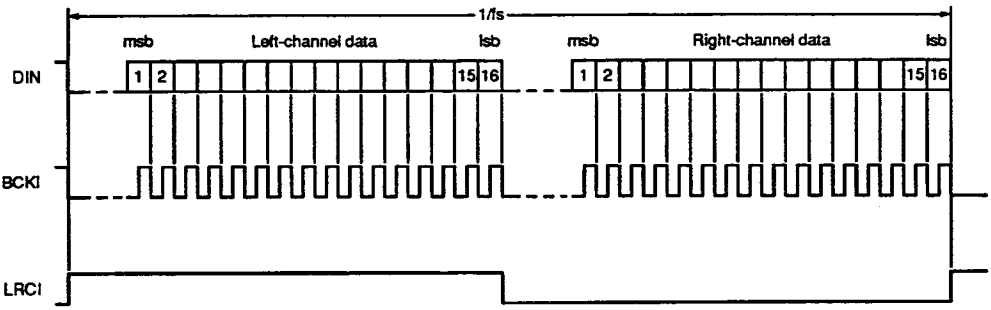
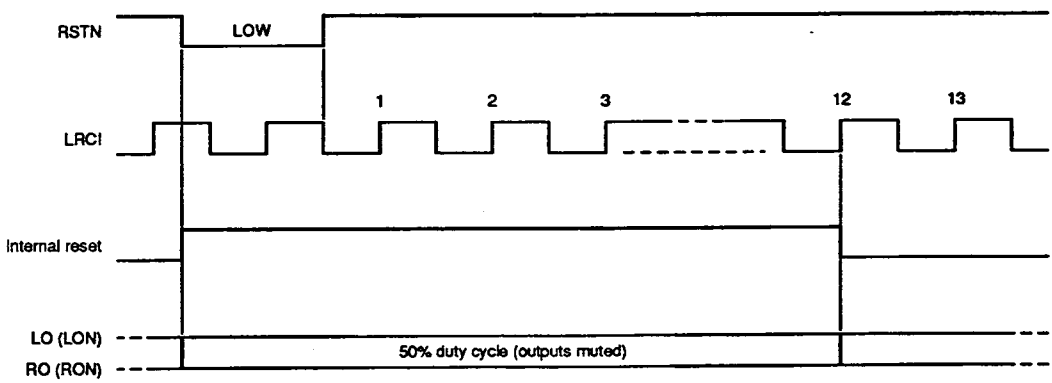


Figure 10. Audio data format 2

Reset Timing



Mute Detection

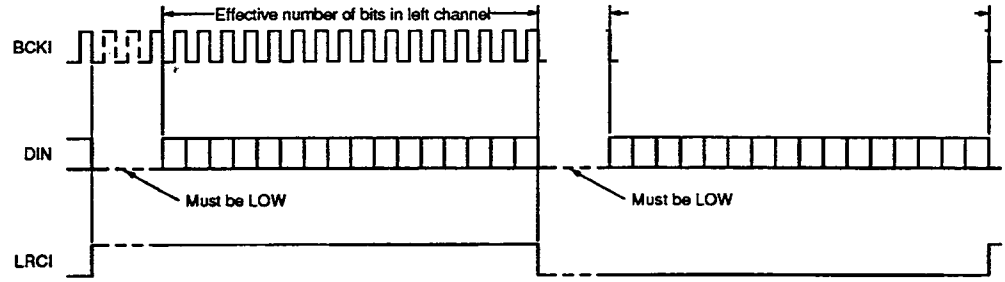


Figure 11. Mute detect timing

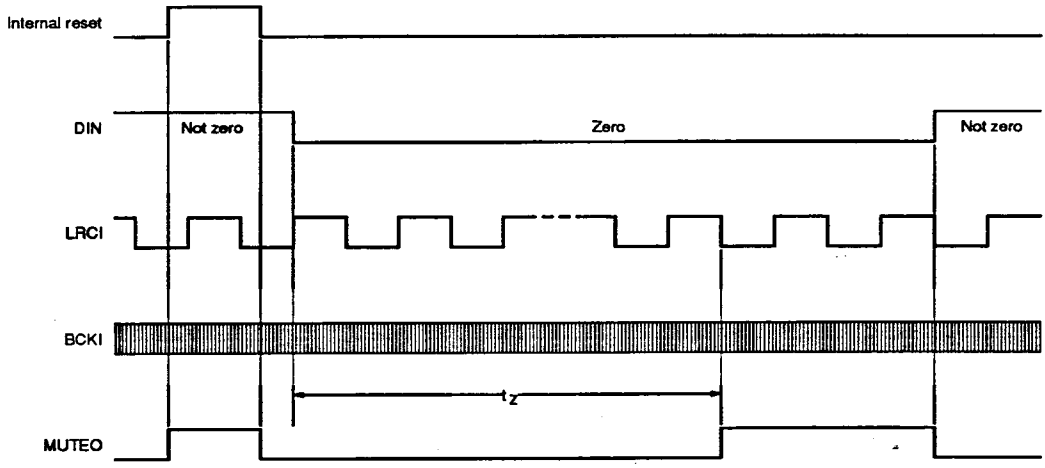


Figure 12. MUTEO output timing

APPLICATION NOTES

Input Interfaces

Normal replay mode

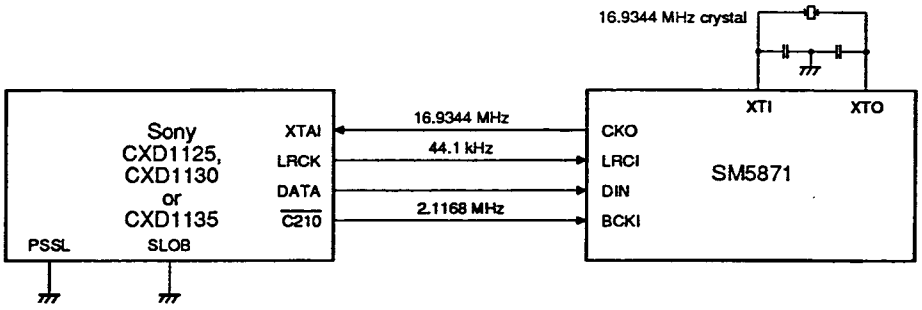


Figure 13. Sony CXD1125, CXD1130, CXD1135 interface

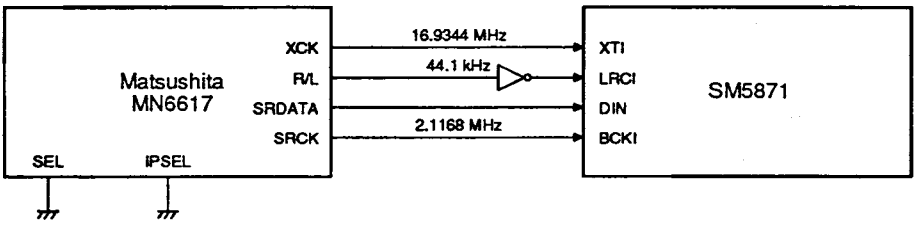


Figure 14. Matsushita MN6617 interface

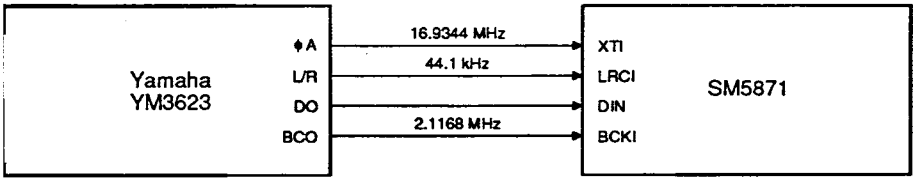


Figure 15. Yamaha YM3623 interface

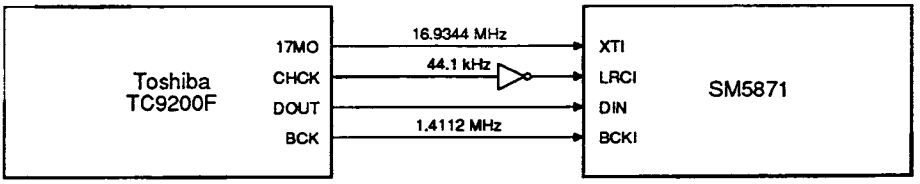


Figure 16. Toshiba TC9200F interface

Double-speed replay mode

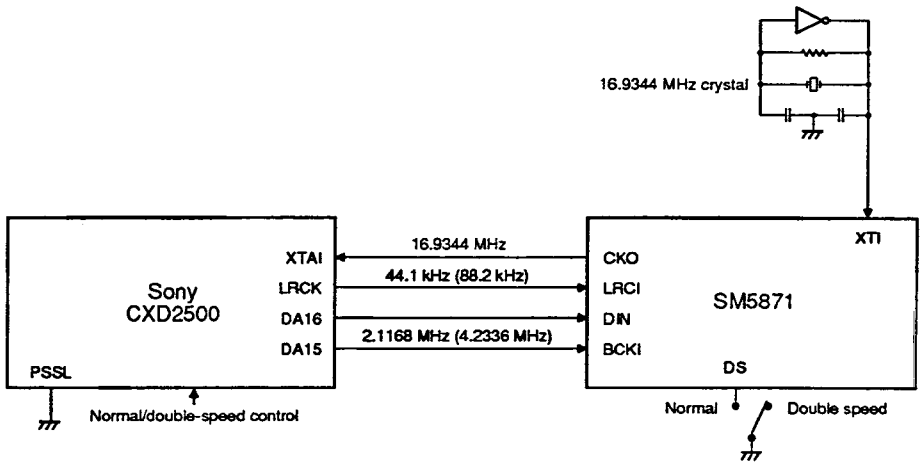


Figure 17. Sony CXD2500 interface

Note
The values in parentheses are for double-speed mode.

Output Interfaces

In the following figures, only the left channel has been shown to avoid duplication.

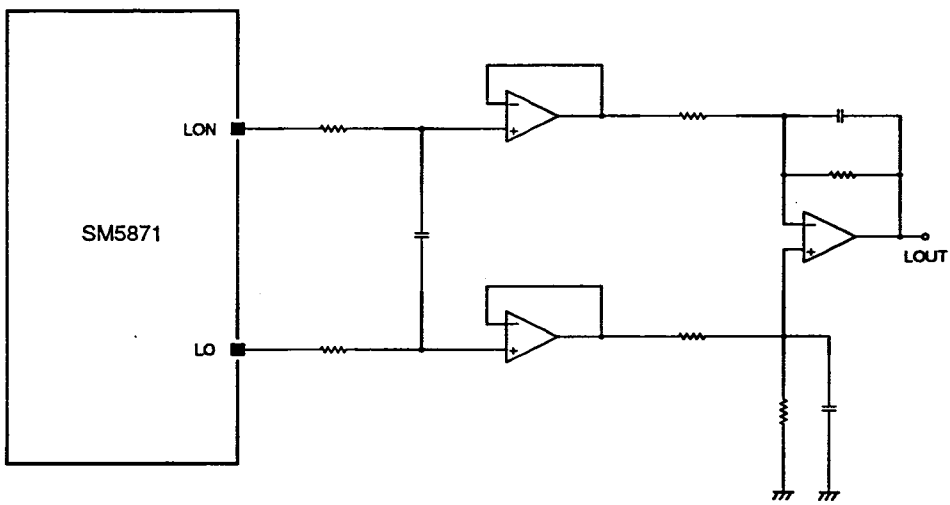


Figure 18. Output interface 1

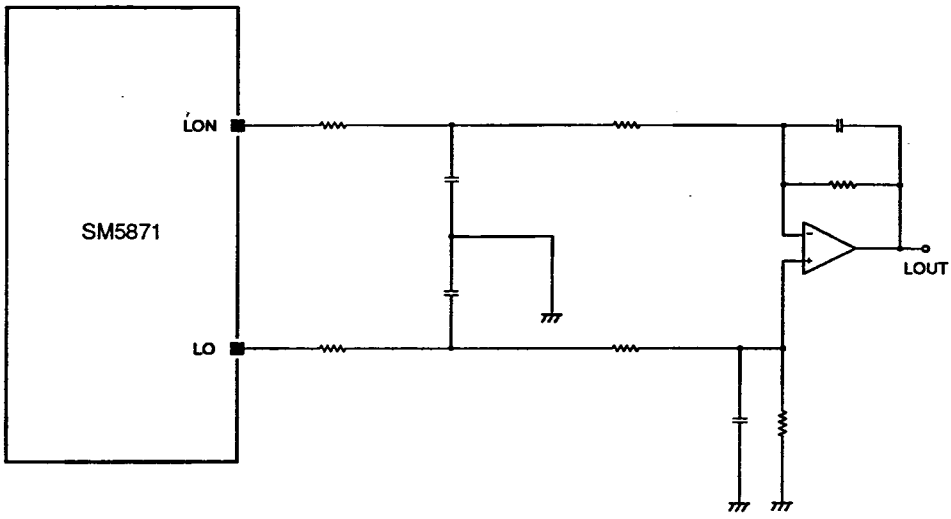


Figure 19. Output interface 2

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