AN2842
Application note

Paralleling of power MOSFETs in PFC topology

Introduction

The current handling capability demands on power supply systems to meet high load current requirements and provide greater margins for overload and reliability, often exceed the capability of the largest semiconductor devices considered, and their paralleling may become an attractive alternative. All semiconductor circuits using parallel connected devices to switch to higher load currents can easily be analyzed by using Kirchoff's law. As long as all voltage drops in the parallel branches are equal, the currents through the branches are of similar values if the resistance in each branch is the same. This is logical, but when we consider the various functions where switching devices are employed, we must also consider the parameters of each single switching device and all the parasitic phenomena related to the device.

In this paper we review several factors that influence the behaviors of devices in parallel configurations. When devices operate in parallel configurations to provide a good dynamic equilibrium among device currents, consideration should be given to current sharing. The layout design must be carried out carefully to minimize the differences between device branches. In addition, switching parameters of devices may not be the same, causing one to be continuously stressed (by at some time supporting all the input current). Naturally, this problem worsens as the number of paralleled devices increases. Therefore, it is very important to understand which factors are linked to the device that cause current imbalance.

Concerning power MOSFET devices, there are many parameters that can influence the current imbalance and in principle they can be summarized as threshold voltage, gain, intrinsic capacitances, ON resistance and working temperature mismatches. Individually or in combination, mismatch between these parameters may produce serious imbalances and could cause device failure.

In order to investigate the impact of the different factors, some PFC topologies have been analyzed. The study has included different topologies to understand if the device behaviors are also related to the configuration. In this paper, three booster PFC topologies are discussed. In the first topology, a booster PFC is developed using two power MOSFETs connected directly in parallel (*Figure 1*). In this case, two different drive circuits are used for each single device. Another topology under analysis uses two PFC blocks connected in parallel (*Figure 2*). Also in this case, two drive circuits pilot the gate pin. Finally, a topology with three devices connected in a parallel configuration is analyzed (*Figure 3*).

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1 Schematic diagrams of analyzed topologies

The following schematics show the three booster PFC topologies discussed in this application note.

Figure 1. Two MOSFETs connected in parallel with a single boost inductor

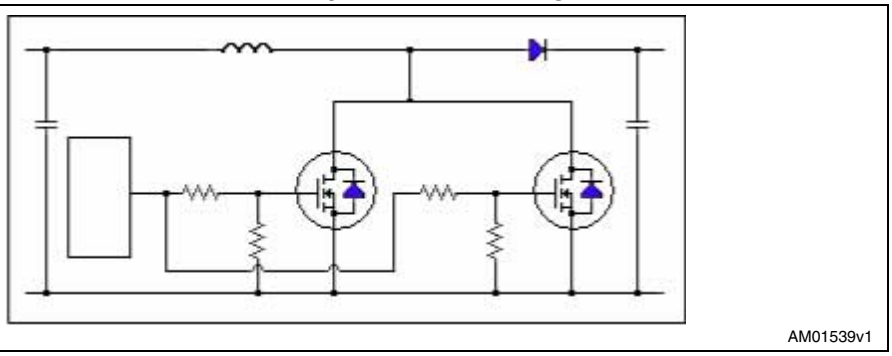


Figure 2. Two MOSFETs connected in parallel with a different boost inductor

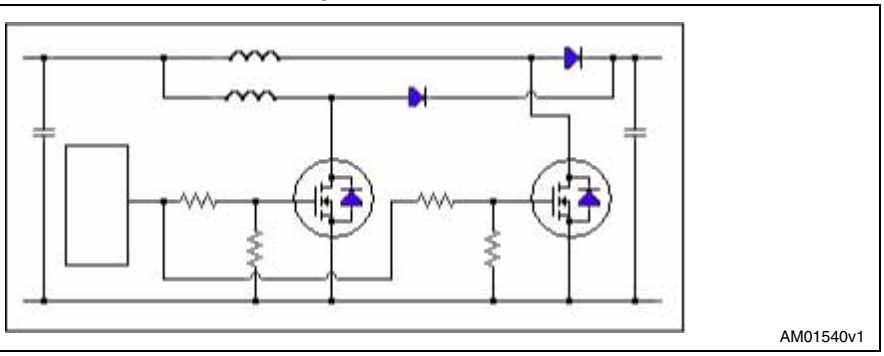
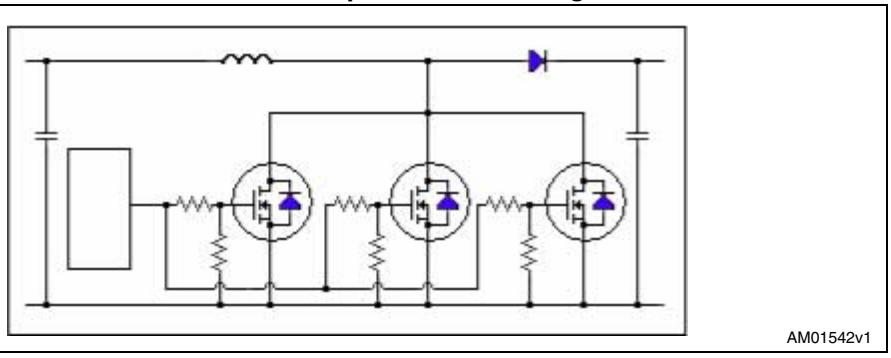


Figure 3. Three MOSFETs connected in parallel with a single boost inductor



2 Approach to the study

To better understand the factors that cause current imbalance, it is important to divide the analysis into two different areas: in the first, we study the influence of the parameters around the power device, while in the second we analyze the impact of the intrinsic parameters of the power MOSFET. The parameters analyzed in the first approach are:

- differences between the power circuit components
- gate circuitry
- influence of the boost diode in the current imbalance
- temperature imbalance between devices

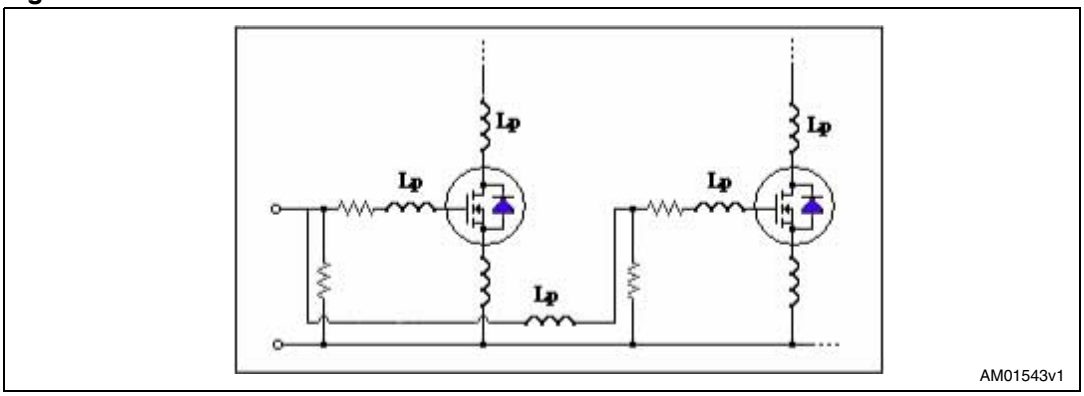
In the second part, we analyze the parameters linked directly to the power MOSFET, and in particular:

- differences in the $V_{GS(th)}$
- differences of $R_{DS(on)}$
- influence of the g_{fs} parameter

2.1 Differences between the power circuit components

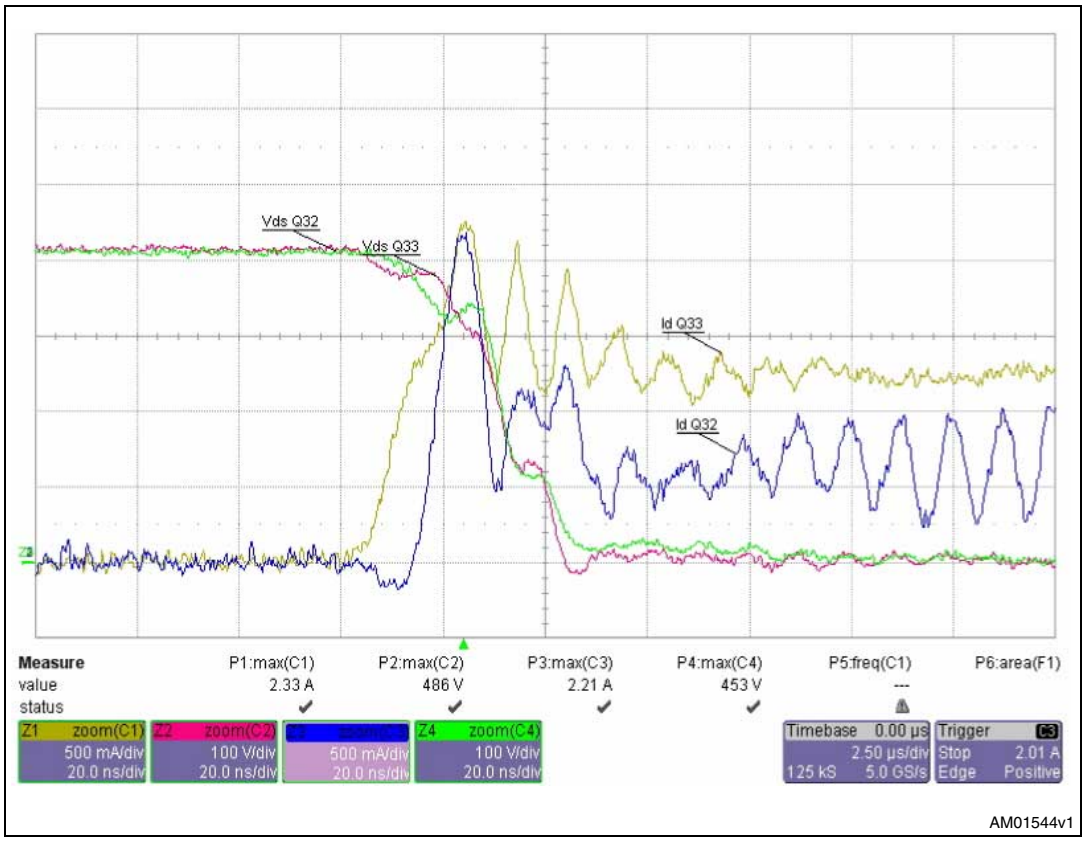
The primary contributors to current imbalance in power circuits are different drain or branch inductance and common source inductance. These "parasitic" inductances (labeled as Lp in *Figure 4*) are mainly generated by interconnection wiring and discrete components and have different effects depending on where they are situated. Thus the variation between branches is a function of layout symmetry and production tolerance. If we analyze a system that uses devices with similar electrical characteristics, the different device behaviors are linked to external parameters.

Figure 4. Parasitic inductance in a circuit



The impact due to the inductance in series to the gate terminal during the turn-on operation is a delay of the event. In fact, when the signal coming to the driver is applied to the gate, the inductance Lp in series generates an extra voltage that decreases the real voltage on the gate pin and consequently causes a delay of the operation. The same delay effects during turn-on are caused by the parasitic inductances on the drain and source pins. Also during turn-off operation, the impact due to the parasitic inductances is to generate a delay of the commutations. In the following figure, we can see how an external inductance introduced on the gate pin generates a delay on the drain current.

Figure 5. Details of current imbalance during turn-on due to external parasitic inductances



If we analyze a topology with two devices connected in a parallel configuration, where the current imbalance is due only to the external parasitic inductances, the typical waveforms are shown in the *Figure 5*.

Figure 6. Details of current imbalance during steady state operation due to the layout

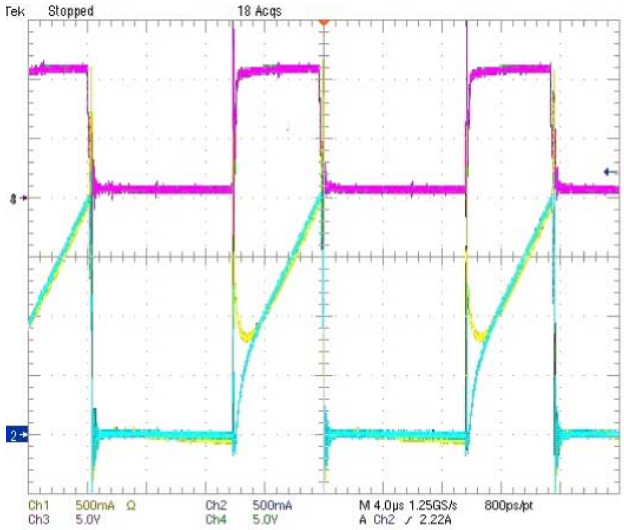


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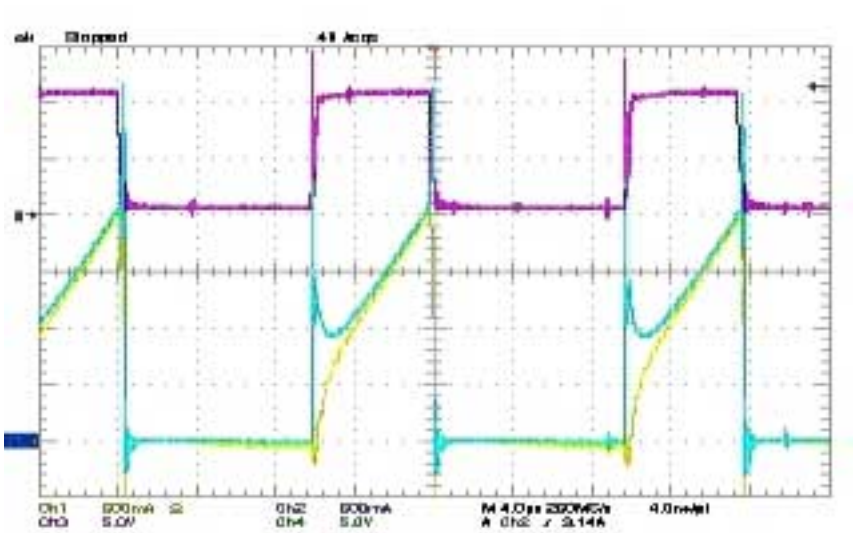
Figure 6 and *Figure 7* refer to the normal operation in a PFC configuration of two devices in parallel. The blue and yellow lines refer to the two currents on the devices, the green line to the voltage across the drain and source and fuchsia to the voltage across gate to source. In this case, devices with the same electrical characteristics are tested and as can be observed, if they change their position the waveforms remain the same. This confirms that the position and then the layout are responsible for the behaviors, so they are very important for the operation of parallel devices. In the following figure, the position of the two devices is inverted.

Figure 7. Current imbalance due to layout during steady state operation when the device position is changed



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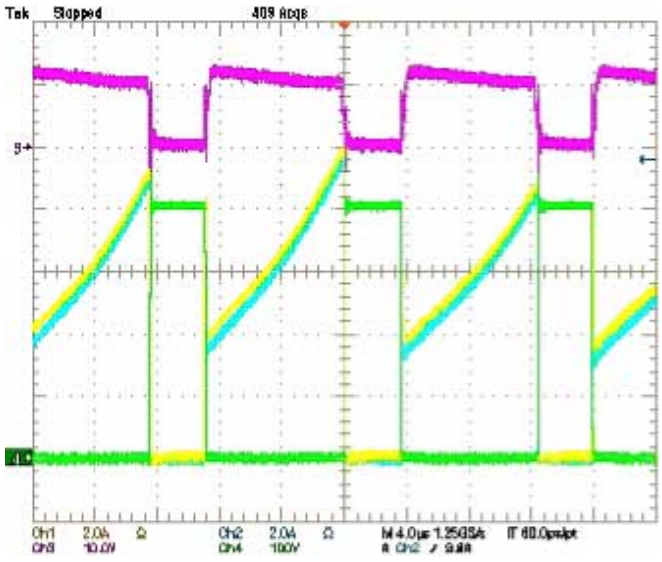
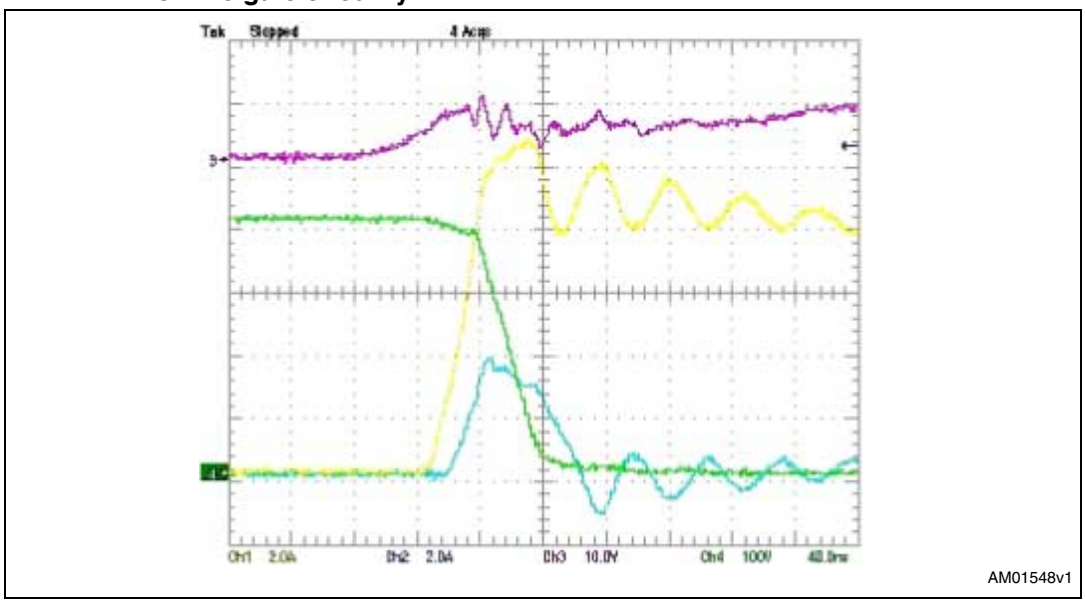
With the Q1 device in position A and Q2 in position B, the current relative to Q1 (yellow line) changes depending on its position, and in particular, during turn-on detail it is bigger than Q2. When Q1 is put in position B and Q2 in A, its current is lower than Q2. So, the device behaviors are linked to their positions. In this case it is necessary to compensate this difference or redesign the circuit to reduce the PCB differences. A deeper analysis has shown a small difference in the source path, a difference that caused unbalanced current during turn-on operation and then different working temperatures (if the devices are mounted on different heat-sinks). If the system arrives at a thermal balance, different working temperatures for the devices are the final results. Instead, when the circuit has very similar parameters in terms of electrical characteristics as the devices, layout considerations and so on, the currents and the relative waveforms are balanced as shown in *Figure 8*.

Figure 8. Details of current balance when circuit has very similar parameters



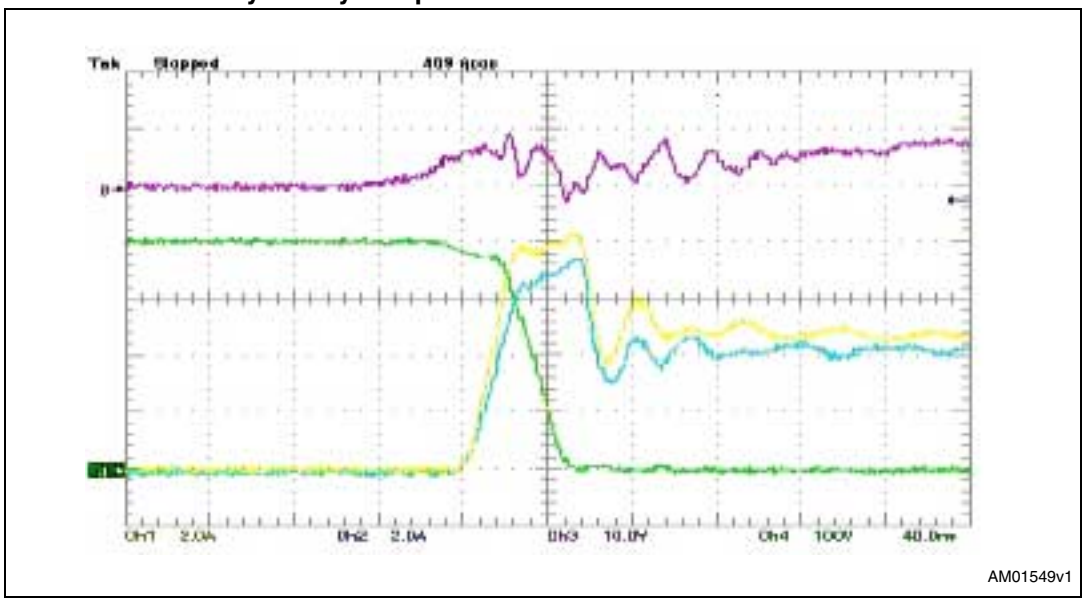
In the switching system, as seen previously, when the current imbalance is due principally at the voltage on the gate circuitry, main different happens not clear during the commutation; in fact, during this phase the variation between branches causes different voltage on the gate pin. If we look at the *Figure 9* and *Figure 10*, we can see the details during the switching on in two different conditions.

Figure 9. Details of current imbalance during turn-on due principally at the voltage on the gate circuitry



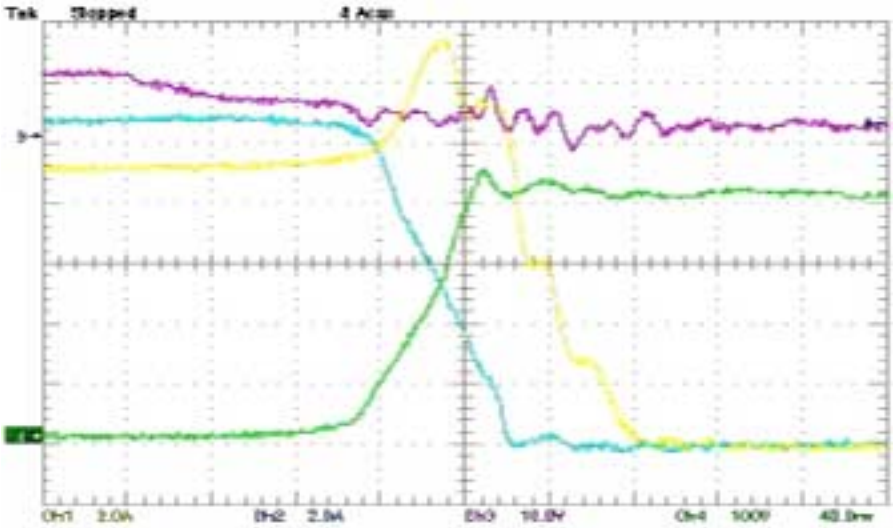
If there is some difference between the branches, the voltage across the gate pin of two devices is different and this causes a gap current during switching. In fact, if one device starts before the other, it brings all the current, generating imbalance. Instead, as we can see in *Figure 10*, if the conditions are the same for both devices the current imbalance is minimal.

Figure 10. Details of current imbalance during turn-on when the voltage on the gate circuitry is very comparable



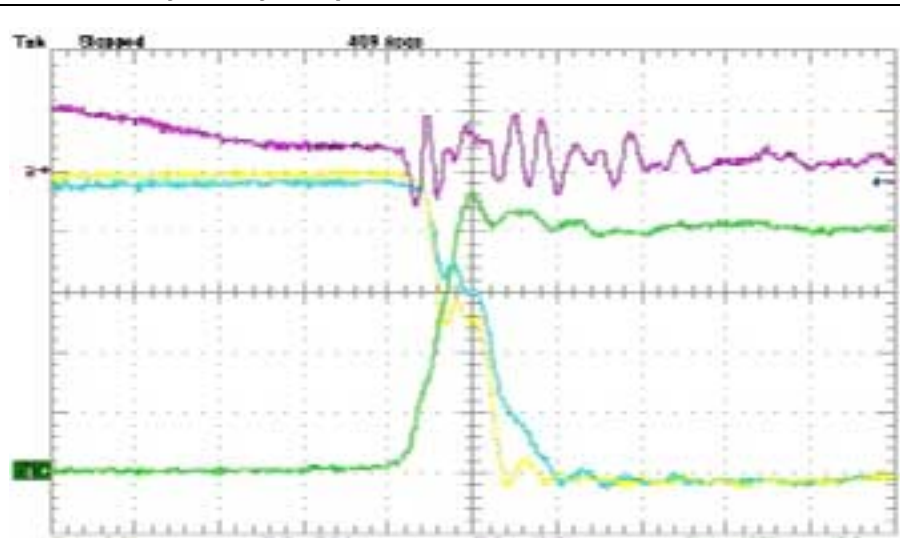
Like the turn-on details, we can also see similar behaviors for the currents during turn-off. In fact, the device with the lower $V_{THRESHOLD}$ value has a delayed switch-off compared to the other device, which for a short time carries the total current of the system. In *Figure 11* and *Figure 12* details relative to these instances are reported.

Figure 11. Details of current imbalance during turn-off due principally to the voltage on the gate circuitry



The switching losses during this instance can became very high and it can cause thermal runaway with consequent device failure (see *Figure 16*). Instead, if the two $V_{THRESHOLD}$ values are similar, the current profiles assume the same aspect (see *Figure 12*). During turn-off operations, the two devices switch in the same way and at the same time, sharing the current correctly.

Figure 12. Details of current imbalance during turn-off when the voltage on the gate circuitry is very comparable



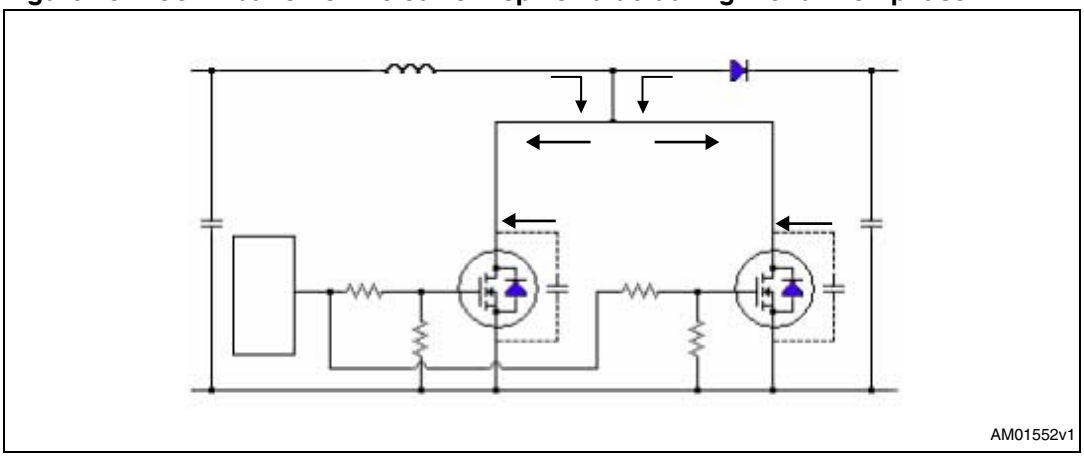
2.2 Gate circuitry

Another reason for unbalanced current in a parallel topology is the gate circuitry. If a common voltage source is used, the primary factor contributing to imbalance is mismatch between decoupling resistors (if they are used). Normally, in order to reduce the impact of the gate resistance, one can use different resistance for the drive gate circuit. In fact, if a device with a lower R_{gate} brings more current than the other, its temperature increases and consequently so does its $R_{DS(on)}$. This effect limits the current on the drain to source only during the conduction operation. If we look at the previous paragraph, we can note that the current imbalance is mainly present during the commutation and precisely during the plateau zone. In order to reduce the current imbalance, it is necessary to decrease the duration of the plateau by putting a resistor R_G with a lower value. The impact of this operation is oscillations on the gate pin, so the R_G value is a compromise between speed of the commutation and oscillations.

2.3 Influence of the boost diode in the current imbalance

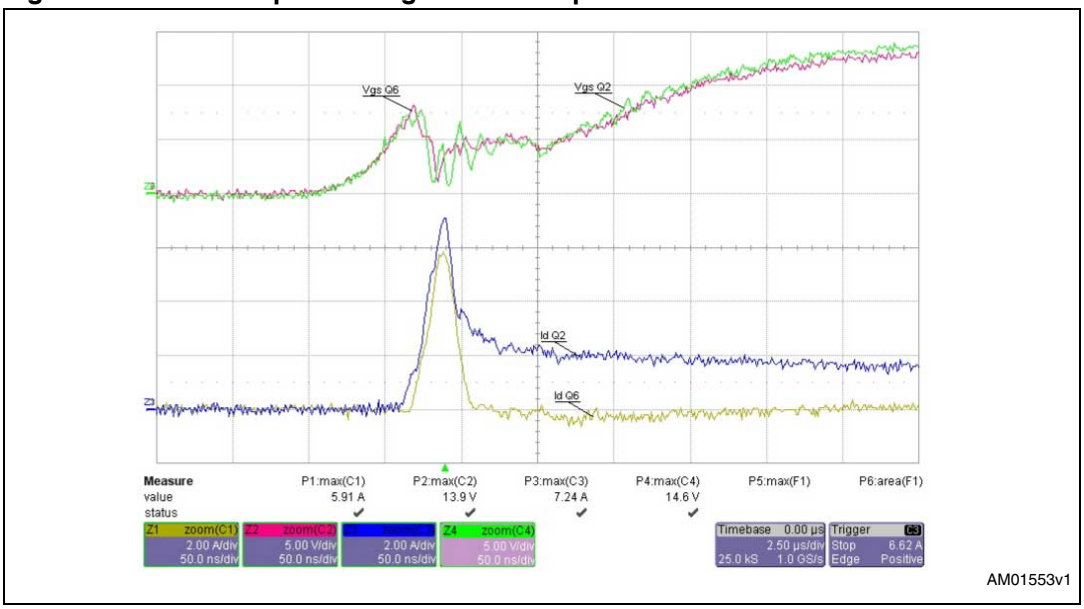
Among the key factors that influence current imbalances is the boost diode. In fact, the performance of this component are determinant during the turn-on operation of devices in a parallel configuration. The most important of the diode's characteristics for this topology is the recovery time (t_{rr}). In a PFC in boost topology, when the active device switches on, the current that was flowing to the boost diode has to flow through the device. The current value is made up of three components; the first is the current coming from the inductor, the second is the current coming from the recovery of the diode, while the last is the current from the output capacitances of the devices.

Figure 13. Contribution of the current spike value during the turn-on phase



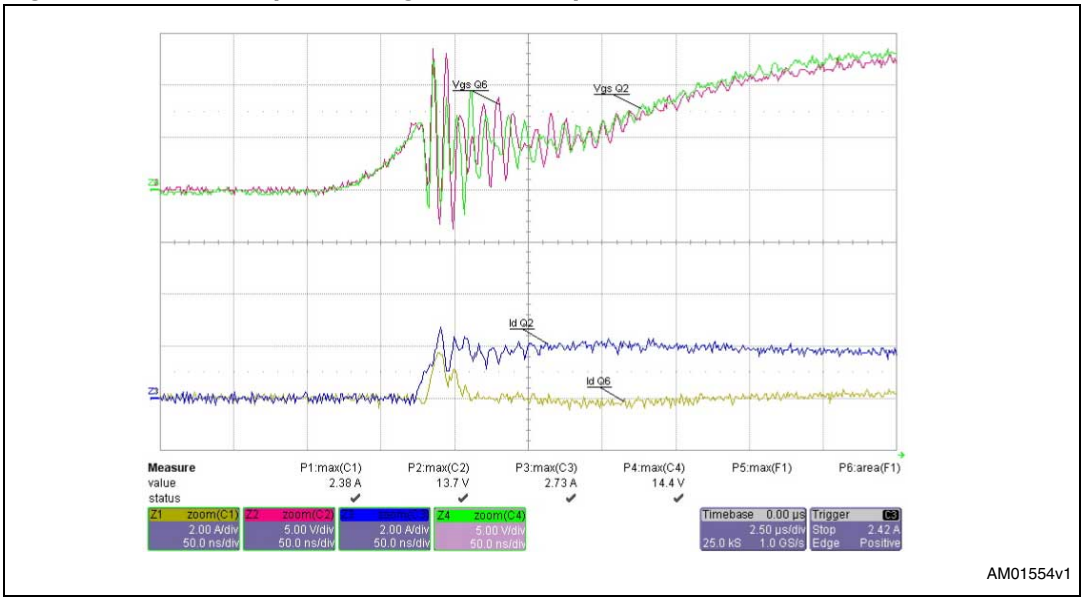
So, the contribution to the current spike value during the turn-on phase is due also to the intrinsic characteristics of the device. Even if devices with different V_{th} (around 500 mV) values are used, during turn-on operation a bigger difference in the current value of the peak is present if an ultra fast diode and a fast diode are used. In *Figure 14* and *Figure 15*, details during turn-on are shown.

Figure 14. Current spike during the turn-on phase when a fast diode is used



In *Figure 13*, an ultra fast diode is used, while in *Figure 14* a fast diode is used. In *Figure 13* we can see that a large current spike is present during the turn-on phase, compared with *Figure 14*. It is important to underline that the impact due to the boost diode is present only during the turn-on phase.

Figure 15. Current spike during the turn-on phase when an ultra fast diode is used



2.4 Temperature imbalance between devices

As explained in the previous paragraph, an important parameter for current imbalance in a parallel configuration is working temperature. Analytical proof of thermal instability is derived from the expression of the drain current I_D in the active region of the I_D-V_{DS} plane of a power MOSFET device. In this region, the drain current is independent of the drain-source voltage:

$$I_D = K' \cdot (V_{GS} - V_{Th})^2$$

where V_{th} is the threshold voltage. The constant K' depends on the device geometric characteristics and is given by:

$$K' = \frac{1}{2}\mu_c\left(\frac{W}{L}\right) \cdot C_{OX}$$

where:

- W: channel perimeter
- L: channel length
- μ_c: electron mobility
- C_{ox}: gate oxide capacitance

The current temperature coefficient at low drain current is related to geometrical and physical parameters of the device by:

$$\frac{\partial I_D}{\partial T} = 2k' \cdot (V_{GS} - V_{th}) \cdot \left|\frac{\partial V_{th}}{\partial T}\right| - (V_{GS} - V_{th})^2 \cdot \left|\frac{\partial K'}{\partial T}\right|$$

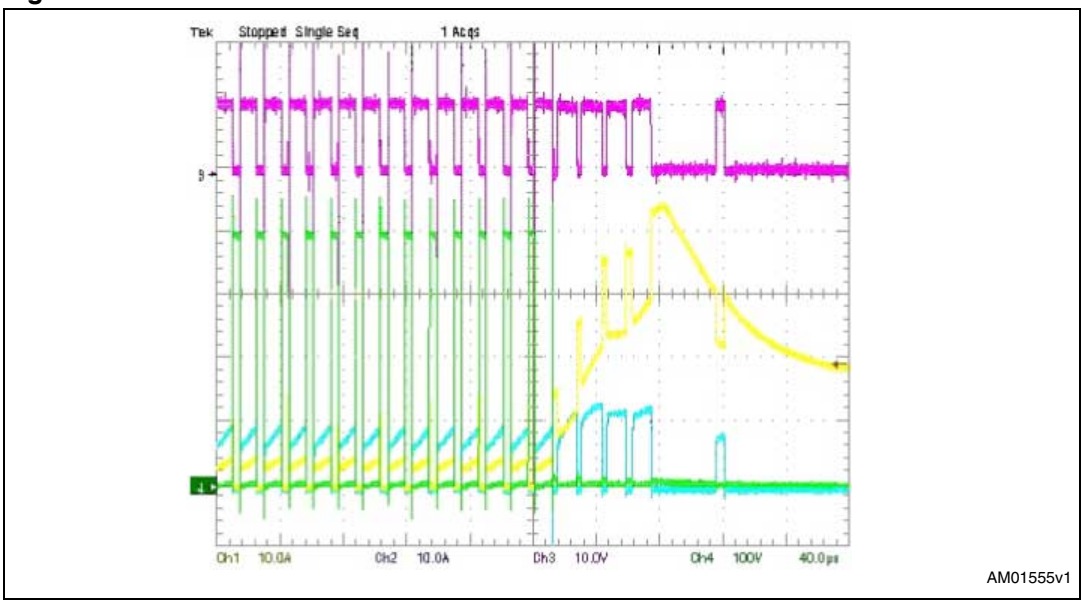
since both (∂V_{th}/ ∂T) and (∂K'/ ∂T) are negative.

2.5 Influence of the differences between the power circuit components

The principal factors linked to the temperature for this analysis are the threshold voltage and $R_{DS(on)}$. Each of the two factors operate in different ways. While an increasing temperature generates a decrease in threshold voltage, the $R_{DS(on)}$ increases with temperature. The effects of the two parameters are opposite. In fact, if the threshold voltage decreases, the device, in the same condition of V_{GS}, carries more current. However, more current means greater losses and consequently a higher temperature. This phenomenon is iterative (known as thermal runaway) and could cause the failure of the device. Losses linked to this parameter are evident during switching and in particular during turn-on and turn-off operations, and in a systems with high frequency they are highly important. When the temperature changes, the contribution linked to the RDS(on) parameter is different. This factor plays a fundamental role during the conduction phase. In fact, during this period, if the temperature increases, the $R_{DS(on)}$ also increases and this limits the current value during the conduction operation. So, while in a first phase the conduction losses are more significant than switching losses; when the temperature increases, the second become predominant over the first. In the end, the working temperature is a factor that plays an important role in the parallel configuration, and for this reason if the devices are mounted to

the same heat-sink, it is important to know their thermal distribution. In fact, two devices connected in parallel, but with different working temperatures, have different behaviors. The different working temperatures could be caused by other factors (another device mounted to the same heat-sink, different air flow by fan, etc.). Many PFC systems use the same heat-sink for power device and diode. In this case, the power device close to the diode shows a working temperature higher than the other. If the circuit does not have a feedback system, an increase in the temperature could cause failure of the system. In *Figure 16*, details of this phenomenon are shown.

Figure 16. Instant of failure

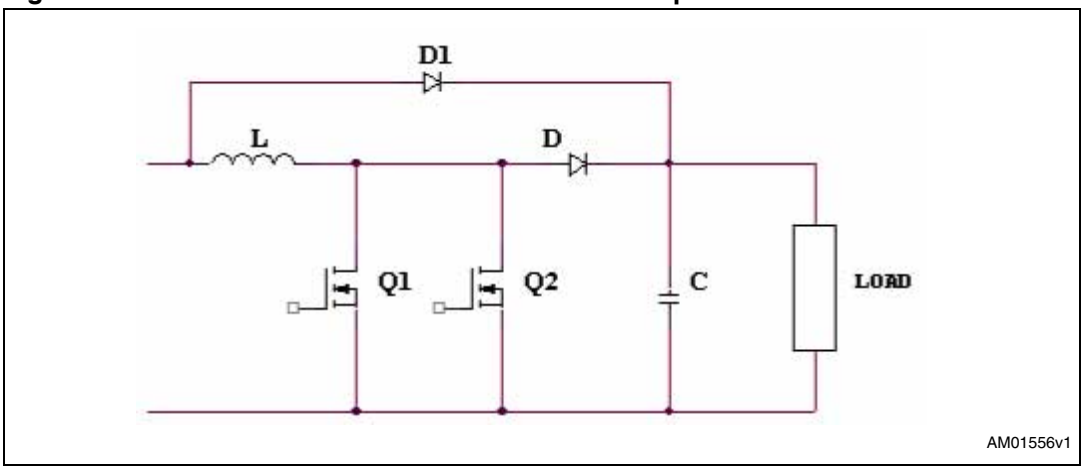


In the introduction of this document, the study was divided into two areas: the first, which has been explored in the previous paragraphs, is an analysis of current imbalances due to the external parameters of a power device. The second is an analysis of the intrinsic characteristics of a power MOSFET, which are predominant in the mismatching. In this section, we look at the influence of the voltage threshold $V_{GS(th)}$, $R_{DS(on)}$ and g_{fs} parameters.

2.6 Differences in the $V_{GS(th)}$

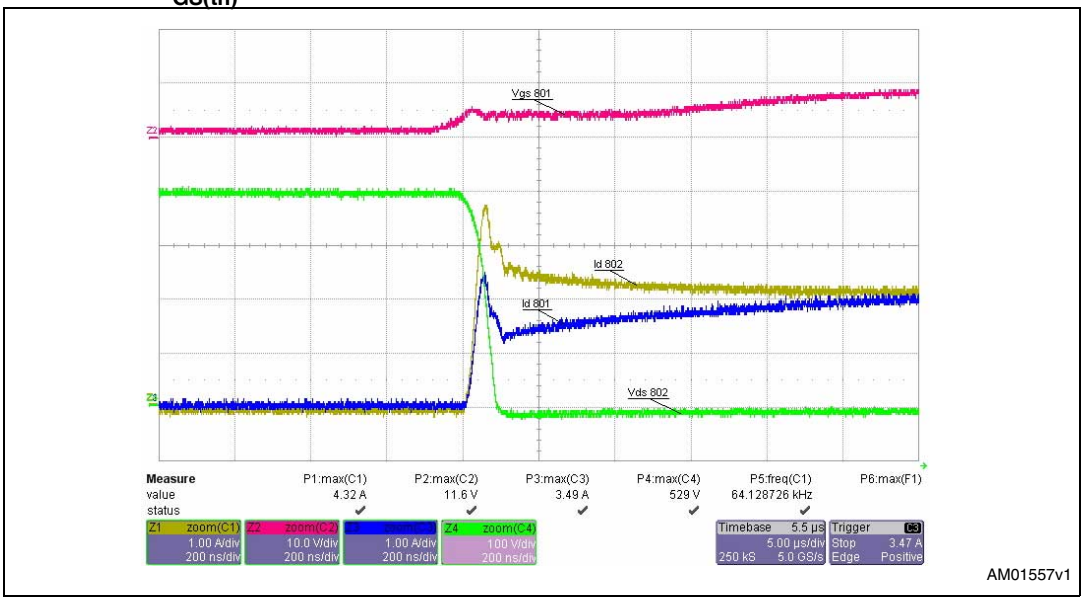
The following analysis refers to a system with two devices connected in parallel based on the schematic in *Figure 17*.

Figure 17. Schematics of two devices connected in parallel



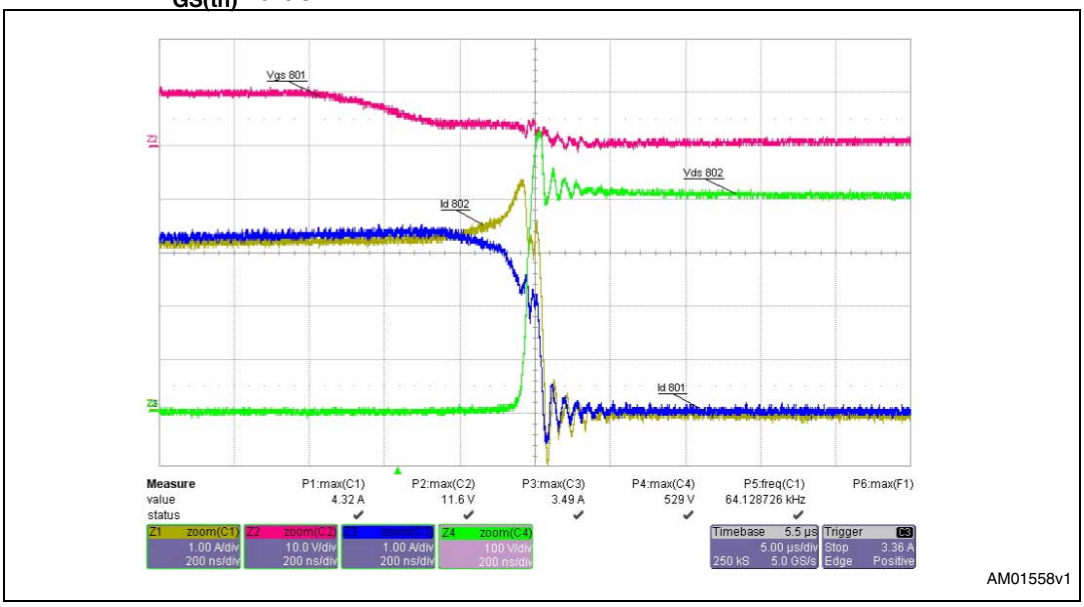
If we suppose the voltage threshold of Q1 is lower than Q2, during the turn-on phase device Q1 starts to turn-on before Q2. This means that for a short time, it brings more current than the other and consequently it has greater power losses and higher temperature. *Figure 18* provides details of this occurrence.

Figure 18. Details of current imbalance during turn-on when there is a difference in $V_{GS(th)}$ value



The same approach can be taken during the turn-off phase. The device with a higher voltage threshold switches off before than other (*Figure 19*). In this case, all the current must be brought by the device with the lower $V_{GS(th)}$ causing increased power losses. As can be observed, in a parallel connection between two devices, the device with the lower $V_{GS(th)}$ has more power losses both at turn-on and turn-off, and its working temperature is also higher.

Figure 19. Details of current imbalance during turn-off when there is a difference in $V_{GS(th)}$ value

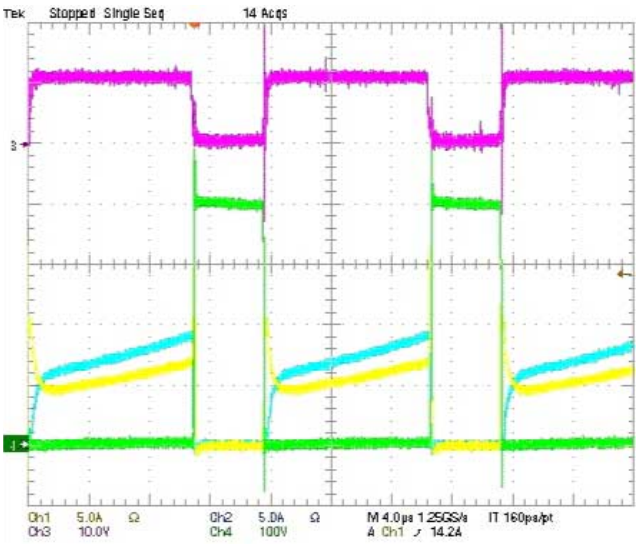


It is important to highlight that the voltage spread isn't the only cause of failure of the device. In fact, in a right thermal project, devices with high spread of voltage threshold work fine in each condition.

2.7 Differences in $R_{DS(on)}$

In order to check the impact due to the $R_{DS(on)}$, we analyze the conduction phase only. Referring to the schematics shown in *Figure 18*, if we suppose that the devices Q1 and Q2 have a different $R_{DS(on)}$, during the conduction phase the system can be represented by two resistors with different values connected in parallel. If resistor R1 has a lower value than R2, more current flows through it. In the following figure, details relative to this situation are reported.

Figure 20. Details of current imbalance due to a difference in $R_{DS(on)}$ value



This current imbalance causes an increase in power losses and consequently an increase of its working temperature. Since the thermal coefficient for the resistance is positive, the resistance increases in value, limiting the current with a negative feedback. If the number of devices in parallel is high, this process is very quick.

2.8 Influence of the g_{fs} parameter

In the previous paragraphs we have seen how current imbalance is present during the commutation and in particular during the plateau zone. During this phase, a parameter that influences behaviors is the g_{fs}. If we look *Figure 20*, during the commutation the voltage V_{GS} value is around 5 V. If we observe the transfer characteristics reported in *Figure 22*, we can see that at V_{GS} = 5 V, the current may be different.

Figure 21. g_{fs} curves for devices with comparable g_{fs} values

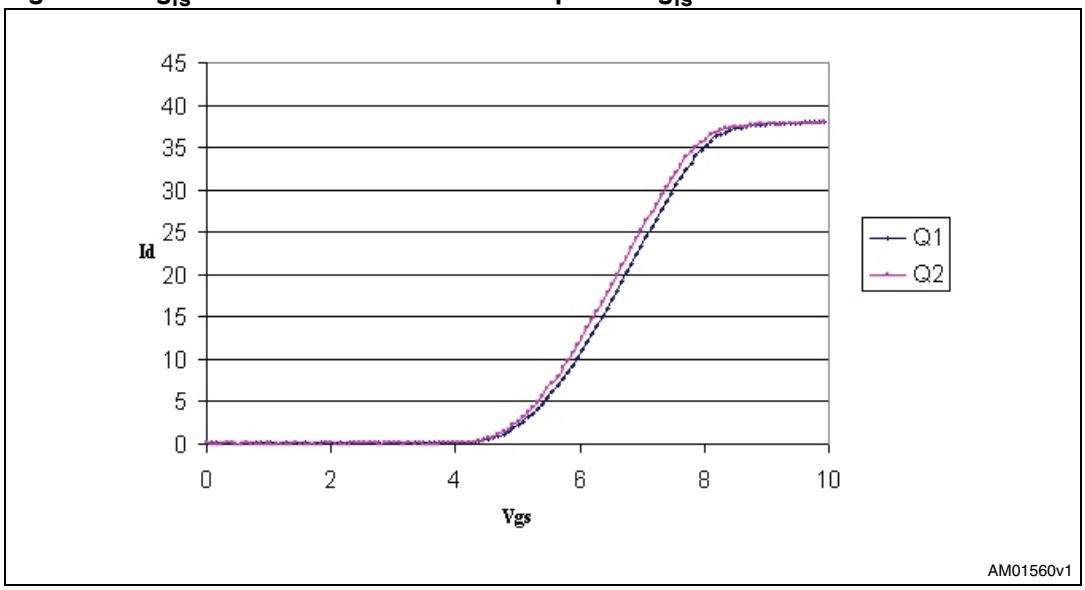


Figure 22. g_{fs} curves for devices with different g_{fs} values

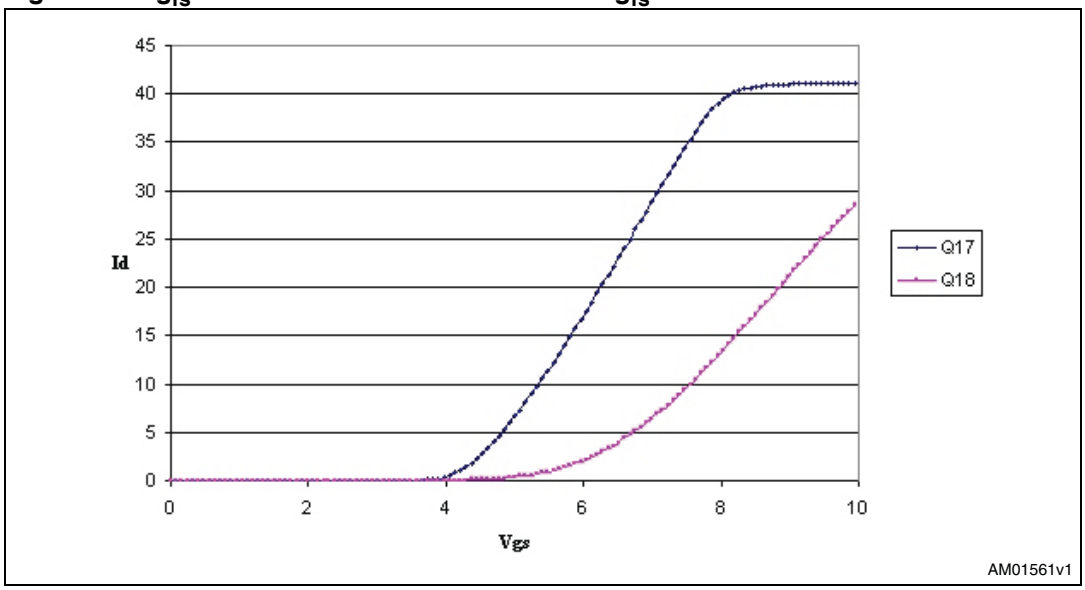
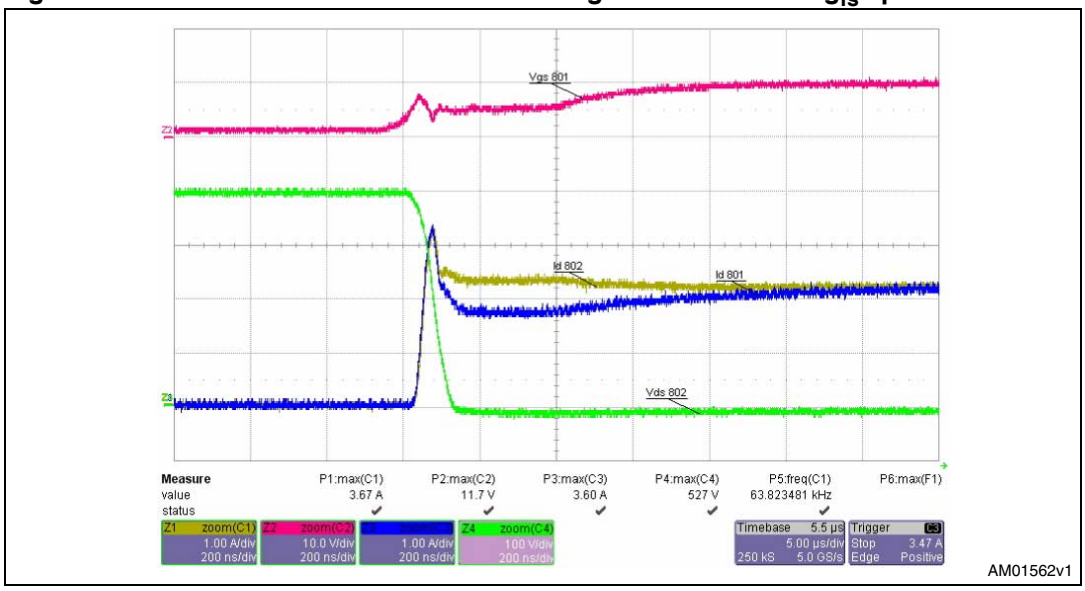


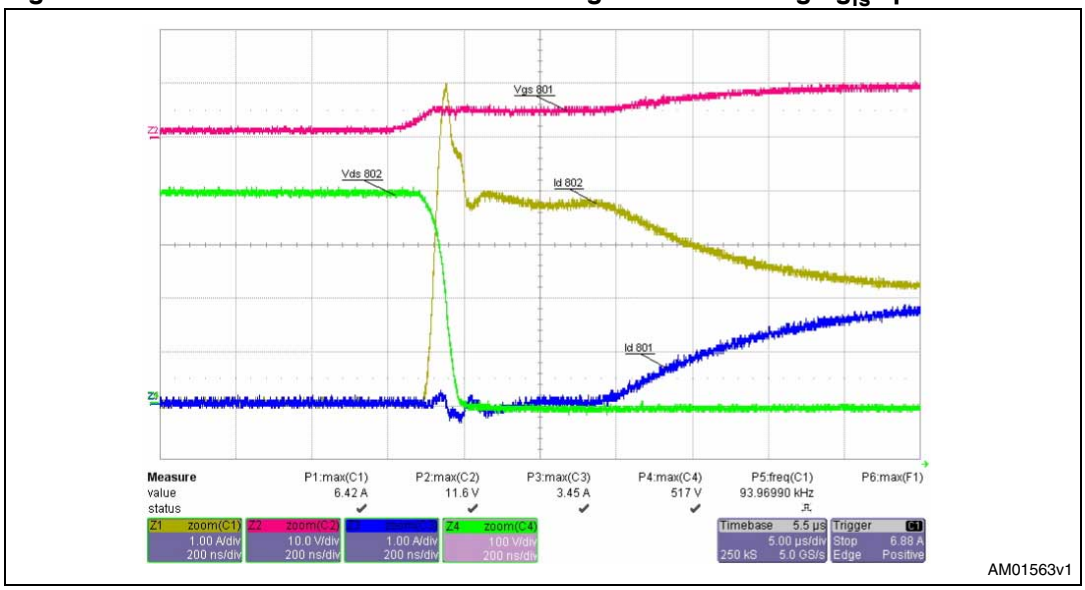
Figure 21 and *Figure 22* refer to the transfer characteristics of two pair of devices, while in *Figure 23* and *Figure 24*, we can observe the relative waveforms. A large current imbalance can be seen if there is a big difference in the transfer characteristics. Thus, the g_{fs} parameter is also responsible for the current imbalance both during turn-on and turn-off operations.

Figure 23. Details of current imbalance during turn-on with low g_{fs} spread



While, during turn-on operation with high g_{fs} spread, we have:

Figure 24. Details of current imbalance during turn-on with high g_{fs} spread



From this analysis it is very evident the impact due to the g_{fs} parameter. In order to decrease its influence, it is very important to reduce the spread during the production.

3 Conclusion

The analyses performed have shown some factors responsible for the current imbalance in a parallel connection between two power MOSFETs. Some intrinsic parameters show a remarkable impact on device operation, such as differences in the $V_{GS(th)}$ and $R_{DS(on)}$, and the influence of the g_{fs} parameter. External parameters also playing a fundamental role in current imbalance are differences between power circuit components, gate circuitry, the influence of the boost diode and temperature imbalance between devices. In order to develop a robust design the production spreads and the electrical and thermal behaviors of the system must be taken into account.

4 Revision history

Table 1. Document revision history

Date	Revision	Changes
29-Jul-2009	1	Initial release.