JEWEL HILL ELECTRONIC CO.,LTD.

SPECIFICATIONS FOR LCD MODULE

Module No. JHB7021A

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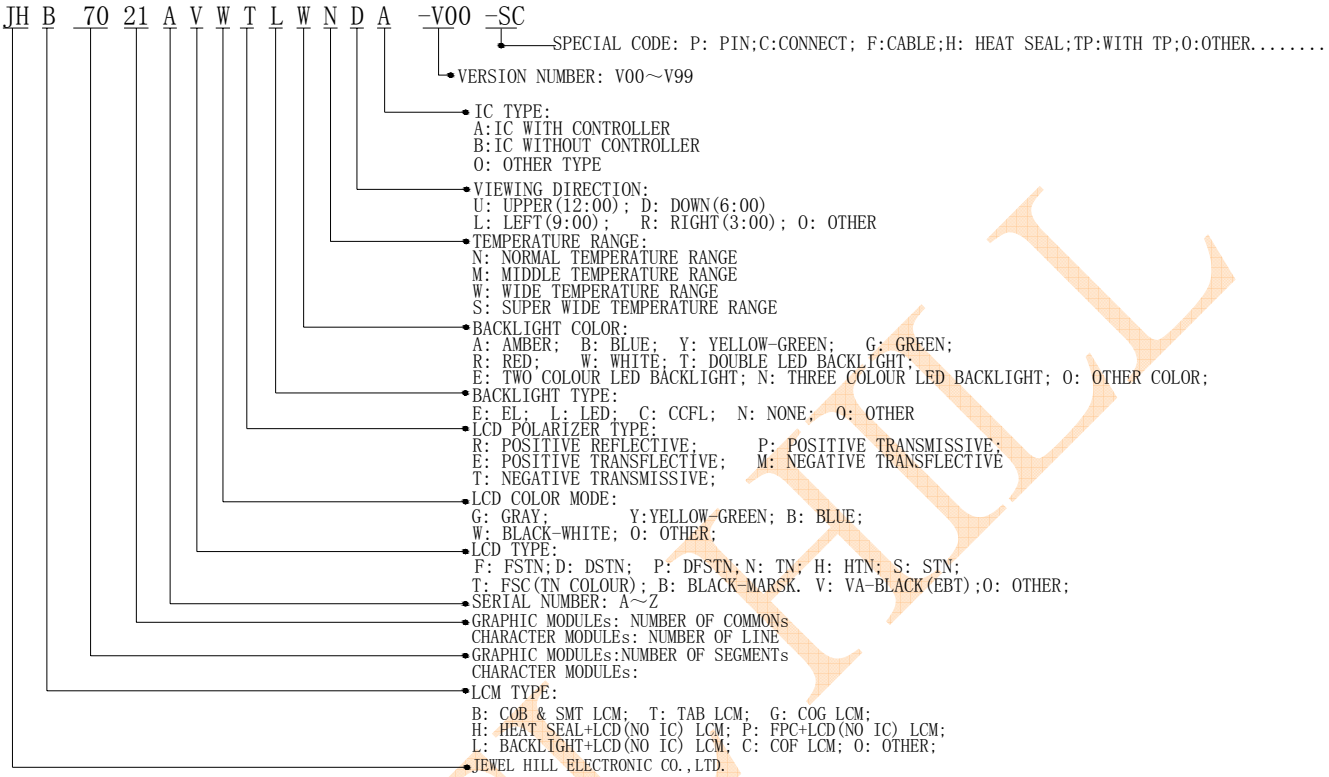
TABLE OF CONTENTS

LCM Number System.



1.GENERAL DESCRIPTION.

The JHB7021A is a segments LCD module. It has a V.A(EBT) panel composed of 27segments and 4 commons. The LCM can be easily accessed by micro-controller via serial interface.

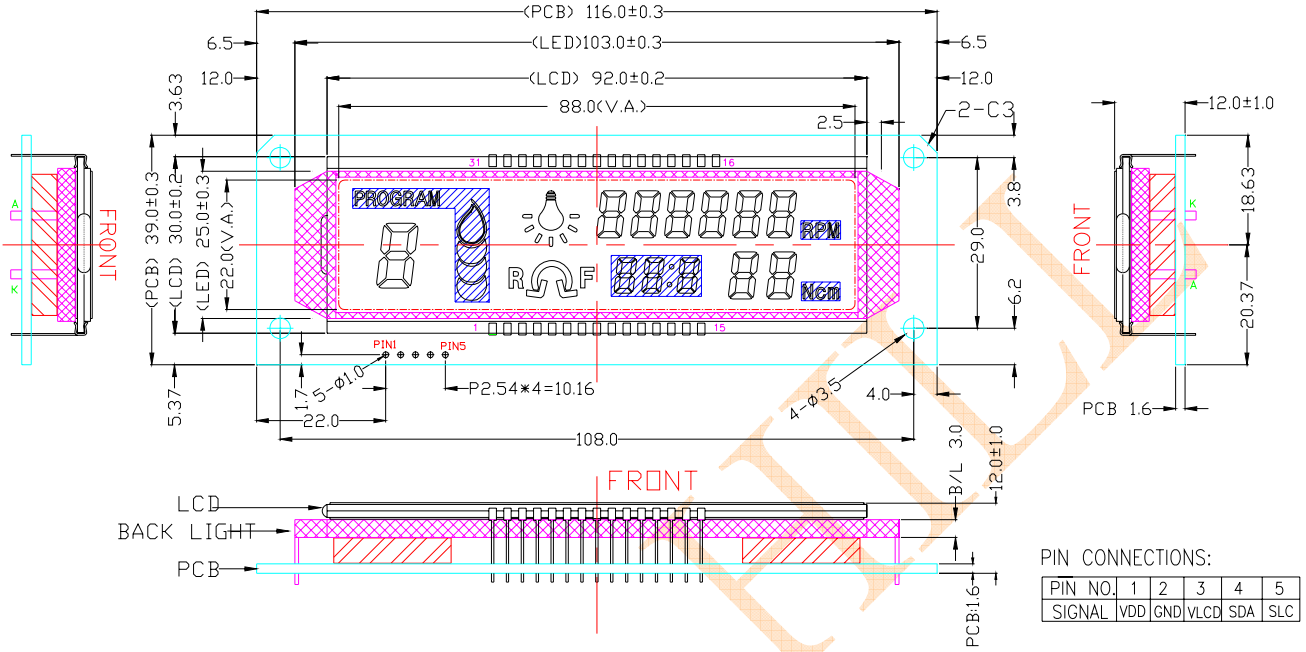
2.FEATURES.

Display Mode	V.A(EBT)Negative Transmissive Module
Display Format	segments 27 x 4 commons
Input Data	I2C serial data input from MPU
Multiplexing Ratio	1/4 Duty
Bias	1 /3 Bias
Viewing Direction	6 O'clock
Backlight	LED（White）

3.MECHANICAL SPECIFICATION.

Item	Specifications	Unit
Dimensional outline	116.0x 39.0 x 12.0	mm
Resolution	27segs x 4coms	-
Viewing area	88.0(W) x 22.0(H)	mm

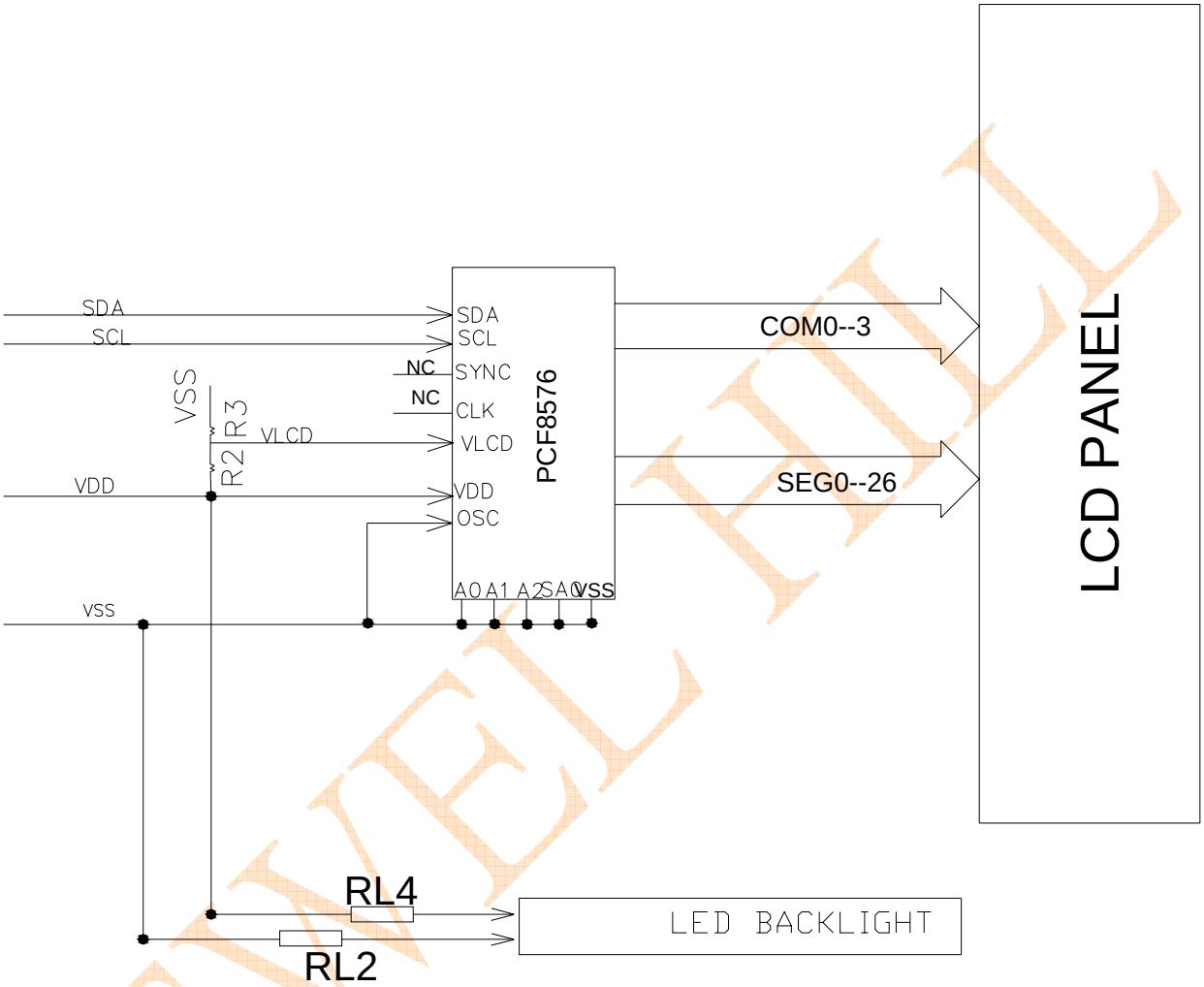
4.MECHANICAL DIMENSION.



PIN CONNECTIONS:

PIN NO.	1	2	3	4	5
SIGNAL	VDD	GND	VLCD	SDA	SLC

5.BLACK DIAGRAM.



6.INTERFACE PIN CONNECTIONS.

Pin No.	Symbol	Description
1	VDD	Power supply for positive (5V)
2	GND	Power supply for Ground (0V)
3	VLCD	NC. inside adjust voltage with (R2,R3).
4	SDA	I2C-bus serial data input/output
5	SLC	I2C-bus serial clock input

7.ELECTRICAL CHARACTERISTIC.

(1)MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit	Note
Supply voltage	V_{DD} - Vss	-0.5	8.0	V	
	V_{OP}	VDD-8.0	VDD	V	
Input Voltage	V_{IN}	VSS-0.8	8.0	V	
Operating temperature	T_{OPR}	0	+50	℃	
Storage temperature	T_{STR}	-10	+60	℃	
Humidity	---	---	90	%RH	

(2) DC CHARACTERISTICS.

VDD=+5.0V±10%, Ta=0℃ to +50℃

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	-	4.8	5.0	5.2	V
Supply Current	I_{DD}	VDD=5.0V	-	1.2	1.5	mA
Input Voltage	V_{IH}	VDD=5.0V	0.7VDD	-	VDD	V
Output voltage	V_{OH}	I_{OH}=-0mA	VDD-0.05	-	-	V
	V_{OL}	I_{OL}=0mA		-	0.05	V
LCD Driving Voltage	V_{OP}	VOP=VDD-VLCD	4.2	4.5	4.8	V
Back light Supply Voltage	Vf	If=60mA	4.8	5.0	5.2	V
Back light Supply Current	If	Vf=5.0V	-	60	80	mA

8. DRIVER IC FUNCTION DESCRIPTION.

The PCF8576C is a versatile peripheral device designed to interface to any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576C depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.4.

The host microprocessor/microcontroller maintains the 2-line I²C-bus communication channel with the PCF8576C. The internal oscillator is selected by tying OSC (pin 6) to V_{SS} (pin 11). The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

Table 1 Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		14-SEGMENTS ALPHANUMERIC		DOT MATRIX
BACKPLANES	SEGMENTS	DIGITS	INDICATOR SYMBOLS	CHARACTERS	INDICATOR SYMBOLS	
4	160	20	20	10	20	160 dots (4 × 40)
3	120	15	15	8	8	120 dots (3 × 40)
2	80	10	10	5	10	80 dots (2 × 40)
1	40	5	5	2	12	40 dots (1 × 40)

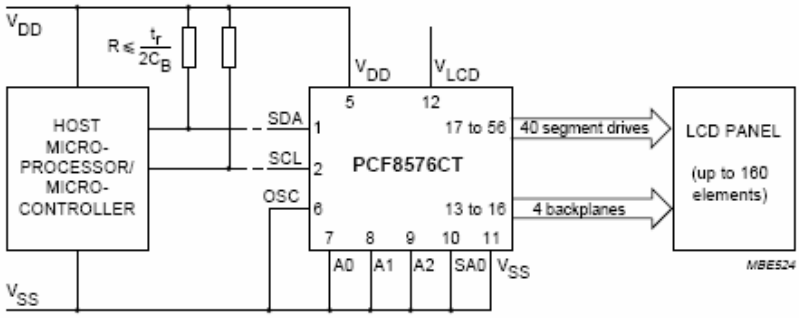


Fig.4 Typical system configuration.

8. 1 Power-on reset

At power-on the PCF8576C resets to a starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with ⅓bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I²C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

8. 2 LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of the circuit to provide a ½bias voltage level for the 1 : 2 multiplex configuration.

8. 3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} > 3V_{th}$ approximately.

Multiplex drive ratios of 1 : 3 and 1 : 4 with ½bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3}$ = 1.732 for 1 : 3 multiplex or $\frac{\sqrt{21}}{3}$ = 1.528 for 1 : 4 multiplex).

The advantage of these modes is a reduction of the LCD full-scale voltage V_{op} as follows:

- 1 : 3 multiplex (½bias):

  $V_{op} = \sqrt{6} \times V_{off(rms)} = 2.449\ V_{off(rms)}$

- 1 : 4 multiplex (½bias):

  $V_{op} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when ⅓bias is used.

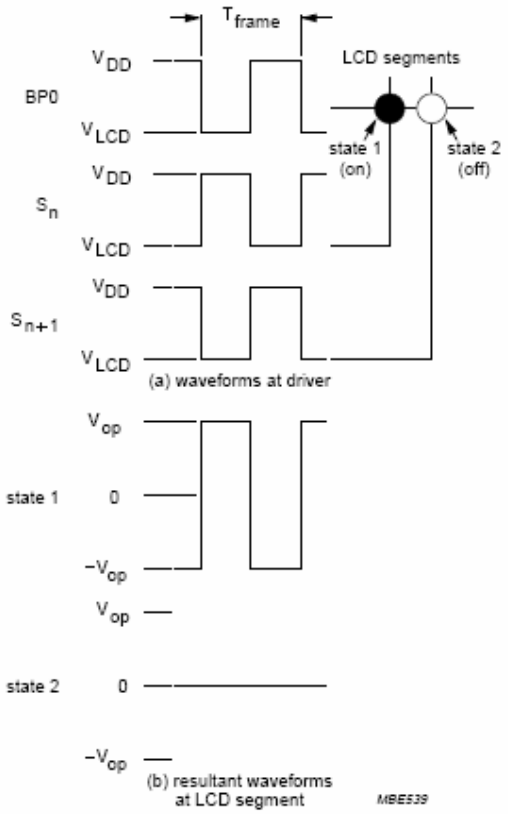
Table 2 Preferred LCD drive modes: summary of characteristics

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on(rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
static	1	2	static	0	1	∞
1 : 2	2	3	½	0.354	0.791	2.236
1 : 2	2	4	⅓	0.333	0.745	2.236
1 : 3	3	4	⅓	0.333	0.638	1.915
1 : 4	4	4	⅓	0.333	0.577	1.732

8.4 LCD Driver mode waveforms

8.4.1. STATIC DRIVER MODE

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.5.



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = V_{op}$

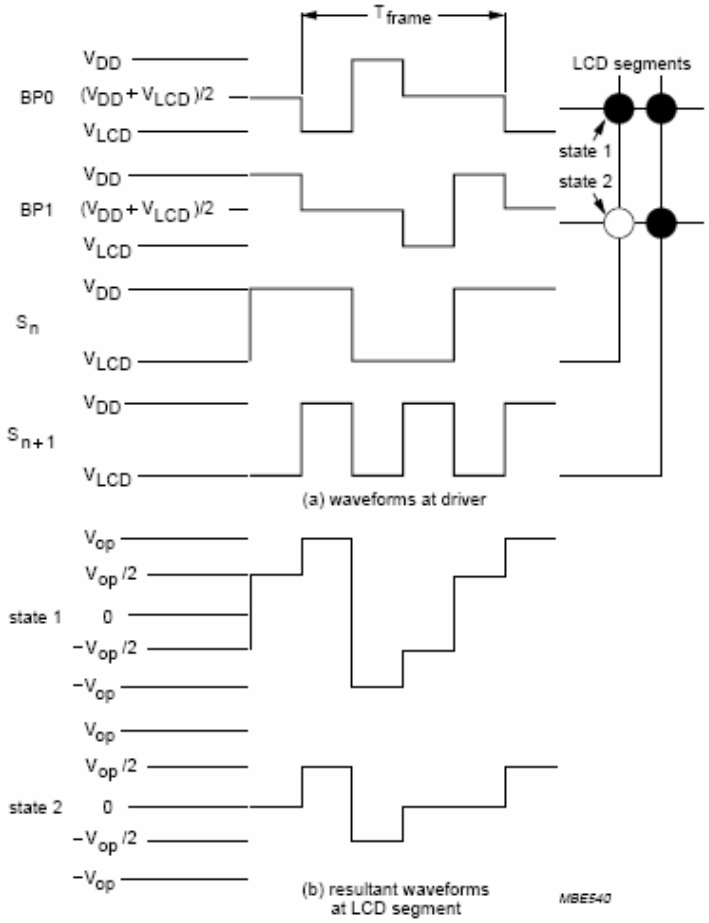
$V_{state2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off(rms)} = 0\ V$

Fig.5 Static drive mode waveforms ($V_{op} = V_{DD} - V_{LCD}$).

8.4.2. 1:2 MULTIPLEX DRIVER MODE

When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies. The PCF8576C allows use of ½bias or ⅓bias in this mode as shown in Figs 6 and 7.



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.791V_{op}$

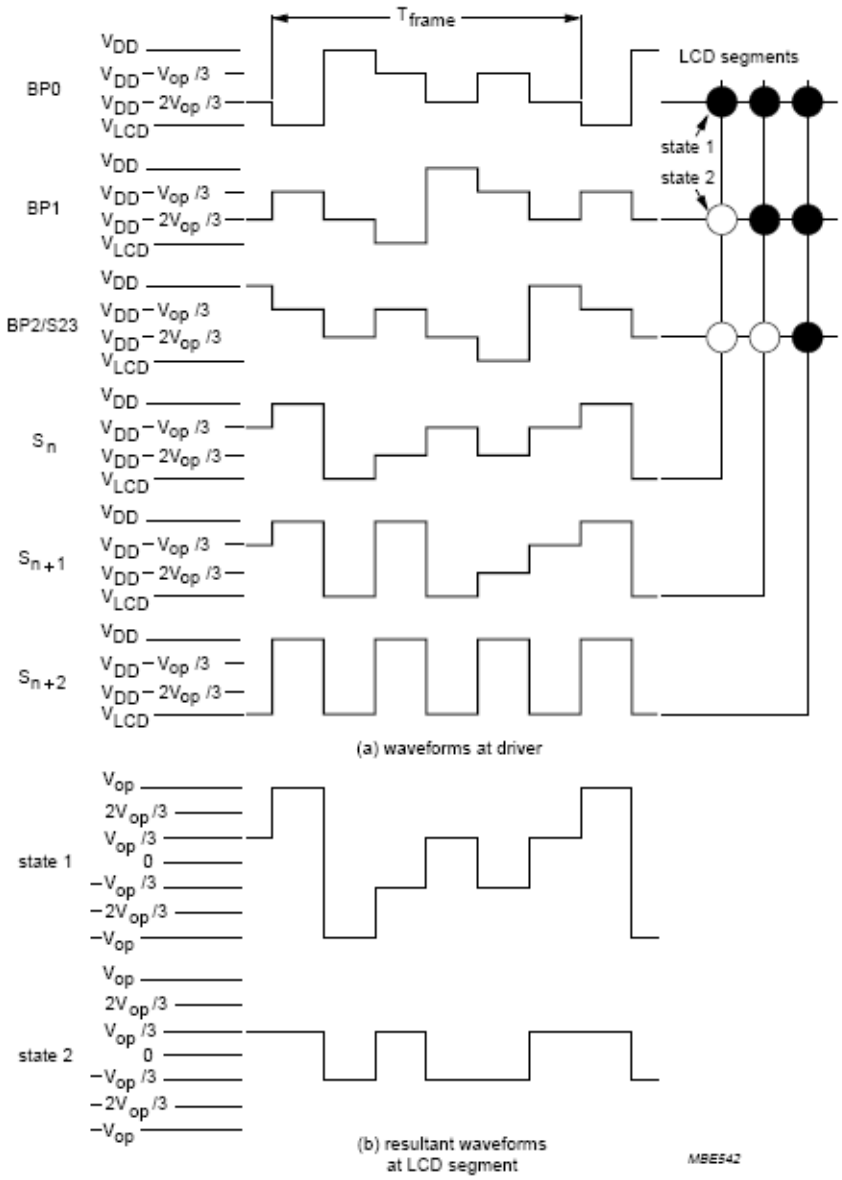
$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.354V_{op}$

Fig.6 Waveforms for the 1 : 2 multiplex drive mode with ½bias ($V_{op} = V_{DD} - V_{LCD}$).

8.4.3. 1:3 MULTIPLEX DRIVER MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex drive mode applies, as shown in Fig.8.



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.638V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.8 Waveforms for the 1 : 3 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

8.4.4. 1:4 MULTIPLEX DRIVER MODE

When four backplanes are provided in the LCD, the 1 : 4 multiplex drive mode applies, as shown in Fig.9.

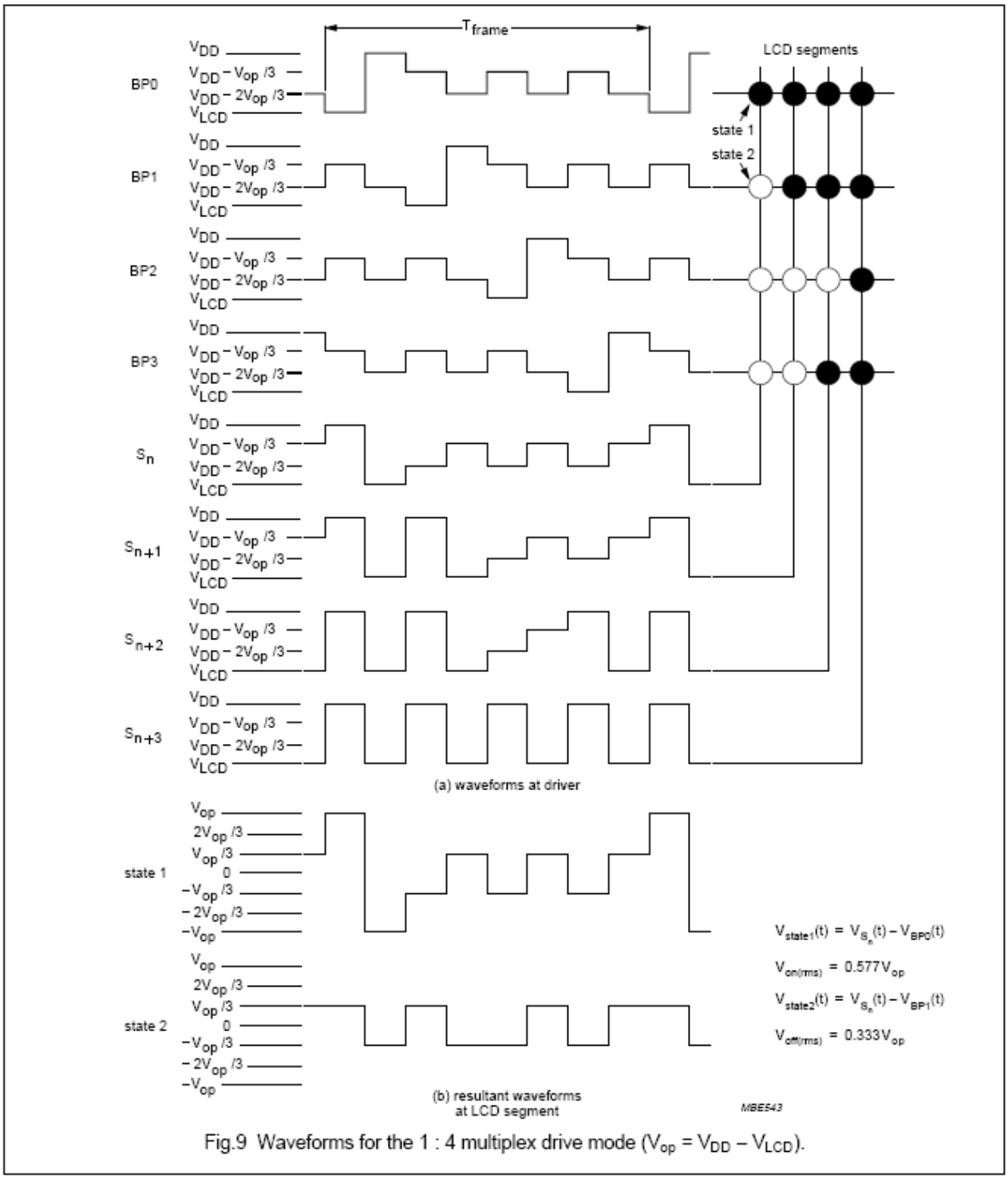


Fig.9 Waveforms for the 1 : 4 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

8.5 Oscillator

8.5.1 Internal clock

The internal logic and the LCD drive signals of the PCF8576C are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, OSC (pin 6) should be connected to V_{SS} (pin 11). In this event, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s or PCF8576Cs in the system.

Note that the PCF8576C is backwards compatible with the PCF8576. Where resistor R_{osc} to V_{SS} is present, the internal oscillator is selected.

8.5.2 External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{clk}) determines the LCD frame frequency and the maximum rate for data reception from the I²C-bus. To allow I²C-bus transmissions at their maximum data rate of 100 kHz, f_{clk} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

8.6 Timing

The timing of the PCF8576C organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576Cs in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (see Table 3). The frame frequency is set by the MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I²C-bus.

When a device is unable to digest a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I²C-bus but no data loss occurs.

8.7 Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

8.8 Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

8.9 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open-circuit.

8.10 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open-circuit. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

8.11. Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (see Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8576C the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode.
To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses.

In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Table 3 LCD frame frequencies

PCF8576C MODE	FRAME FREQUENCY	NOMINAL FRAME FREQUENCY (Hz)
Normal mode	$\frac{f_{clk}}{2880}$	64
Power-saving mode	$\frac{f_{clk}}{480}$	64

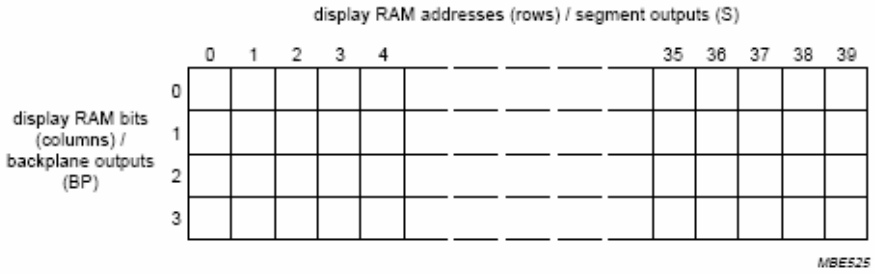


Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

8.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.11. The data pointer is automatically incremented in accordance with the chosen LCD configuration. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

8.13 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place.
The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576C occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

8.14 Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.
In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 and 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576C includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

8.15 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independent of the output bank selector.

8.16 Blinker

The display blinking capabilities of the PCF8576C are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads.

By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	POWER-SAVING MODE RATIO	NOMINAL BLINKING FREQUENCY
Off	–	–	blinking off
2 Hz	$\frac{f_{clk}}{92160}$	$\frac{f_{clk}}{15360}$	2 Hz
1 Hz	$\frac{f_{clk}}{184320}$	$\frac{f_{clk}}{30720}$	1 Hz
0.5 Hz	$\frac{f_{clk}}{368640}$	$\frac{f_{clk}}{61440}$	0.5 Hz

9. INSTRUCTION DESCRIPTION.

COMMAND	OPCODE								OPTIONS	DESCRIPTION
MODE SET	C	1	0	LP	E	B	M1	M0	Table 6	Defines LCD drive mode.
									Table 7	Defines LCD bias configuration.
									Table 8	Defines display status. The possibility to disable the display allows implementation of blinking under external control.
									Table 9	Defines power dissipation mode.
LOAD DATA POINTER	C	0	P5	P4	P3	P2	P1	P0	Table 10	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses.
DEVICE SELECT	C	1	1	0	0	A2	A1	A0	Table 11	Three bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of eight hardware subaddresses.
BANK SELECT	C	1	1	1	1	0	I	O	Table 12	Defines input bank selection (storage of arriving display data).
									Table 13	Defines output bank selection (retrieval of LCD display data). The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes.
BLINK	C	1	1	1	0	A	BF1	BF0	Table 14	Defines the blinking frequency.
									Table 15	Selects the blinking mode; normal operation with frequency set by BF1, BF0 or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes.

Table 6 Mode set option 1

LCD DRIVE MODE		BITS	
DRIVE MODE	BACKPLANE	M1	M0
Static	1 BP	0	1
1 : 2	MUX (2 BP)	1	0
1 : 3	MUX (3 BP)	1	1
1 : 4	MUX (4 BP)	0	0

Table 7 Mode set option 2

LCD BIAS	BIT B
⅓bias	0
½bias	1

Table 8 Mode set option 3

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 9 Mode set option 4

MODE	BIT LP
Normal mode	0
Power-saving mode	1

Table 10 Load data pointer option 1

DESCRIPTION	BITS					
6 bit binary value of 0 to 39	P5	P4	P3	P2	P1	P0

Table 11 Device select option 1

DESCRIPTION	BITS		
3 bit binary value of 0 to 7	A0	A1	A2

Table 12 Bank select option 1

STATIC	1 : 2 MUX	BIT I
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 13 Bank select option 2

STATIC	1 : 2 MUX	BIT O
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 14 Blink option 1

BLINK FREQUENCY	BITS	
	BF1	BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 15 Blink option 2

BLINK MODE	BIT A
Normal blinking	0
Alternation blinking	1

10.INTERFACE WITH MPU.

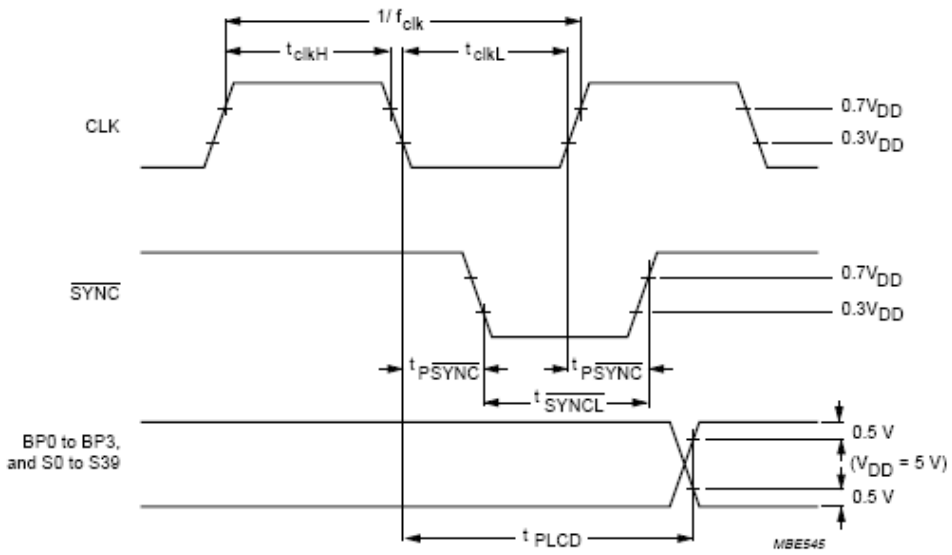


Fig.21 Driver timing waveforms.

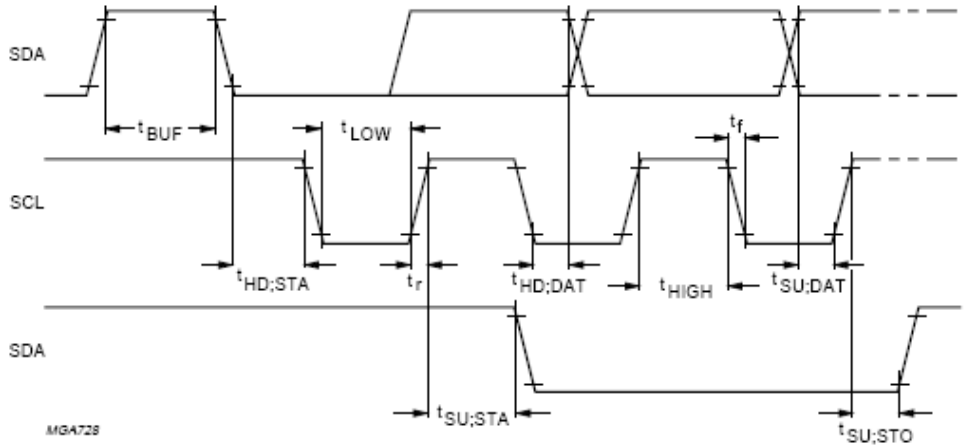
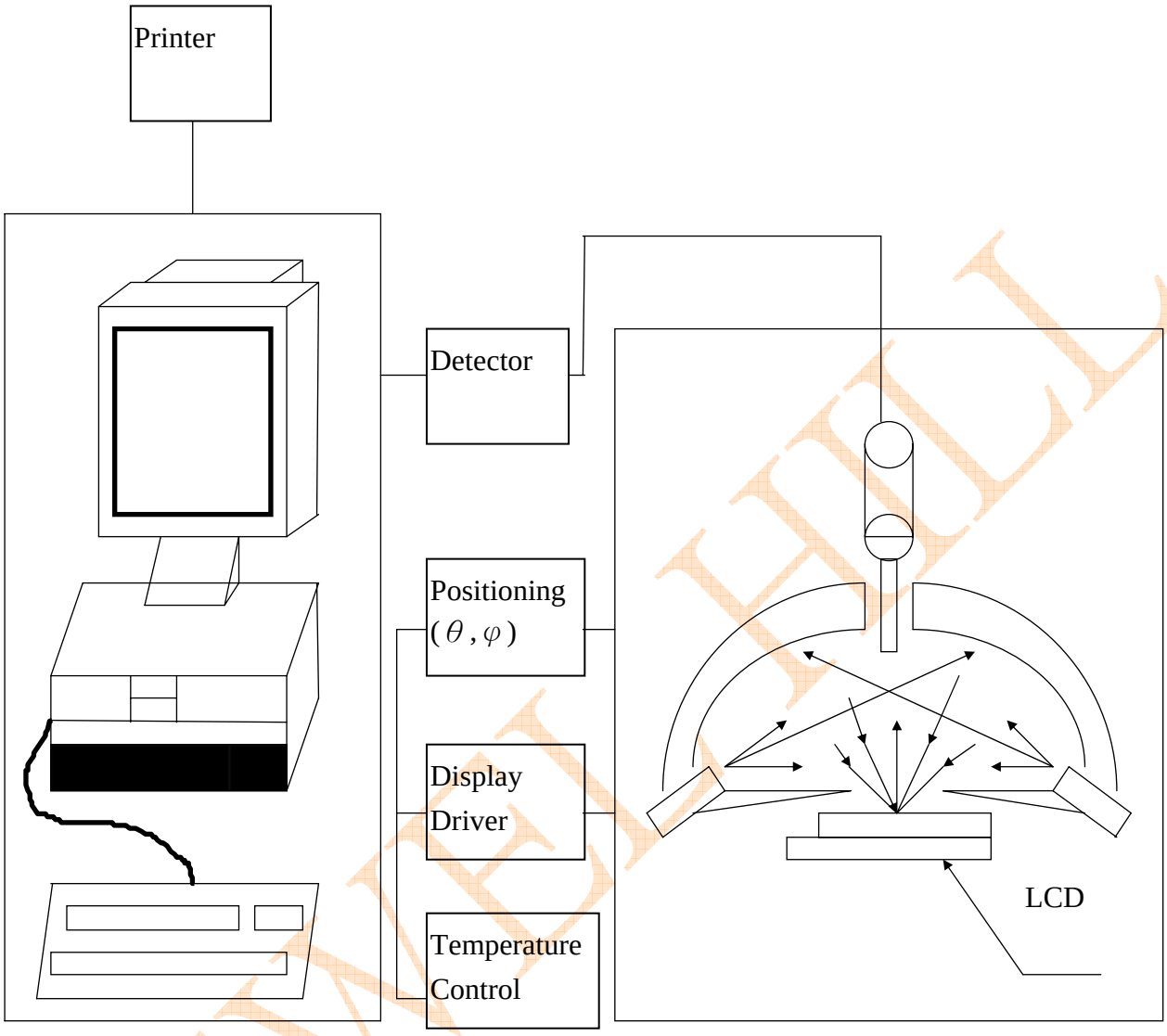


Fig.22 I²C-bus timing waveforms.

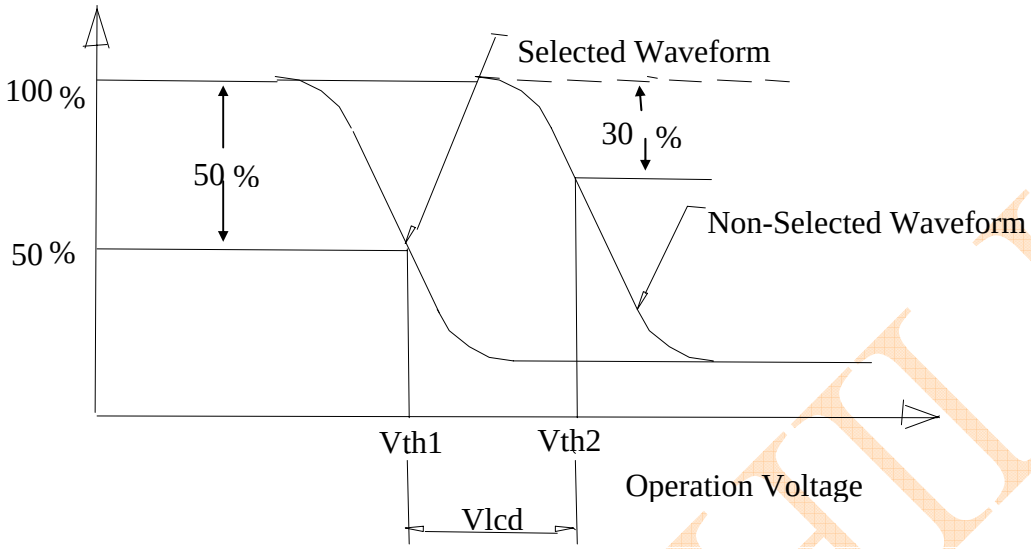
11.Electro-Optical Characteristics Measuring Equipment(DMS501).



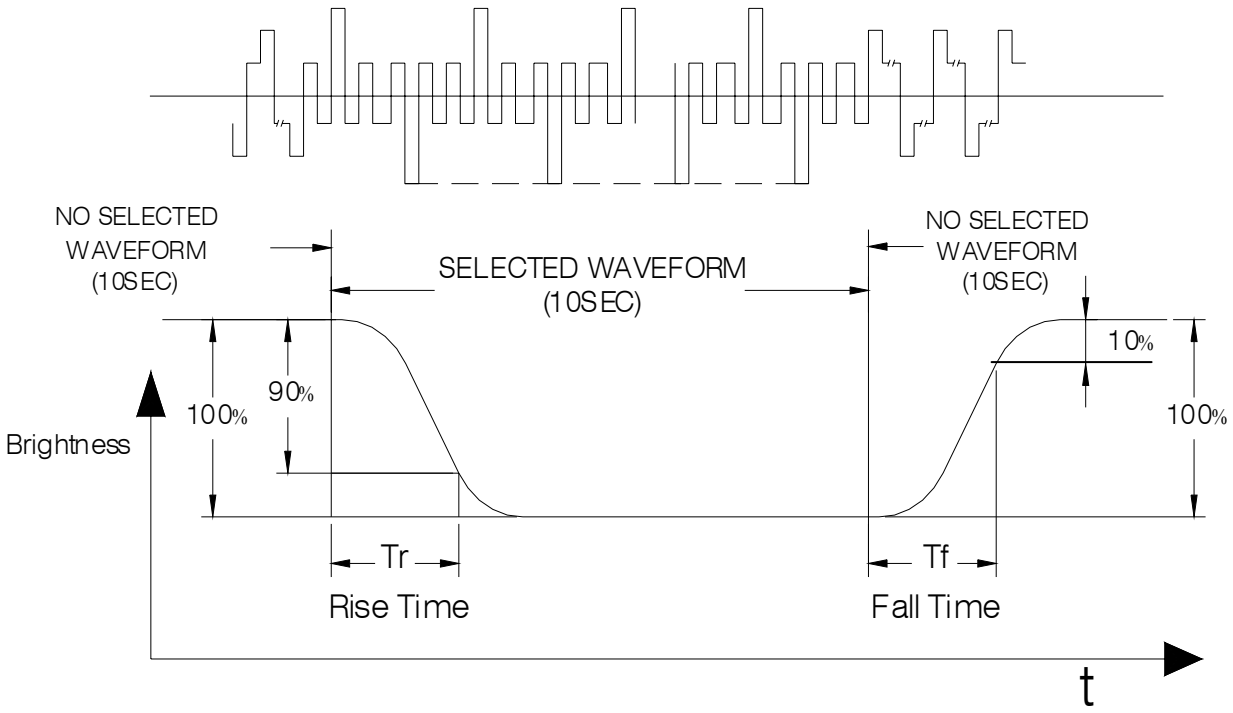
System

Illumination (D65)

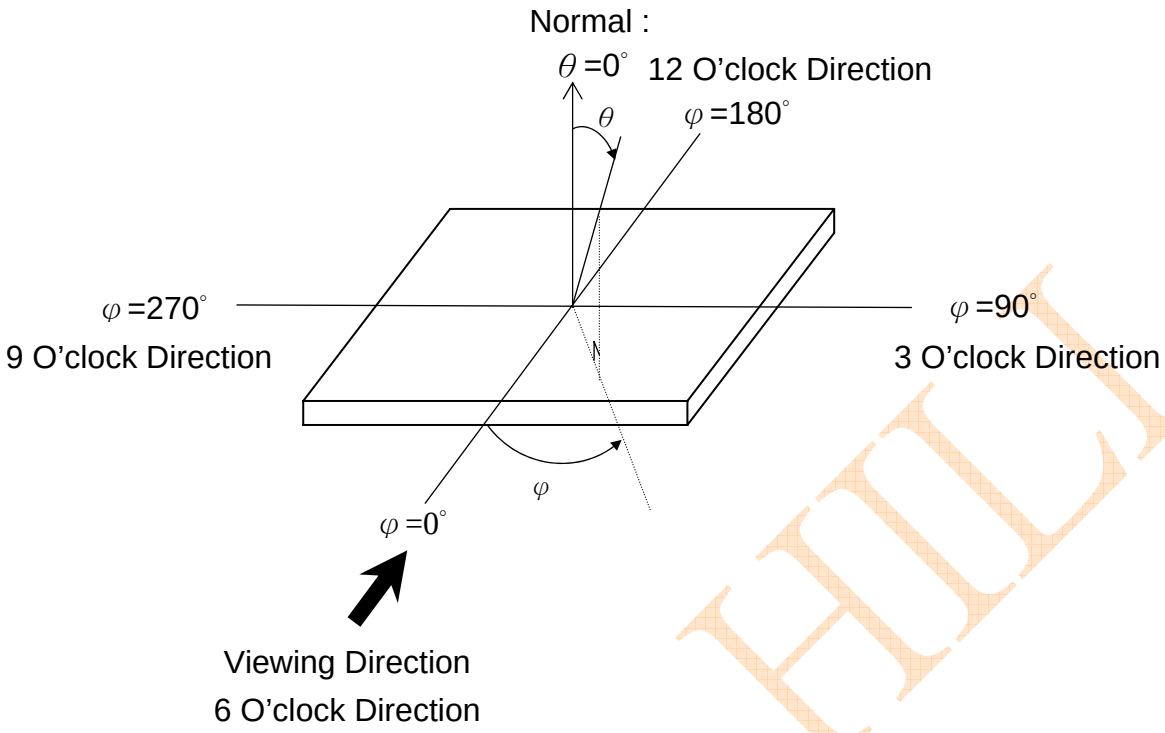
- **Note 1. Definition of Driving Voltage(Vlcd) :**



- **Note 2. Definition of Optical Response Time :**

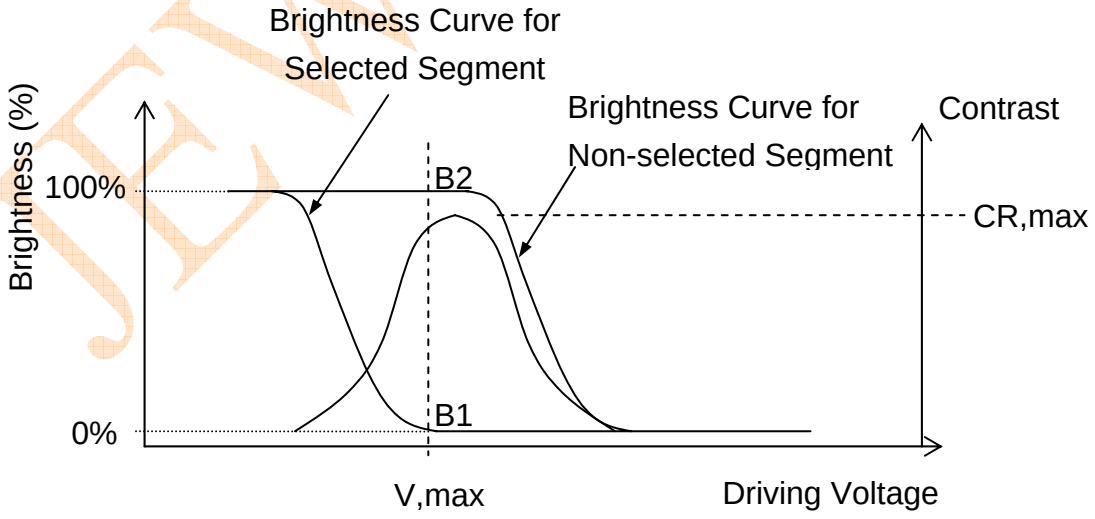


- **Note 3. Definition of Viewing Angle θ and ϕ :**



- **Note 4. Definition of Contrast ratio(CR) :**

$$CR = \frac{\text{Brightness of Non-selected Segment (B2)}}{\text{Brightness of Selected Segment (B1)}}$$



12. RELIABILIT.

12.1 MTBF.

The LCD module shall be designed to meet a minimum MTBF value of 30000 hours with normal. (25℃ in the room without sunlight)

12.1.1 TESTS.

NO.	ITEM	CONDITION	CRITERION
1	High Temperature Operating	50℃ 120Hrs	◦ No Defect Of Operational Function In Room Temperature Are Allowable. ◦ IDD of LCM in Pre-and post-test should follow specification
2	Low Temperature Operating	0℃ 120Hrs	
3	High Temperature/ Humidity Non-Operating	50℃ ,90%RH ,120 Hrs	
4	High Temperature Non-Operating	60℃ 120Hrs	
5	Low Temperature Non-Operating	-10℃ 120Hrs	
6	Temperature Cycling Non-Operating	0℃(30Min)↔ 50℃(30Min) 10 CYCLES	

Notes: Judgments should be mode after exposure in room temperature for two hours.

13. PRECAUTIONS FOR USING LCD MODULES.

13.1HANDLING PRECAUTIONS.

(1) The display panel is made of glass. Do not subject it to a mechanical shock or impact by dropping it.

(2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.

(3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

(5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten a cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

(6) Solvents other than those above mentioned may damage the polarizer.
Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

(7) Extra care to minimize corrosion of the electrode. Water droplets, moisture condensation or a current flow in a high-humidity environment accelerates corrosion of the electrode.

(8) Install the LCD Module by using the mounting holes. When mounting the LCD Module, make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.

(9) Do not attempt to disassemble or process the LCD Module.

(10) NC terminal should be open. Do not connect anything.

(11) If the logic circuit power is off, do not apply the input signals.

(12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling he LCD Module.
- Tools required for assembling, such as soldering irons, must be properly grounded.
-To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
-The LCD Module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

13.2 STORAGE CONDITIONS.

When storing, avoid the LCD module to be exposed to direct sunlight of fluorescent lamps. For stability, to keep it away form high temperature and high humidity environment (The best condition is : 23±5°C, 45±20%RH). ESD protection is necessary for long-term storage also.

13.3 OTHER.

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD Module have been operating for a long time showing the same display patterns the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be recovered by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD Module resulting from destruction caused by static electricity etc. exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- *Terminal electrode sections.*

14.Using LCD MODULE.

14.1 LIQUID CRYTAL DISPLAY MODULES.

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

(1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

(2) Do not touch, push or rub the exposed polarizers with anything harder than a HB pencil lead (glass, tweezers, etc).

(3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances, which will be damaged by chemicals such as acetone, toluene, toluene, ethanol and isopropyl alcohol.

(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum ether. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

(7) Condensation on the surface and contact with terminals due to cold will damage, stain or polarizers. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

(9) Do not touch the display with bare hands. This will stain the display area and degrade insulation between terminals (some cosmetics are determinate to the polarizers).

(10)As glass is fragile, it tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

14.2 INSTALLNG LCD MODULE.

Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.

(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ±0.1mm.

14.3 ELECTRO-STATIC DISCHARGE CONTROL.

Since this module uses a CMOS LSI, the same careful attention should be paid for electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handing LCM.

(2) Before removing LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.

(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.
(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.
(5) As far as possible, make the electric potential of your work clothes and that of the workbenches to the ground potential.
(6) To reduce the generation of electro-static discharge, be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended

14.4 PRECAUTIONS FOR OPERATION.

(1) Viewing angle varies with the change of liquid crystal driving voltage (Vo). Adjust Vo to show the best contrast.
(2) Driving the LCD in the voltage above the limit will shorten its lifetime.
(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.
(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then on.
(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, this product must be used and stored within the specified condition of 23±5°C, 45±20%RH.
(6) When turning the power on, input each signal after the positive/negative voltage becomes stable.

14.5 SAFETY.

(1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
(2) If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

15. REVISION HISTORY.

Version	Revise record	Date
00	Original version	12-06-12
0.01	Perfect the VER00 spec，Commany internal modify.	13-08-01

SAMPLE APPROVED REPORT

(样品确认单)

SAMPLE MODEL NO. (样品型号)	JHB7021A
SAMPLE SERIES NUMBER NO. (样品序号)	
SAMPLE QUANTITY (样品数量)	
COLOR/TYPE (底色/类型)	VA/EBT
VIEWING DIRECTION (视角)	6:00
DRIVING METHOD (驱动参数)	1/4Duty, 1/3Bias
LOGIC VOLTAGE (工作电压)	5.0V
LCD VOP (LCD 驱动电压)	4.5V
OPERATING TEMP. (操作温度)	0 ~ +50℃
STORAGE TEMP. (储存温度)	-10 ~ +60℃
POLARIZER----FRONT (首偏光片)	Transmissive
POLARIZER----BACK (后偏光片)	Transmissive
CONTROLLER/DRIVER IC(控制/驱动 IC)	PCF8576CT
BACKLIGHT COLOR/TYPE (背光源类型/颜色)	LED/WHITE
DRAWING REV/NO./QUANTITY (图纸版本/数量)	
SPECIFICATION (规格书　份数)	

REMARKS:
(备注)
WRIT BY: _____ DATE: _____ APROV BY: _____ DATE: _____

CUSTOMER'S APPROVAL (客户确认):

1） FUNCTION （功能）: ☐ OK ☐ N.G.
2） DRIVER CONDITION （驱动条件）: ☐ OK ☐ N.G.
3） DISPLAY MODE （显示模式）: ☐ OK ☐ N.G.
4） VIEWING ANGLE （视角）: ☐ OK ☐ N.G.
5） BACKLIGHT （背光源）: ☐ OK ☐ N.G.
6） DISPLAYING PATTERN （显示效果）: ☐ OK ☐ N.G.

CUSTOMER'S CONCLUSIONS (客户意见): _____
_____
_____

CUSTOMER'S SIGNATURE（客户签名）: _____ DATE (日期): _____