

**N-CHANNEL ENHANCEMENT MODE MOSFET**

**Product Summary**

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	$I_D$ max $T_A = +25^\circ C$
30V	28mΩ @ $V_{GS} = 10V$	5.8A
	42mΩ @ $V_{GS} = 4.5V$	4.8A
	82mΩ @ $V_{GS} = 3V$	2.0A

**Description**

This MOSFET has been designed to minimize the on-state resistance ( $R_{DS(ON)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

**Applications**

- Battery Charging
- Power Management Functions
- DC-DC Converters
- Portable Power Adaptors

**Features and Benefits**

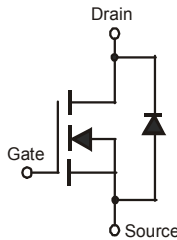
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

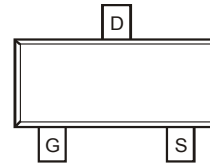
- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208  $\text{e3}$
- Terminals Connections: See Diagram Below
- Weight: 0.008 grams (approximate)



Top View



Internal Schematic



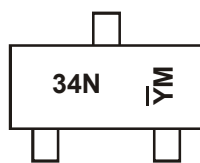
Top View

**Ordering Information** (Note 4 & 5)

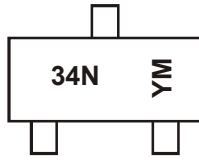
Part Number	Compliance	Case	Packaging
DMN3404L-7	Standard	SOT23	3000/Tape & Reel
DMN3404LQ-7	Automotive	SOT23	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. Automotive products are AEC-Q101 qualified and are PPAP capable. Automotive and standard products are electrically and thermally the same, except where specified. For more information, please refer to [http://www.diodes.com/quality/product\\_compliance\\_definitions/](http://www.diodes.com/quality/product_compliance_definitions/).
  5. For packaging details, go to Diodes website at <http://www.diodes.com/products/packages.html>.

**Marking Information**



Chengdu A/T Site



Shanghai A/T Site

34N = Product Type Marking Code  
 YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)  
 $\bar{Y}\bar{M}$  = Date Code Marking for CAT (Chengdu Assembly/ Test site)  
 Y or  $\bar{Y}$  = Year (ex: A = 2013)  
 M = Month (ex: 9 = September)

Date Code Key

Year	2009	2010	2011	2012	2013	2014	2015
Code	W	X	Y	Z	A	B	C

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic		Symbol	Value	Units	
Drain-Source Voltage (Note 6 & 7)		$V_{DS}$	30	V	
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$I_D$	$T_A = -40^\circ\text{C}$	4.6	A
			$T_A = +25^\circ\text{C}$	4.2	
			$T_A = +85^\circ\text{C}$	3.0	
Continuous Drain Current (Note 7) $V_{GS} = 10\text{V}$	Steady State	$I_D$	$T_A = -40^\circ\text{C}$	6.2	A
			$T_A = +25^\circ\text{C}$	5.8	
			$T_A = +85^\circ\text{C}$	4.0	
Continuous Drain Current (Note 7) $V_{GS} = 4.5\text{V}$	Steady State	$I_D$	$T_A = -40^\circ\text{C}$	5.2	A
			$T_A = +25^\circ\text{C}$	4.8	
			$T_A = +85^\circ\text{C}$	3.2	
Continuous Drain Current (Note 7) $V_{GS} = 3\text{V}$	Steady State	$I_D$	$T_A = -40^\circ\text{C}$	2.2	A
			$T_A = +25^\circ\text{C}$	2.0	
			$T_A = +85^\circ\text{C}$	1.0	
Pulsed Drain Current		$I_{DM}$	30	A	

**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 6)	$P_D$	0.72	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$	$R_{\theta JA}$	173	$^\circ\text{C}/\text{W}$
Power Dissipation (Note 7)	$P_D$	1.4	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$	$R_{\theta JA}$	90	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

Notes: 6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.  
7. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	—	—	1.0	μA	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	1.0	1.5	2.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance T <sub>J</sub> = -40°C (Note 9)	R <sub>DS(on)</sub>	—	23	27	—	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 4.8A
		—	57	74	—	V <sub>GS</sub> =3V, I <sub>D</sub> =2A
Static Drain-Source On-Resistance T <sub>J</sub> = +25°C	R <sub>DS(on)</sub>	—	24	28	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 5.8A
		—	33	42		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 4.8A
		—	63	82	V <sub>GS</sub> =3V, I <sub>D</sub> =2A	
		—	71	95	mΩ	V <sub>GS</sub> =3V, I <sub>D</sub> =2A
Static Drain-Source On-Resistance T <sub>J</sub> = +85°C (Note 9)	R <sub>DS(on)</sub>	—	71	95	mΩ	V <sub>GS</sub> =3V, I <sub>D</sub> =2A
Forward Transfer Admittance	Y <sub>fs</sub>	—	10	—	S	V <sub>DS</sub> = 5V, I <sub>D</sub> = 5.8A
Diode Forward Voltage	V <sub>SD</sub>	—	0.75	1.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A
<b>DYNAMIC CHARACTERISTICS (Note 10)</b>						
Input Capacitance	C <sub>iss</sub>	—	498	—	pF	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	52	—	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	45	—	pF	
Gate Resistance	R <sub>g</sub>	—	1.75	2.8	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = 3V)	Q <sub>g</sub>	—	3.8	5.3	nC	V <sub>GS</sub> = 3V, V <sub>DS</sub> = 15V, I <sub>D</sub> = 1A
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	—	5.3	7.5	nC	V <sub>GS</sub> = 10V/4.5V, V <sub>DS</sub> = 15V, I <sub>D</sub> = 5.8A
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	—	11.3	16	nC	
Gate-Source Charge	Q <sub>gs</sub>	—	1.4	—	nC	
Gate-Drain Charge	Q <sub>gd</sub>	—	2.1	—	nC	
Turn-On Delay Time	t <sub>D(on)</sub>	—	3.41	10	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 10V, R <sub>L</sub> = 2.6Ω, R <sub>G</sub> = 3Ω
Turn-On Rise Time	t <sub>r</sub>	—	6.18	13	ns	
Turn-Off Delay Time	t <sub>D(off)</sub>	—	13.92	28	ns	
Turn-Off Fall Time	t <sub>f</sub>	—	2.84	10	ns	

Notes: 8. Short duration pulse test used to minimize self-heating effect.  
 9. Guaranteed by design and 25°C data. Not subject to production testing  
 10. Guaranteed by design. Not subject to production testing.

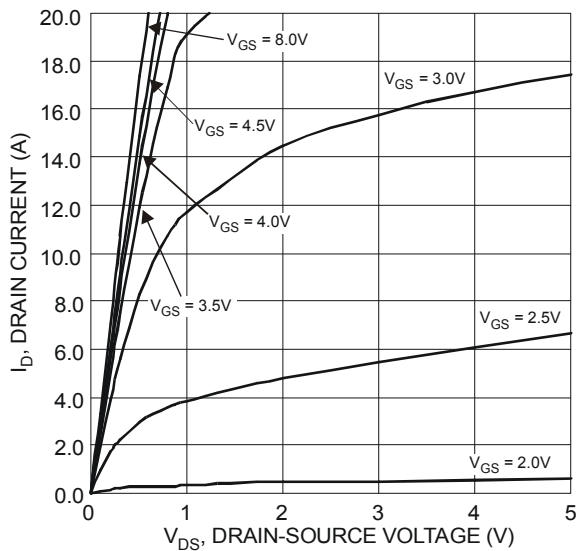


Figure 1 Typical Output Characteristics

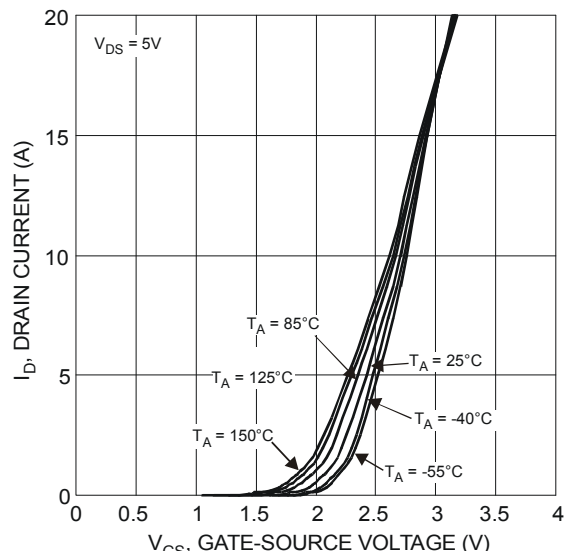


Figure 2 Typical Transfer Characteristics

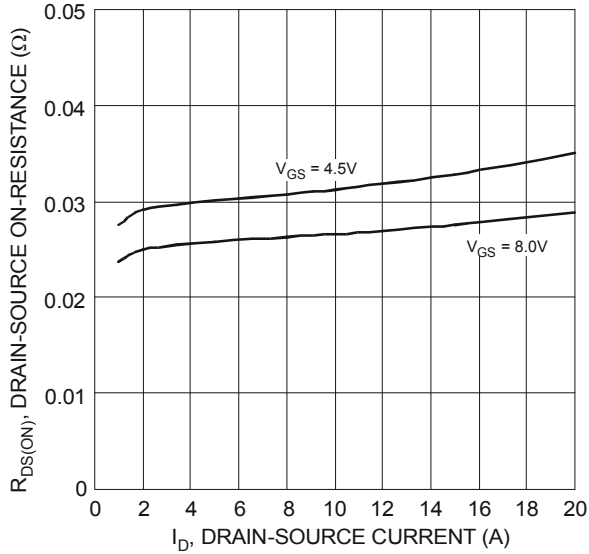


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

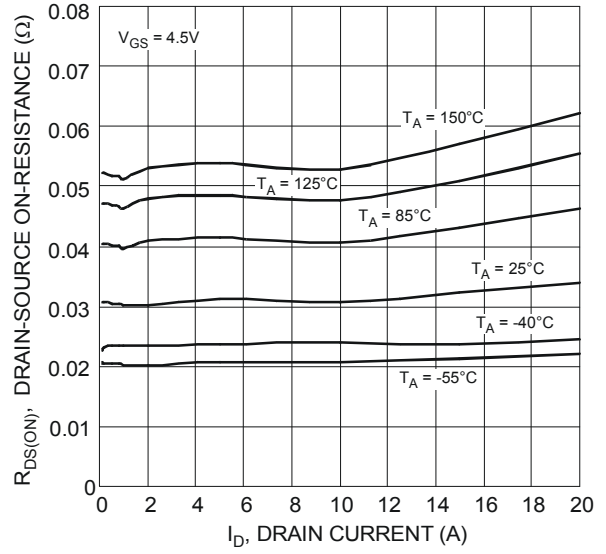


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

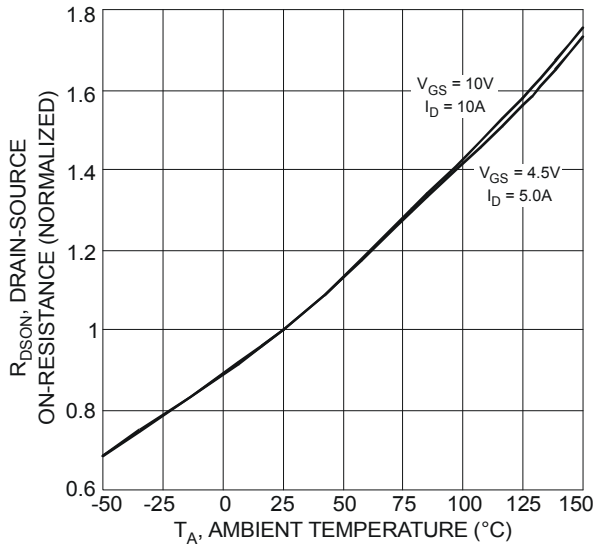


Figure 5 On-Resistance Variation with Temperature

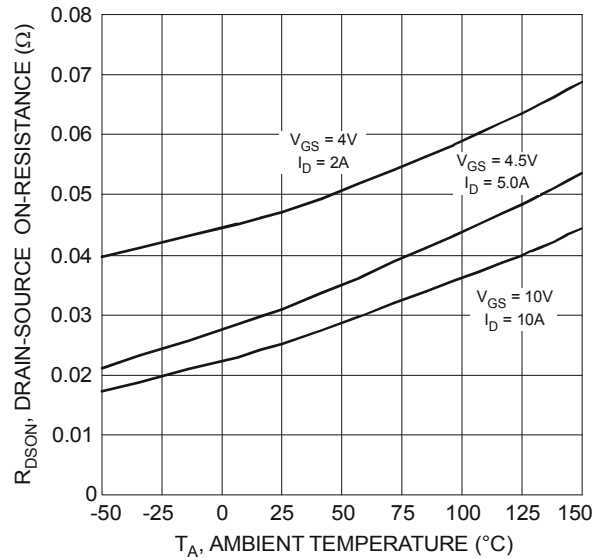


Figure 6 On-Resistance Variation with Temperature

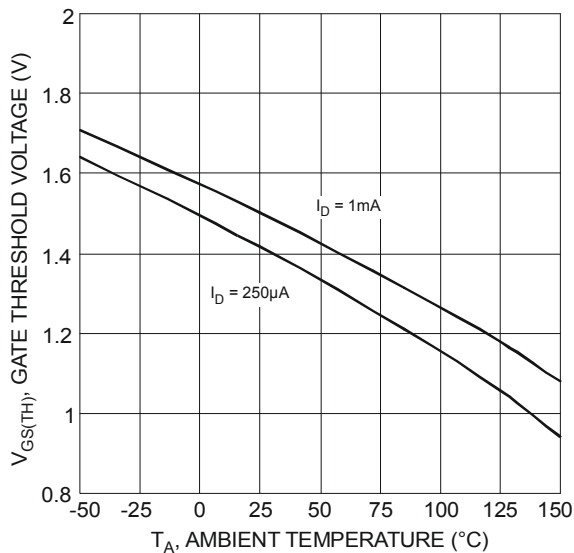


Figure 7 Gate Threshold Variation vs. Ambient Temperature

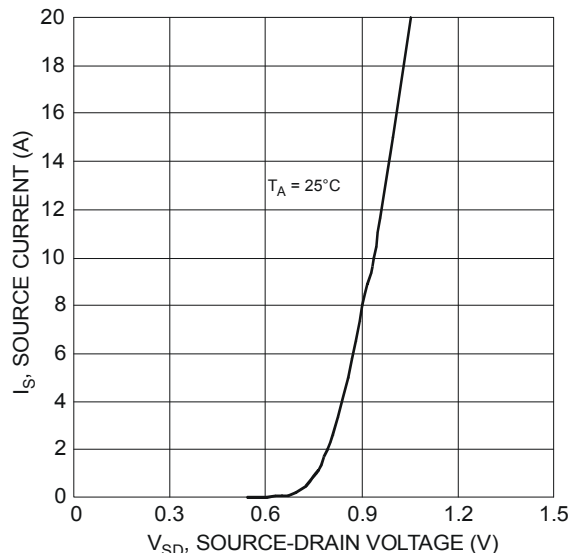


Figure 8 Diode Forward Voltage vs. Current

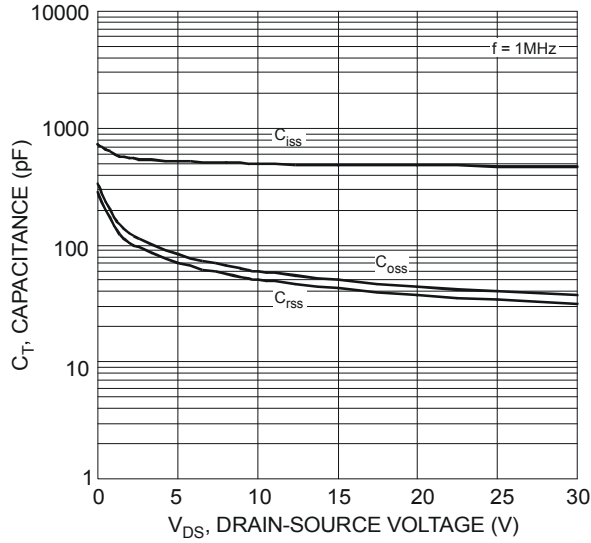


Figure 9 Typical Total Capacitance

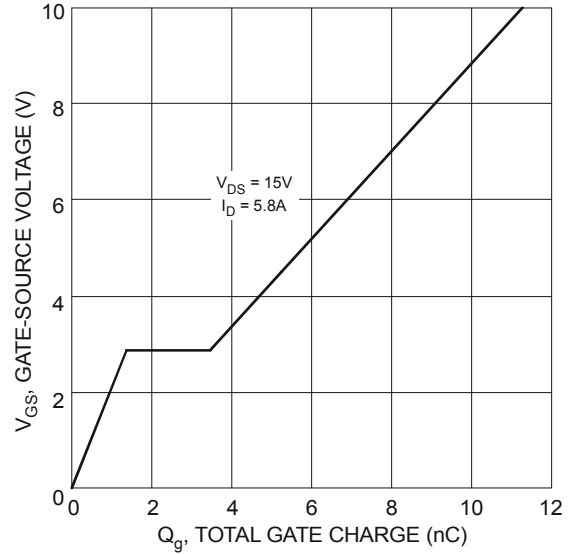


Figure 10 Gate-Charge Characteristics

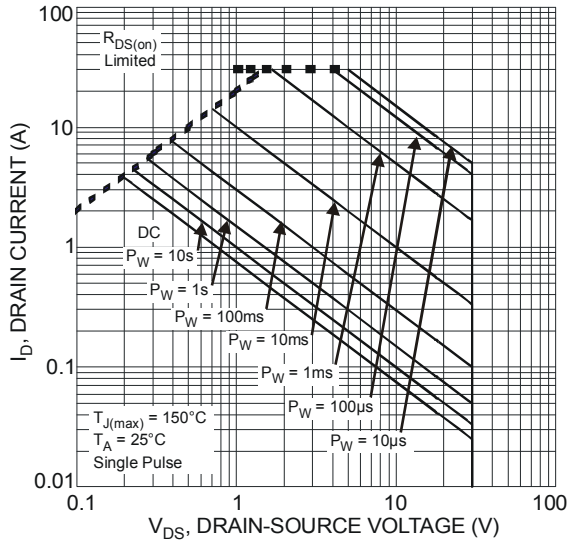


Figure 11 Safe Operation Area

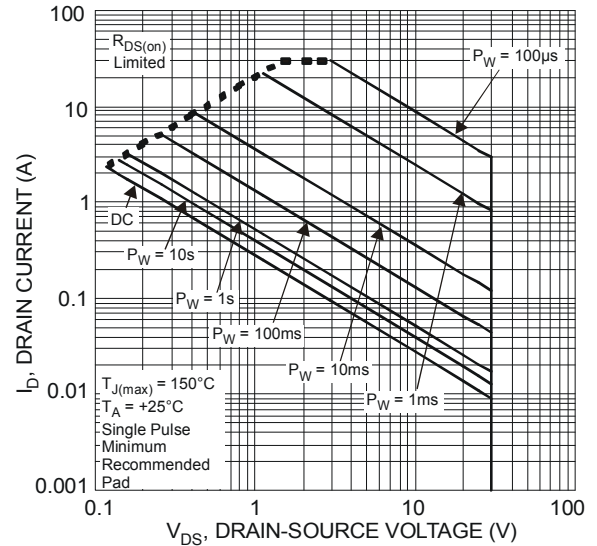


Figure 12 Safe Operation Area

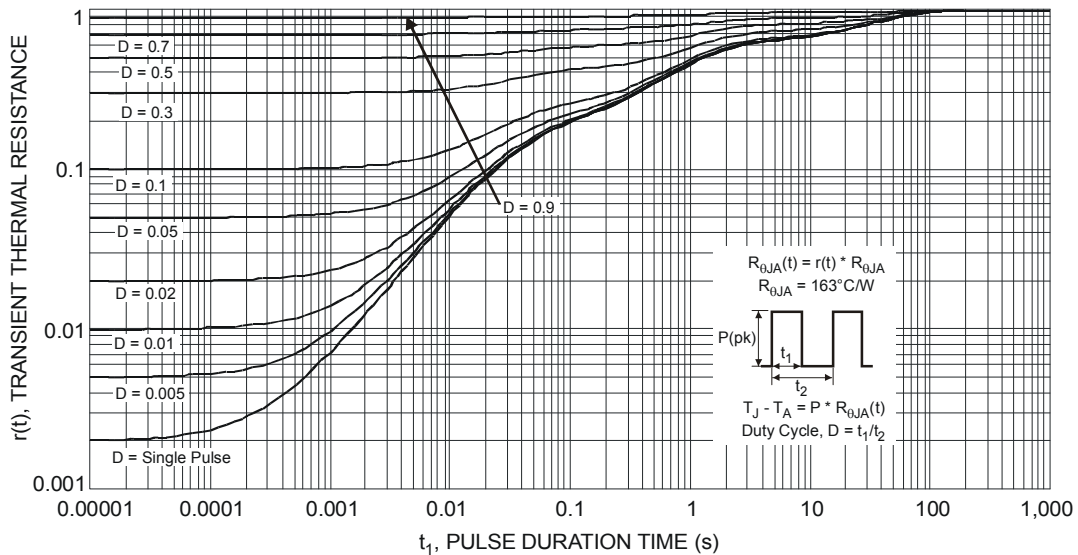
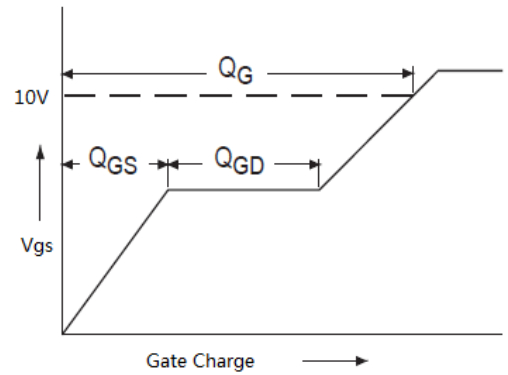
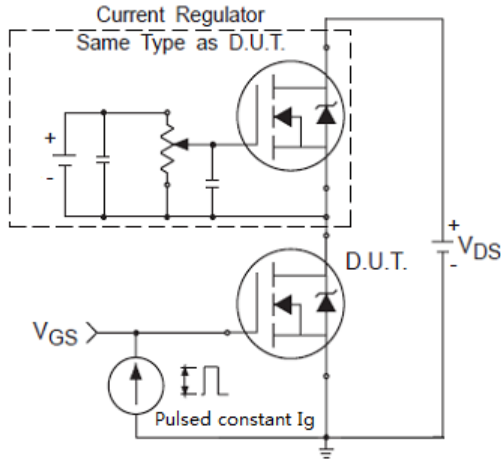
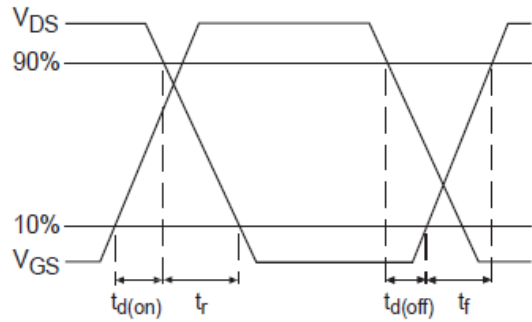
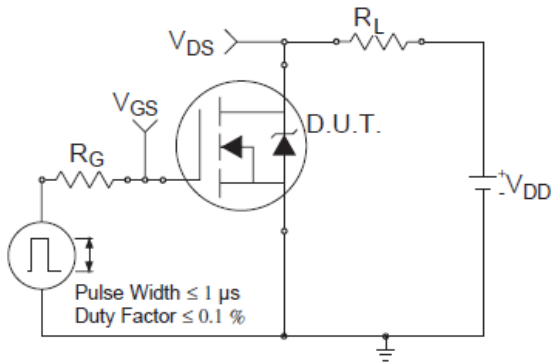


Figure 13 Transient Thermal Response

**Gate Charge Test Circuit and Waveform**

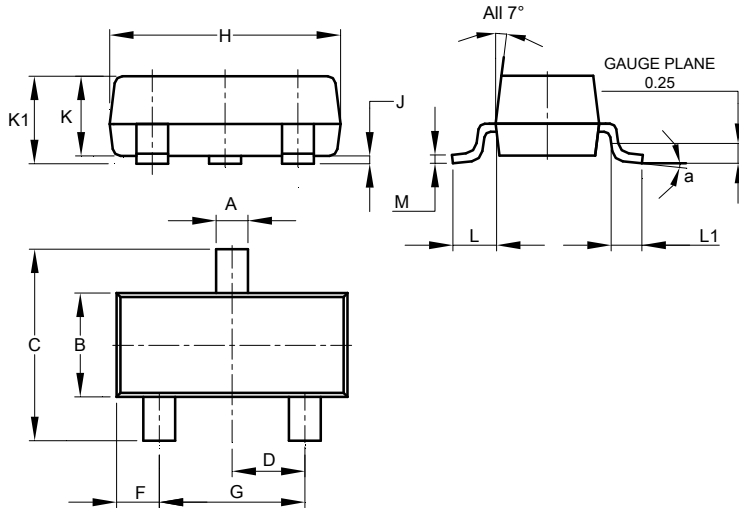


**Switching Test Circuit and Waveform**



**Package Outline Dimensions**

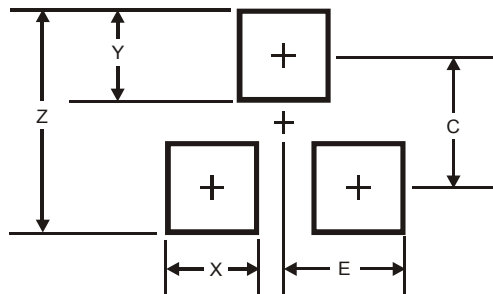
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
α	8°		
All Dimensions in mm			

**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for latest version.



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35

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