DESIGN GUIDE FOR ISOLATED DC/DC USING THE SI884XX/886XX

1. Introduction

The Si884xx/Si886xx product families integrate digital isolator channels with an isolated dc-dc controller. This application note provides guidance for selecting external components necessary for the operation of the dc-dc controller.

Digital isolation applications with primary side supply voltage V_{IN} > 5.5 V or load power requirements of >2 W can use Si884xx/Si886xx products. These product's dc-dc controller uses the isolated flyback circuit topology. The advantage of this topology when compared with the Si882xx/Si883xx is that it can be tailored to work in higher voltage and higher power applications.

Figure 1 shows the minimum external components required for the isolated flyback, including optional support circuitry. The components shown in Figure 1 are input capacitor C2, transformer T1, power switching FET Q1, current sense resistor R12, primary snubber R16 and C19, secondary diode D1, output capacitor C10, secondary snubber R8 and C8, voltage sense resistors R5 and R6, and compensation network components R7 and C11. Q2, R14, and C14 create a regulator circuit to power VDDA from V_{IN}. C6 and R13 set the switching frequency and soft start characteristics for product variants that use external frequency and soft start control.

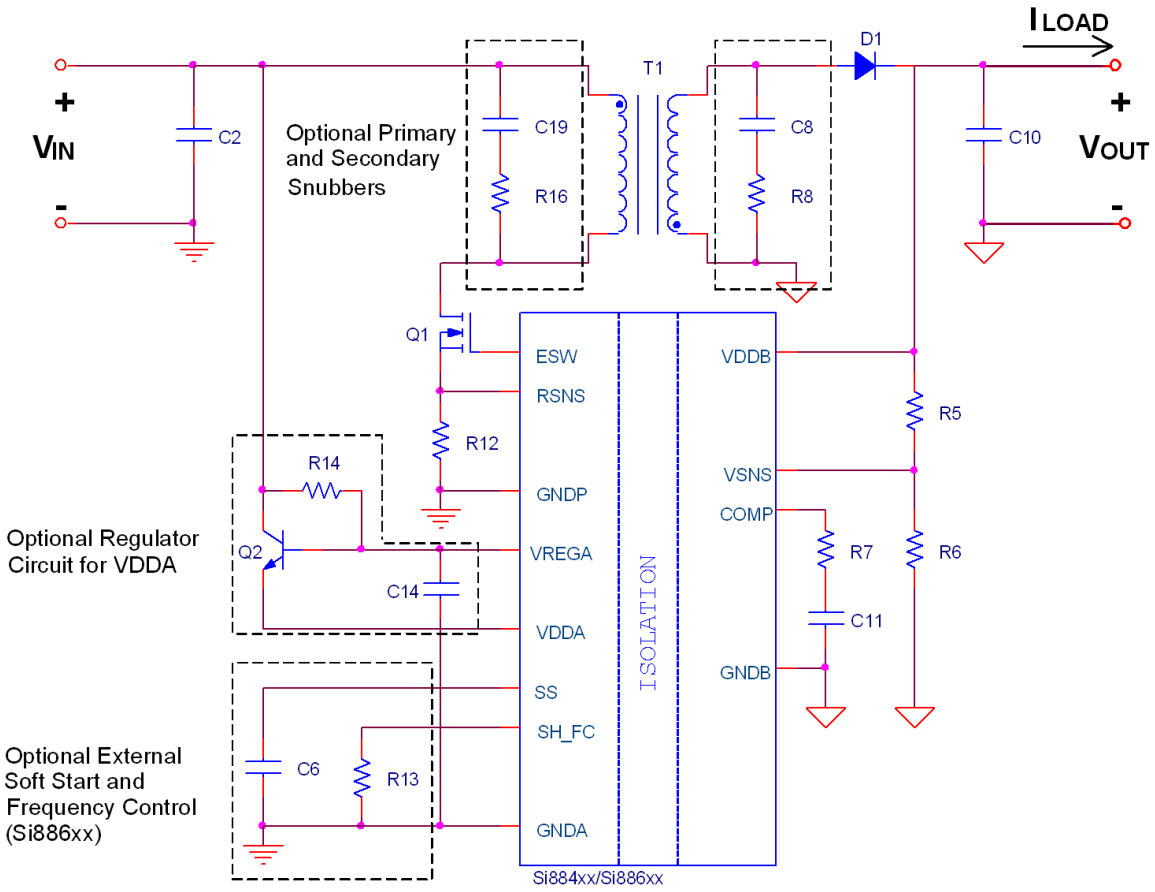

Figure 1. Required External Components

2. Simplified DC Steady State Analysis

Analyzing the flyback behavior in DC steady state provides formulas to assist with selecting values for the components used in Figure 1. For this analysis, it is assumed that components are ideal, at 100% efficiency ($P_{IN} = P_{OUT}$), and the circuit has reached equilibrium.

Figure 2 shows the critical components of the flyback converter. The transformer model includes magnetizing inductance L_m and inductance leakage L_{lkg}. R_{LOAD} does not necessarily represent a physical resistor, rather it is an expression of V_{OUT}/I_{OUT}.

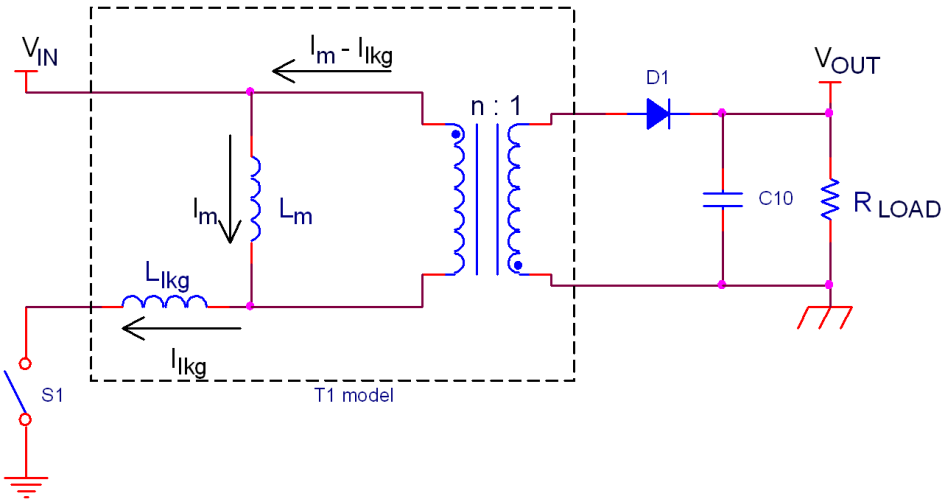

Figure 2. Flyback Converter

For DC steady state analysis, the two modes where the system operates the majority of the cycle are only required when S1 is closed and when S1 is open. Figure 3 depicts the simplified magnetizing and secondary current waveforms.

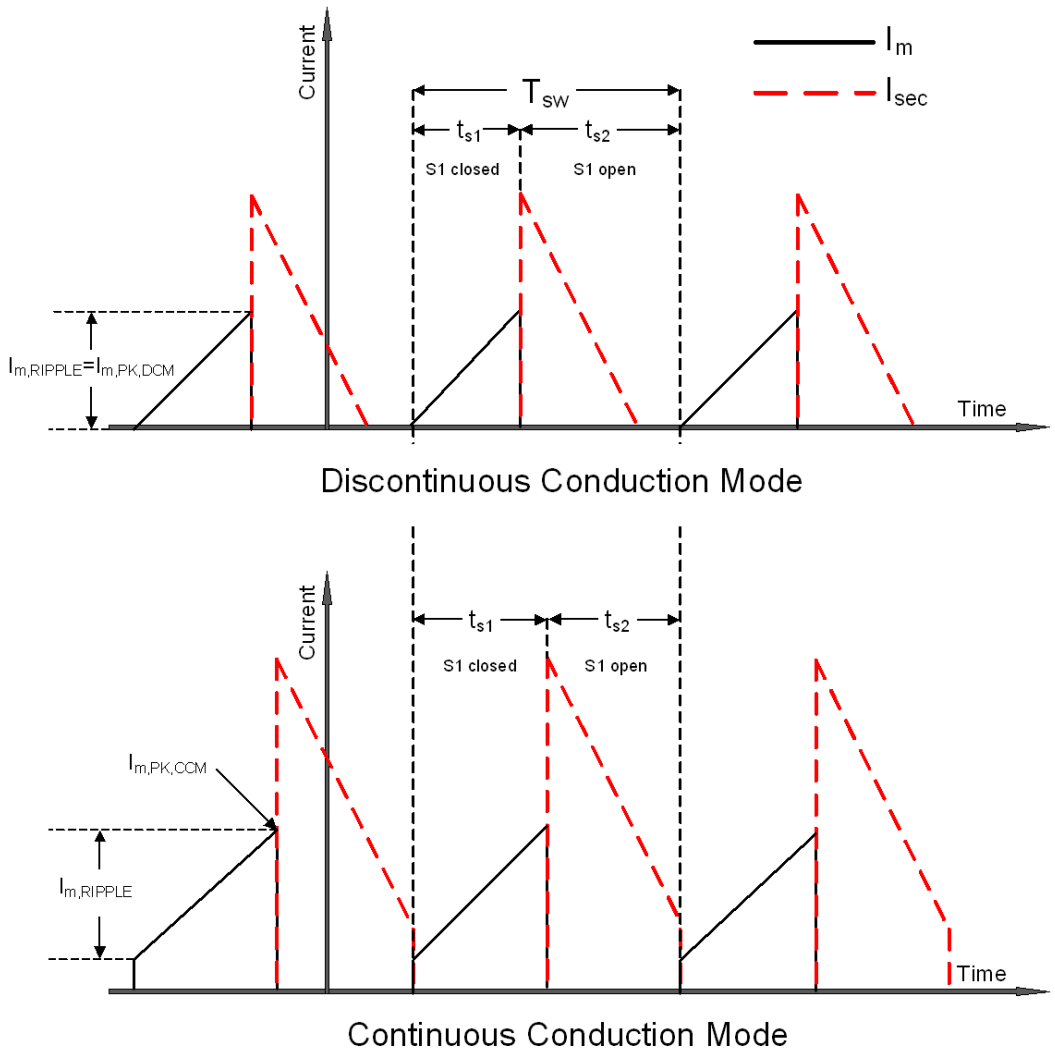

Figure 3. Inductor Currents

2.1. S1 Closed

V_{IN} is applied to the primary inductance L_m. As a result, current flows through inductance L_m and energy is stored in the magnetic field of the transformer T1:

$$V_{IN} = (L_m)\frac{I_{m,RIPPLE}}{t_{S1}}$$

Equation 1.

$I_{m,RIPPLE}$ is the magnetizing current ramp during t_{S1}, and t_{S1} is the time that S1 is closed. In Discontinuous Conduction Mode (DCM), $I_{m,RIPPLE}$ is equal to $I_{m,PK}$ as primary and secondary currents returning to zero before the next cycle. In Continuous Conduction Mode (CCM), the currents do not reach zero before the next switching cycle.

2.2. S1 Open

The instant S1 opens, current can no longer flow through the primary and the magnetic field collapses, transferring energy to the secondary, causing current to flow out of the dot of the ideal transformer. The energy stored in the leakage inductance is not transferred and it must be dissipated in the primary through the snubber network. The voltage at the secondary will be impressed on the primary. The governing current equation is:

$$I_{m,RIPPLE} = -\frac{n \times V_{OUT} \times t_{S2}}{L_m}$$

Equation 2.

where n and t_{S2} are primary to secondary turns ratio and time that S1 is open, respectively.

2.3. Voltage Transfer

Let duty cycle D be defined as the ratio of time S1 is closed over the complete switching period T_{sw}:

$$D = \frac{t_{S1}}{t_{S1} + t_{S2}}$$

Equation 3.

Now t_{S1} and t_{S2} can be expressed in terms of D and switching period as:

$$t_{S1} = DT_{sw}$$

Equation 4.

$$t_{S2} = (1 - D)T_{sw}$$

Equation 5.

and assume diode D1 has no voltage drop when conducting the volt-second balance equation for L_m, which in CCM operation can be written as:

$$V_{IN}DT_{sw} - (nV_{OUT})(1 - D)T_{sw} = 0$$

Equation 6.

Equation 6 simplifies to:

$$V_{OUT} \cong \frac{V_{IN}D}{n(1 - D)}$$

Equation 7.

For DCM, current does not flow out of the secondary over the entire (1-D) portion, which changes the voltage transfer function shown in Equation 7. Unlike CCM, the voltage transfer characteristics in DCM are dependent on factors such as R_{LOAD} and switching period. The governing equation is:

$$V_{OUT} \cong V_{IN}D\sqrt{\frac{R_{LOAD}T_{sw}}{2L_m}}$$

Equation 8.

2.4. Magnetizing Current

Substituting Equation 4 into Equation 1, the ripple magnetizing current is:

$$I_{m,RIPPLE} = \frac{V_{IN} t_{S1}}{L_m} = \frac{V_{IN} DT_{sw}}{L_m}$$

Equation 9.

The average magnetizing current is related to the output current as:

$$I_{m,AVE} = \frac{I_{LOAD}}{n(1-D)}$$

Equation 10.

When a flyback converter is operating in CCM, the peak magnetizing current is given by the average current plus one half of the ripple current:

$$I_{m,PK,CCM} = I_{m,AVE} + \frac{V_{IN} DT_{sw}}{2L_m}$$

Equation 11.

When a flyback converter is operating in DCM, the peak magnetizing current is equal to the ripple current:

$$I_{m,PK,DCM} = I_{m,RIPPLE}$$

Equation 12.

Si884xx/Si886xx controller limits the peak magnetizing current by comparing the voltage across the current sense resistor R12 to an internal reference voltage of approximately 100 mV. If more than 100 mV is developed across R12 during S1 closed, the controller immediately switches S1 open. The controller maintains the same switching period, but reduces the duty cycle D to limit peak current. The cycle by cycle current limit is given by:

$$I_{m,LIMIT} = \frac{100\,mV}{R12}$$

Equation 13.

2.5. Optional Primary Snubber

Snubbers are used for two purposes in a flyback converter: to limit the peak voltage on the drain of the Q1, and to attenuate high frequency ringing that leads to emissions. There are several methods to create a primary side flyback snubber. The RC snubber is presented here. The energy stored in the leakage inductance L_{lkg} does not transfer to the secondary and must be dissipated in the primary. The power dissipated in the leakage inductance is given by:

$$P_{lkg} = \frac{L_{lkg} I_{m,PK}^2}{2T_{sw}}$$

Equation 14.

When S1 opens, the current flowing in the primary will charge the drain-source capacitance of Q1 causing the voltage at the drain to increase rapidly. When this voltage exceeds $V_{IN} + nV_{OUT}$, a ringing occurs with frequency dependent on the inductance leakage L_{lkg} and C_{ds}. The RC snubber presents a load for which to dissipate the power stored in the inductance leakage. This load limits the switching speed of Q1, which limits the peak voltage across the drain-source. A first order approximation for determining R16 and C19 is to set them to the characteristic impedance of the ringing caused by L_{lkg} of T1 and C_{ds} of Q1.

$$R16 \cong Z_{C19} \cong \sqrt{\frac{L_{lkg}}{C_{ds}}}$$

Equation 15.

R16 can be determined by measuring L_{lkg} and ringing frequency:

$$R16 \cong 2\pi f_{ring} L_{lkg}$$

Equation 16.

C19 can be set to the same impedance using:

$$C19 \cong \frac{1}{2\pi f_{ring} R16}$$

Equation 17.

2.6. Input Capacitor

The purpose of C2 input capacitor is to provide filtering for V_{IN} during the switching cycle and reduce voltage ripple at the converter input. Operating in CCM, during t_{S1} portion of the cycle C2 current is given by:

$$I_{C2} = I_{IN} - I_{m,AVE} = (D-1)\frac{I_{LOAD}}{n(1-D)} = -\frac{I_{LOAD}}{n}$$

Equation 18.

The voltage ripple on C2 can be written as:

$$V_{IN,RIPPLE} = \left|\frac{I_{C2} D T_{sw}}{C2}\right| = \frac{I_{LOAD} D T_{sw}}{n \times C2}$$

Equation 19.

2.7. Optional Regulator for VDDA Supply

VDDA valid operating range is between 3.0 V and 5.5 V. In applications where the only source available on the primary side is above 5.5 V, Si884xx/Si886xx provides a voltage reference for an external regulator circuit.

The regulator circuit consists of transistor Q2, R14, and C14, as shown in Figure 4. The circuit behind the VREGA pin can be modeled as a zener diode connected from VREGA to GNDA, and requires input current between 350 µA to 950 µA to establish a nominal 4.85 V reference at the VREGA pin. This reference is tied to the base of Q2 and the emitter outputs approximately a 4.3 V supply suitable to power VDDA.

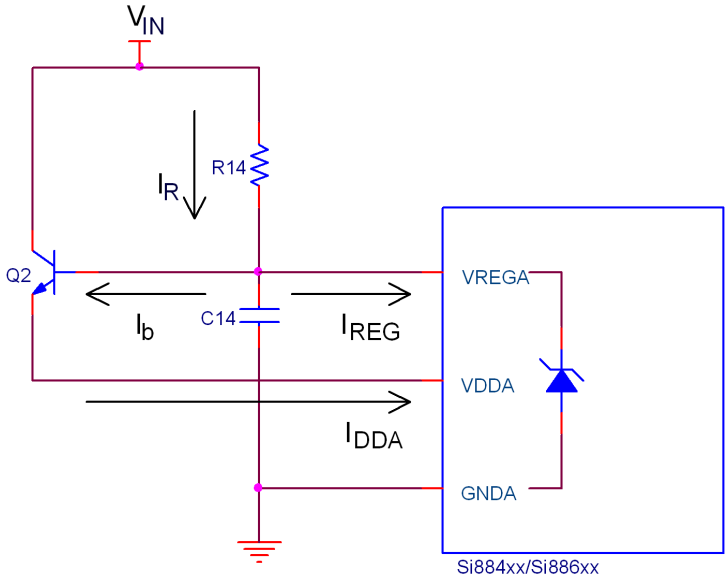

Figure 4. External Regulator Circuit

The governing equations for the circuit are:

$$I_R = I_b + I_{REG} = \frac{V_{IN} - V_{REGA}}{R14}$$

Equation 20.

$$I_{DDA} = I_b(\beta + 1)$$

Equation 21.

$$V_{DDA} = V_{REGA} - V_{be}$$

Equation 22.

It is recommended to set I_R to no more than 950 µA no matter I_{DDA} load. As I_{DDA} increases, more of I_R will flow into the base of Q2. V_{REGA} reference voltage will be maintained as long as the I_{REG} > 350 µA. Choose Q2 with adequate gain β to source the maximum expected I_{DDA}. The recommended value for C14 filter capacitor for the VREGA reference is 100 nF.

2.8. Diode and Output Capacitor

In CCM, current flows through D1 only during the (1-D)T_{sw} portion of the steady state cycle. During the DT_{sw} portion of the cycle, I_{LOAD} is sourced solely by the output capacitor C10. Output voltage ripple on C10 can be calculated by:

$$V_{OUT,\,RIPPLE} = \frac{I_{LOAD} DT_{sw}}{C10}$$

Equation 23.

Applying the charge balance of C10,

$$-I_{LOAD} DT_{sw} + I_{D1,\,AVE(1-D)}(1-D)T_{sw} - I_{LOAD}(1-D)T_{sw} = 0$$

Equation 24.

$$I_{D1,\,AVE(1-D)} = \frac{I_{LOAD}}{1-D}$$

Equation 25.

When D1 is reversed biased, it must withstand:

$$V_{D1,\,REV(D)} = \frac{V_{IN}}{n} + V_{OUT}$$

Equation 26.

2.9. Optional Secondary Snubber

At the instant S1 closes, this reverse voltage applied to D1 can overshoot and ring before settling to $V_{D1,REV(D)}$ as given by Equation 26. A RC snubber can be used to limit the voltage stress across D1. Like the design of the optional primary snubber, a first order approximation for determining R8 and C8 is to set them to the characteristic impedance of the ringing caused by secondary side L_{lkg} of T1 and parasitic capacitance of D1.

$$R8 \cong Z_{C8} \cong \sqrt{\frac{L_{lkg,\,sec}}{C_{D1}}}$$

Equation 27.

R8 can be determined by measuring L_{lkg} and ringing frequency:

$$R8 \cong 2\pi f_{ring} L_{lkg,\,sec}$$

Equation 28.

C8 can be set to the same impedance using:

$$C8 \cong \frac{1}{2\pi f_{ring} R8}$$

Equation 29.

2.10. VSNS Voltage Divider

For the purpose of selecting sense resistors R5 and R6, the entire dc-dc converter can be modeled as a non-inverting amplifier as shown in Figure 5. Notice that the non-inverting input, supply voltage (V+), and output voltage of the amplifier correspond to the internal 1.05 V reference, V_{IN}, and V_{OUT} of the dc-dc converter.

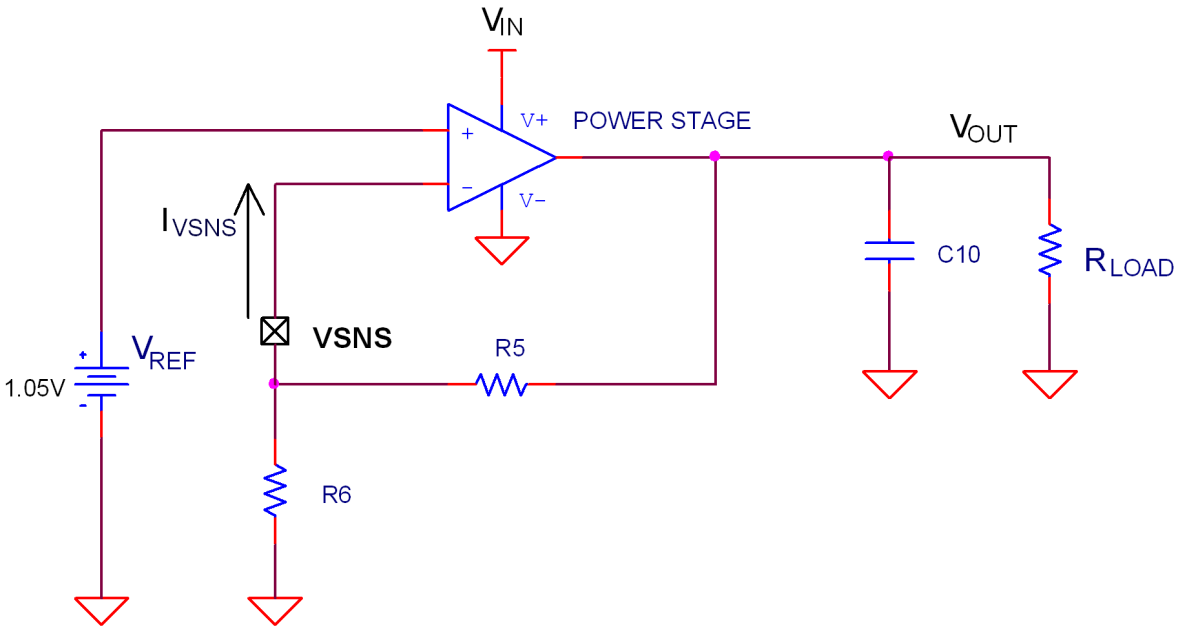

Figure 5. Simplified V_{OUT} Gain Model

Assuming infinite DC gain and applying KCL at the inverting input of the amplifier, V_{OUT} can be expressed by:

$$V_{OUT} = 1.05\left(\frac{R5}{R6} + 1\right) + R5 \times I_{VSNS}$$

Equation 30.

where I_{VSNS} represents the input offset current at VSNS pin. From Equation 30, it can be observed that a very large R5 could reduce the output voltage accuracy.

3. Dynamic Response

The Si886xx start-up response consists of four regions of operation: Calibration, Soft-Start (SS), Proportional-Mode (P-Mode), and Proportional Integral Mode (PI-mode). The Si884xx has fixed switching frequency and soft-start behavior hence its dc-dc operation skips Calibration and begins with Soft-Start. Figure 6 shows a typical V_{OUT} response during start up for the Si886xx operating at 500 kHz:

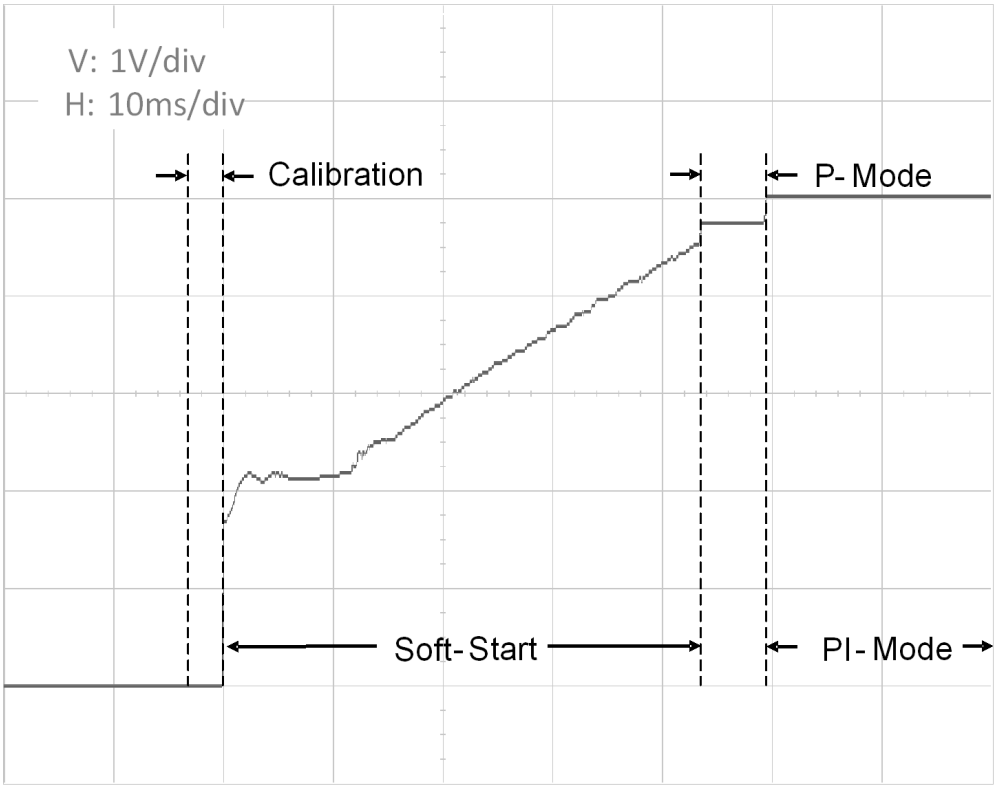

Figure 6. V_{OUT} During Start Up

3.1. External Soft-Start and Switching Frequency Calibration

The Si886xx has two additional external pins compared to Si884xx for setting switching frequency and adjusting soft start time, SH_FC and SS. The capacitor C6 is connected between pin SS and GNDA and sets the soft start time. The resistor R13 is connected between pin SH_FC and GNDA when the dc-dc is operating. Si886xx supports switching frequencies from 200 kHz to 900 kHz, and is set by:

$$T_{sw} \cong \frac{R13 \times C6}{1025.5}$$

Equation 31.

A practical C6 value for soft start is:

$$C6 = 470nF$$

Equation 32.

With C6 = 470 nF, R13 range to set acceptable T_{sw} is 2.42 kΩ to 10.9 kΩ. For any given T_{sw}, soft start time may be increased or decreased by increasing or decreasing C6 while adjusting R13 to maintain the same R13 x C6 time constant.

The time spent in calibration mode is approximately the time constant created by R13 and C6.

3.2. Soft Start

In soft start mode, the dc-dc peak current limit is gradually increased to limit the sudden demand of current needed from the primary supply. This mode of operation guarantees that V_{OUT} monotonically increases and minimizes the probability of a voltage overshoot. Once 90% of the final V_{OUT} is reached, soft start mode ends, and Proportional (P) Mode starts. The total duration of soft start is load dependent as it affects how many switching cycles are required for V_{OUT} to reach 90% of final value. In this mode of operation, the voltage feedback loop is inactive, and hence, loop stability is not a concern.

3.3. Proportional Mode

Once the secondary side senses 90% of V_{OUT}, the control loop begins its P-mode operation. During this mode of operation, the dc-dc converter closes the loop (dc-dc converter secondary side communicates with the primary side), and therefore, analyzing the loop stability is required.

Figure 7 shows a simplified block diagram of the dc-dc control feedback loop. gm_p represents the equivalent modulator and power stage transconductance of the dc-dc converter, and resistors R5 and R6 are the feedback resistors used to sense V_{OUT}. C10 is the output capacitor, and R_{LOAD} represents output load. Parameter gm_{fb} and $R_{o,gmfb}$ are the effective error amplifier transconductance and the error amplifier output resistance, respectively. During the P-Mode, an integrated resistor R_{INT} is connected to the COMP pin.

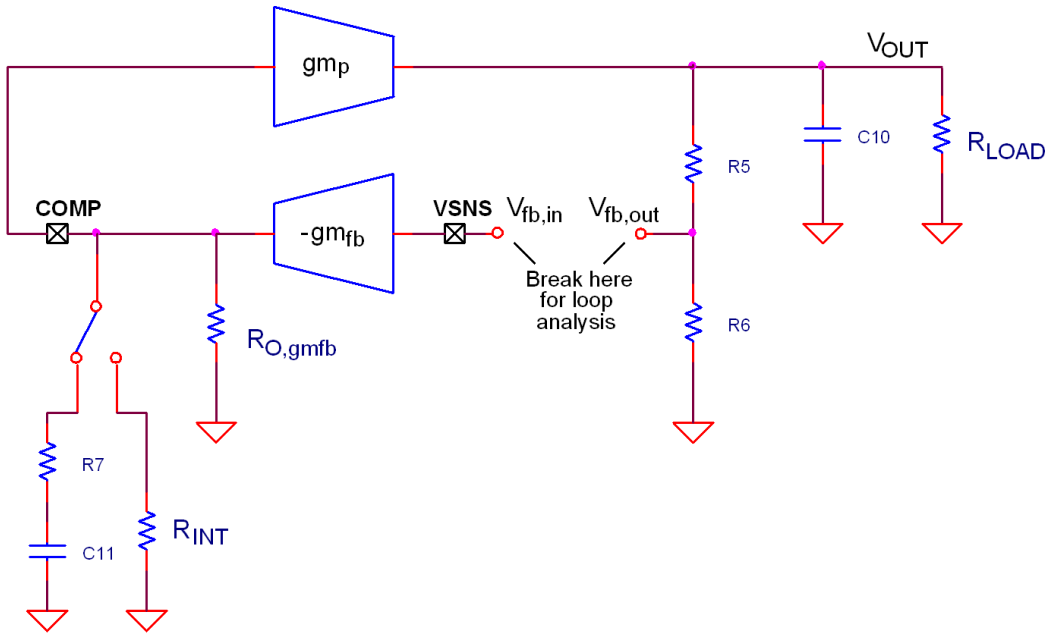

Figure 7. Simplified Feedback Loop

For stability analysis, the loop at the input of the error amplifier is broken to obtain the small-signal transfer function from $V_{fb,in}$ to $V_{fb,out}$:

$$H_P(S) = \frac{V_{fb,out}}{V_{fb,in}} = A_{DC,P}\frac{1}{\left(1+\frac{S}{\omega_p}\right)}$$

Equation 33.

$$\omega_p \cong \frac{1}{R_{load}C_{10}}$$

Equation 34.

$$A_{DC,P} = -\frac{R6}{R5+R6}gm_{fb}(R_{INT} \parallel R_{O,gmfb}) \times gm_p(R_{LOAD} \parallel (R5+R6))$$

Equation 35.

$$gm_{fb} = \frac{gm_{ea}}{gm_{ea}(R5 \parallel R6) + 1}$$

Equation 36.

gm_{ea} is the error amplifier transconductance. For the Si884xx/Si886xx, $gm_{ea} \cong 1x10^{-3}$, $R_{INT} \cong 100\ k\Omega$, and $R_{O,gmfb} \gg R_{INT}$. If R5 and R6 are chosen such that their parallel resistance is sufficiently larger than $1/gm_{ea}$, Equation 36 simplifies to:

$$gm_{fb} \cong \frac{1}{(R5 \parallel R6)}$$

Equation 37.

gm_p is given by:

$$gm_p \cong \frac{n}{10 \times R12}$$

Equation 38.

Typically, $R_{LOAD} \ll (R5 + R6)$ and the DC gain in P-mode simplifies to:

$$A_{DC,P} \cong -\frac{10 \times 10^3 \times n \times R_{LOAD}}{R5 \times R12}$$

Equation 39.

Notice that the DC gain of P mode is proportional to R_{LOAD} and inversely proportional to R5. At heavy loads (small R_{LOAD}), a very large R5 could significantly increase the output voltage error as the DC gain reduces. Conversely, a very small R5 increases power consumption and gm_{fb} variability due to higher dependency on gm_{ea}, which can significantly vary more than 1/(R5||R6) over temperature or from part to part. The total duration of this mode is approximately 7 ms.

3.4. Proportional Integral Mode

After P-mode, the controller switches to PI-mode, the steady state and final operation mode. During this mode of operation, the error amplifier drives an impedance that consists of the series combination of resistor R7 and capacitor C11. To achieve a smooth transition between P and PI modes, it is recommended to set R7 to match R_{INT}.

$$R7 = R_{INT} \approx 100 \times 10^3$$

Equation 40.

In PI-mode, the loop transfer is given by:

$$H_{PI}(S) = A_{DC,PI} \frac{\left(1 + \frac{S}{\omega_{z1}}\right)}{\left(1 + \frac{S}{\omega_{p1}}\right) \times \left(1 + \frac{S}{\omega_{p2}}\right)}$$

Equation 41.

where:

$$\omega_{p1} \cong \frac{1}{R_{O,gmfb} C11}$$

Equation 42.

$$\omega_{z1} = \frac{1}{R7 \times C11}$$

Equation 43.

$$\omega_{p2} \cong \frac{1}{R_{LOAD} C10}$$

Equation 44.

$$A_{DC,PI} \cong \pm \frac{R_{O,gmfb} gm_p R_{LOAD}}{R5}$$

Equation 45.

Notice that the loop transfer function in PI-Mode has an additional pole-zero pair when compared with P-Mode. In addition, the loop DC-gain is much higher in PI-Mode than in P-Mode due to $R_{O,gmfb} \gg R_{INT}$.

Figure 8 shows the magnitude Bode plot of the loop in PI mode.

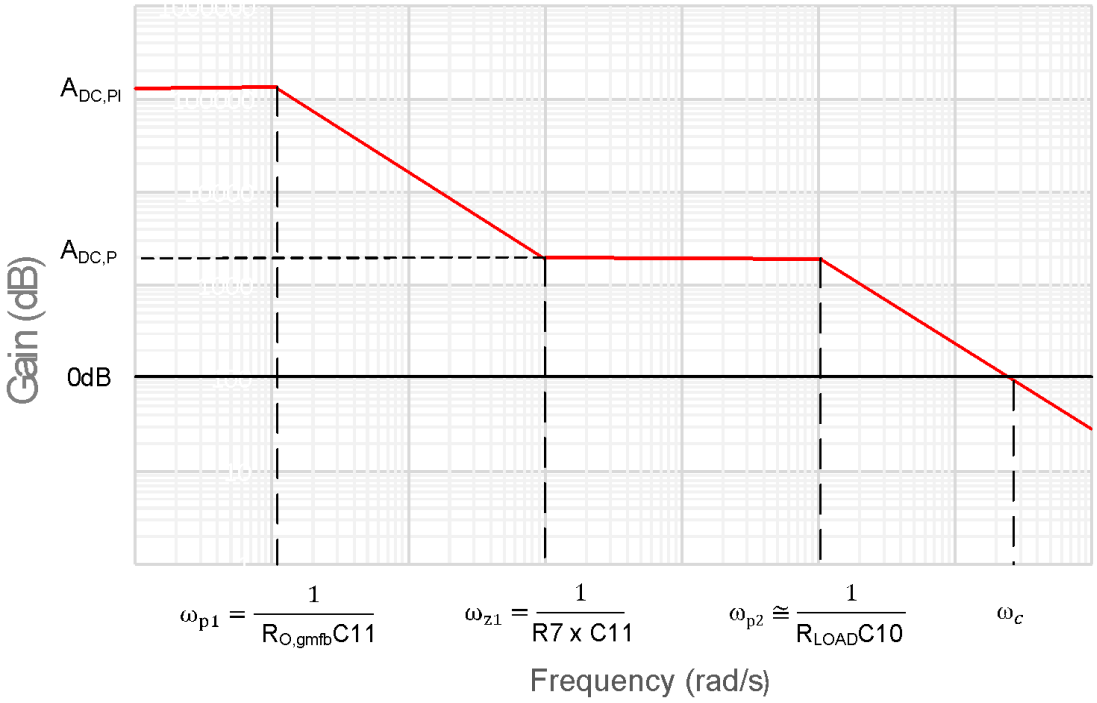

Figure 8. Simplified Bode Magnitude Plot of the Loop in PI Mode

4. Design Example

Consider the desired requirements listed in Table 1.

Table 1. Design Requirements

Parameter	Value
Input Voltage	24.0 V
Output Voltage	5.0 V
Input Voltage Ripple	≤ 50 mV
Output Voltage Ripple	≤ 50 mV
Maximum Output Current	1A

4.1. Transformer Design

For this example, operating in CCM was chosen. Equation 7 establishes the relationship between turns ratio n and duty cycle D. Accounting for forward voltage drop across D1 of 0.5 V and targeting a duty cycle of 40%, Equation 7 can be solved for transformer turns ratio n:

$$n \cong \frac{V_{IN}D}{(V_{OUT} + Vf_{D1})(1-D)} \cong \frac{24 \times 0.4}{5.5 \times 0.6} \cong 2.91$$

Equation 46.

A 3:1 turns ratio was chosen.

The next parameters to choose are the switching period and primary inductance. The Si886xx has externally set switching frequency range of 200 kHz to 900 kHz. 500 kHz was chosen for this example. C6 is set to 470 nF and R13 is calculated by rearranging Equation 31:

$$R13 = \frac{1025.5 \times T_{sw}}{C6} = \frac{1025.5 \times 2 \times 10^{-6}}{470 \times 10^{-9}} = 4.36\text{k}\Omega$$

Equation 47.

R13 was set to 4.32 kΩ as that is the closest 1% resistor value.

To determine L_m, consider at what minimum load should the converter operate in CCM. For this design, it was targeted to operate in CCM between 70% and full load. At the cross-over point between DCM and CCM:

$$Im_{AVE} = \frac{Im_{RIPPLE}}{2}$$

Equation 48.

Substituting,

$$\frac{0.7 \times I_{LOAD}}{n(1-D)} = \frac{V_{IN}DT_{sw}}{2L_m}$$

Equation 49.

And solving for L_m:

$$L_m = \frac{nV_{IN}D(1-D)T_{sw}}{1.4 \times I_{LOAD}} = \frac{3 \times 24 \times 0.4 \times 0.6 \times 2 \times 10^{-6}}{1.4} = 24.7\mu\text{H}$$

Equation 50.

A transformer with turns ratio of 3:1 and primary inductance of 25 µH was chosen.

4.2. R12 Sense Resistor Selection

R12 is chosen to provide a cycle by cycle current limit. Equation 10 gives the average magnetizing current at specified load.

$$Im_{AVE} = \frac{I_{LOAD}}{n(1-D)} = \frac{1}{3 \times 0.6} = 556mA$$

Equation 51.

The peak current in CCM is:

$$I_{m,PK,CCM} = I_{m,AVE} + \frac{V_{IN}DT_{sw}}{2L_m} = 0.556 + \frac{24 \times 0.4 \times 2 \times 10^{-6}}{2 \times 25 \times 10^{-6}} = 0.94A$$

Equation 52.

Allowing for some variation in performance from design calculations, 1 A current limit is chosen. Applying Equation 13 and calculating for R12:

$$R12 = \frac{100mV}{I_{m,LIMIT}} = \frac{0.1}{1} = 100m\Omega$$

Equation 53.

Figure 9 shows the expected magnetizing current waveform at specified load.

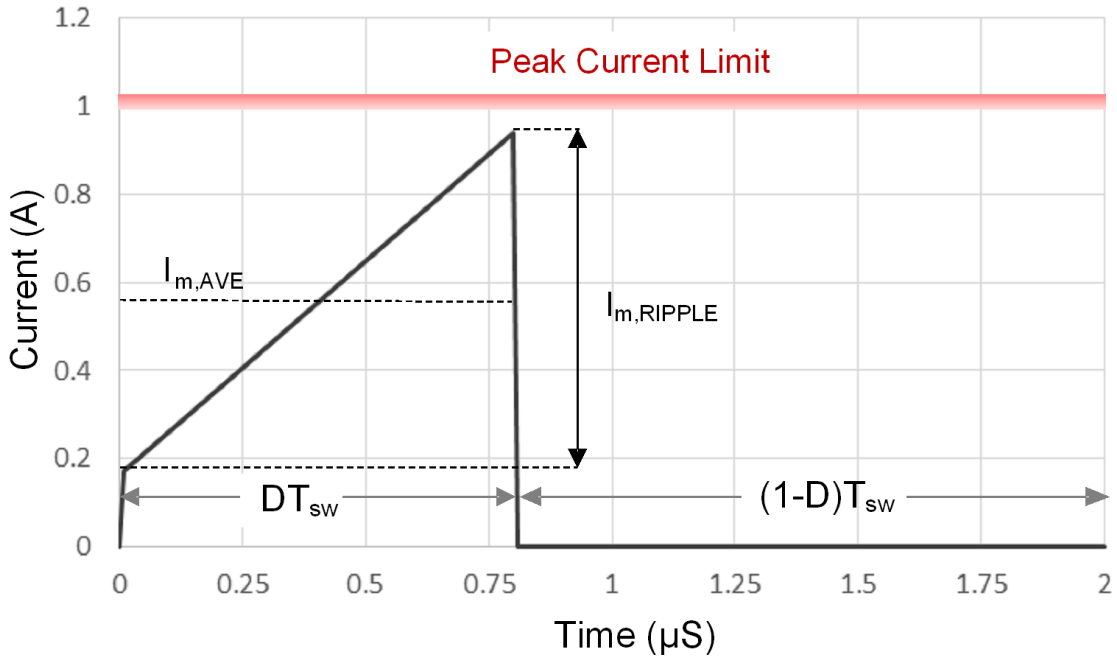

Figure 9. Magnetizing Current

4.3. Q1 Selection

The instant S1 opens, Q1's drain voltage increases rapidly from nearly 0 V and settles to:

$$V_{ds,(1-D)} = V_{IN} + n(V_{OUT} + V_{fD1}) = 24 + 16.5 = 40.5V$$

Equation 54.

However, energy stored in L_{lkg} must be dissipated in the secondary which causes $V_{ds,(D)}$ to spike a higher voltage. Q1 must be able to tolerate this voltage spike between drain and source.

A N-channel MOSFET with 100 V rating was chosen to accommodate the expected voltage stress caused by L_{lkg}

4.4. D1 Selection

Equation 25 and 26 define the requirements for D1. Substituting into Equation 25,

$$I_{D1,AVE(1-D)} = \frac{I_{LOAD}}{1-D} = \frac{1}{0.6} = 1.6A$$

Equation 55.

Diode current capacities are specified in rms. Assuming a linear current through D1, consider the translation of average to rms:

$$I_{D1,RMS(1-D)} = I_{D1,AVE(1-D)}\left(\frac{2}{\sqrt{3}}\right) = 1.84A$$

Equation 56.

Substituting into Equation 26:

$$V_{D1,REV(D)} = \frac{V_{IN}}{n} + V_{OUT} = \frac{24}{3} + 5 = 13V$$

Equation 57.

Equation 26 and 57 do not include the voltage spike due to the interaction of the diode capacitance and secondary side leakage inductance, and as a result, a diode with a larger withstanding voltage is required in practice.

When selecting D1, diodes with low V_f are the preferred choice as it minimizes the associated power loss.

$$P_{D1(1-D)} = V_{fD1} \times I_{D1,AVE(1-D)}$$

Equation 58.

Several diodes were tested in the circuit. A 5 A, 50 V diode was chosen for its tolerance to high operating temperatures at which diode leakage and package heat transfer characteristics affect overall performance and efficiency.

4.5. External Regulator Circuit

For this design, an external regulator circuit was designed to work with the VREGA voltage reference to create a regulated supply for VDDA. R14 was selected for a 950 µA sink current.

$$R14 = \frac{V_{IN} - V_{REGA}}{I_R} = \frac{24 - 4.85}{0.00095} = 20.15k\Omega$$

Equation 59.

R14 was set to 19.6 kΩ and C14 to the recommended 0.1 µF. MMBT2222 was selected for Q1.

4.6. C10 Selection

C10 is inversely proportional to output voltage ripple and sets the crossover frequency of control loop gain. Solving Equation 23,

$$C10 = \frac{I_{LOAD} DT_{sw}}{V_{OUT,RIPPLE}} \geq \frac{1 \times 0.4 \times 2 \times 10^{-6}}{0.05} \geq 16\mu F$$

Equation 60.

A 22 µF X7R capacitor in 1210 package was chosen.

4.7. C2 Selection

In most applications, V_{IN} also supplies the VDDA pin that powers the dc-dc controller and left side digital isolator circuitry. It is recommended to minimize voltage ripple at VDDA. Solving Equation 19:

$$C2 \geq \frac{I_{LOAD} DT_{sw}}{V_{IN,RIPPLE} \times n} \geq \frac{1 \times 0.4 \times 2 \times 10^{-6}}{0.05 \times 3} \geq 5.33\mu F$$

Equation 61.

A 10 µF X7R capacitor in 1210 package was chosen.

4.8. R5 and R6 Selection

The ratios of R5 and R6 are determined by the 5 V output voltage requirement. To reduce the dependence of feedback gain on the internal error amplifier transconductance, it is recommended to have the parallel combination resistance to be ≥10 kΩ. Higher values of R5 and R6 reduce power loss through the divider, but at the expense of increasing output voltage error due to I_{VSNS}, which varies part to part. So R5 and R6 are chosen to target 10 kΩ parallel resistance.

$$10 \times 10^3 = \frac{R5 \times R6}{R5 + R6}$$

Equation 62.

$$5 = 1.05\left(\frac{R5}{R6} + 1\right)$$

Equation 63.

Substituting Equation 52 into Equation 53 and solving for R6,

$$10 \times 10^3 = \frac{3.76R6}{4.76}, \quad R6 = 12.66 \times 10^3, R5 = 48.1 \times 10^3$$

Equation 64.

The nearest 1% resistor to 12.66 kΩ is 12.7 kΩ. However, setting R5 to either 47.5 kΩ or 48.7 kΩ does not target exactly 5 V as well as other 1% resistor pairs. A better match was found with R6 = 13.3 kΩ and R5 = 49.9 kΩ.

4.9. Compensation Network

The compensation network is comprised of R7 and C11. R7 is selected to match R_{INT} and 100 kΩ is the nearest 1% resistor value. The C11 places the compensation zero in relationship to the crossover frequency. The equation for crossover frequency can be obtained by multiplying the P-mode gain (Equation 33), by the frequency of the pole created by R_{LOAD} and C10 (Equation 39):

$$f_c \cong \frac{10\times10^3 \times n \times R_{LOAD}}{R5 \times R12} \times \frac{1}{2\pi R_{LOAD} C10} \cong 43kHz$$

Equation 65.

To achieve good phase margin, it suggested to place the compensation zero near the pole created by R_{LOAD} and C10.

$$C11 = \frac{1}{2\pi f_{p2} \times R7} = \frac{R_{LOAD} C10}{R7} = \frac{5 \times 22\times10^{-6}}{100\times10^3} = 1.1nF$$

Equation 66.

A 1.5 nF capacitor was chosen.

4.10. Primary Snubber

Without R19 and C16 installed, V_{ds} of Q1 was measured to spike at 108 V and ring briefly at 30 MHz until the energy stored in L_{lkg} dissipated. See Figure 10:

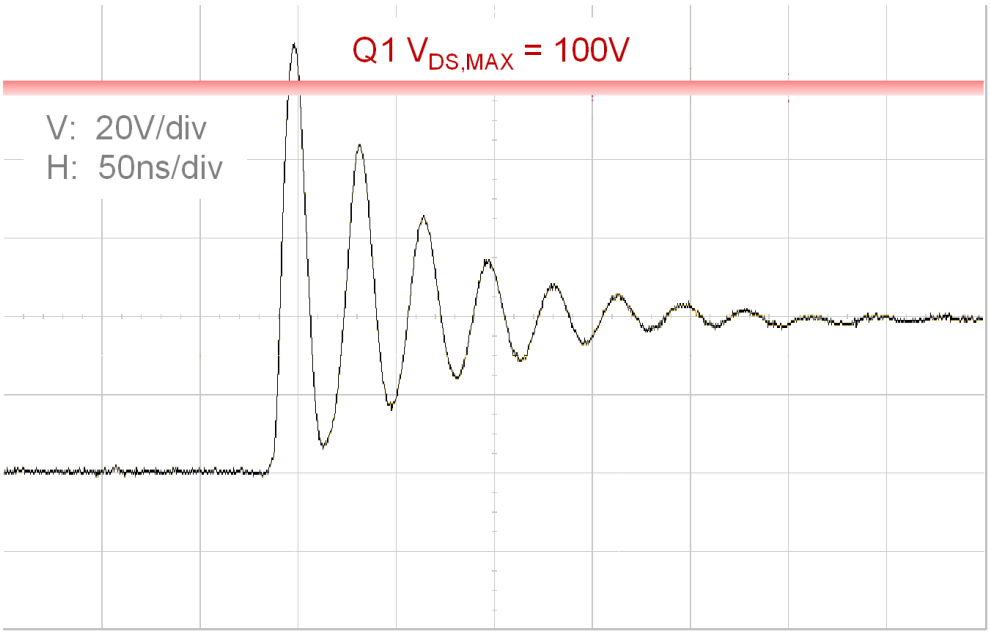

Figure 10. Undamped Vds Ringing

T1 was removed from the board and its primary inductance leakage was measured to be 456 nH. Applying Equation 16 and Equation 17, R16 and C19 were calculated:

$$R16 = 2\pi f_{ring} L_{lkg} = 2\pi \times 30\times10^6 \times 456\times10^{-9} = 86\Omega$$

Equation 67.

$$C19 = \frac{1}{2\pi f_{ring} R16} = \frac{1}{2\pi \times 30 \times 10^{6} \times 86} = 62pF$$

Equation 68.

Closest standard component values of R16 = 82 Ω and C19 = 68 pF were selected and installed. Q1 Vds was measured again to gage effectiveness of the RC snubber. Voltage spike was reduced to 74 V as shown in Figure 11.

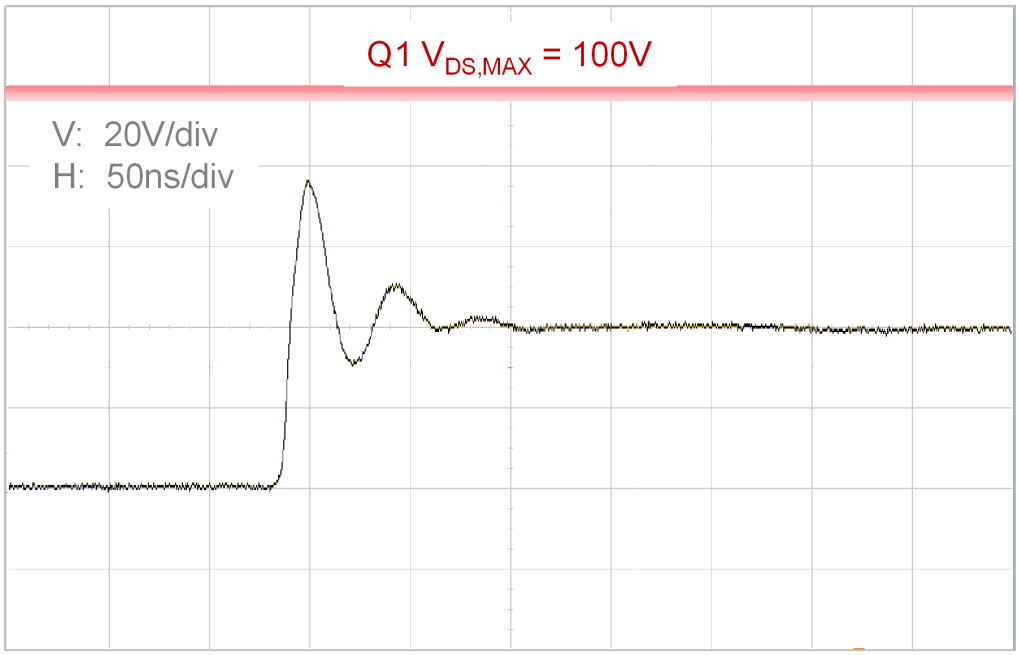

Figure 11. Damped Vds Ringing

R8 and C8 on the secondary side can be selected using the same methodology. Without a secondary side snubber, the voltage spike across D1 at the instant that S1 closes was measured to be 35 V with a ringing frequency of 59 MHz. T1 was removed from the board and its primary inductance leakage was measured to be 74 nH.

$$R8 = 2\pi f_{ring} L_{lkg} = 2\pi \times 59 \times 10^{6} \times 74 \times 10^{-9} = 27.4\Omega$$

Equation 69.

$$C8 = \frac{1}{2\pi f_{ring} R8} = \frac{1}{2\pi \times 59 \times 10^{6} \times 27.4} = 98.4pF$$

Equation 70.

R8 is a 1% resistor value and C8 of 100 pF was chosen. The voltage spike was reduced to 23 V and the ringing damped.

4.11. Design Summary

Table 2 shows the component selection that meets design requirements.

Table 2. Ordering Guide

Part Reference	Description	Manufacturer	Manufacturer Part Number
C2	CAP, 10 µF, 50 V, ±20%, X7R, 1210	Venkel	C1210X7R500-106M
C6	CAP, 0.4 µF, 16 V, ±10%, X7R, 0805	Venkel	C0805X7R160-474K
C8	CAP, 100 pF, 50 V, ±10%, X7R, 0603	Venkel	C0603X7R500-101K
C10	CAP, 22 µF, 25 V, ±10%, X7R, 1210	Venkel	C1210X7R250-226M
C11	CAP, 1.5 nF, 25 V, ±10%, X5R, 0603	Venkel	C0603X5R250-152K
C14	CAP, 0.1 µF, 10 V, ±10%, X7R, 0603	Venkel	C0603X7R100-104K
C19	CAP, 68 pF, 100 V, ±10%, C0G, 0603	Venkel	C0603C0G101-680K
D1	DIO, SUPER BARRIER, 50 V, 5.0 A, SMA	Diodes Inc.	SBRT5A50SA
Q1	TRANSISTOR, MOSFET, N-CHNL, 100 V, 3.7 A, 3 W, Switching, SOT223	Fairchild	FDT3612
Q2	TRANSISTOR, NPN, 30V, 600mA, SOT23	On Semi	MMBT2222LT1
R5	RES, 49.9 K, 1/16 W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-4992F
R6	RES, 13.3 K, 1/16 W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-1332F
R7	RES, 100 K, 1/10 W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-1003F
R8	RES, 27.4 Ω, 1/10 W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-27R4F
R12	RES, 0.1 Ω, 1/2 W, ±1%, ThickFilm, 1206	Venkel	LCR1206-R100F
R13	RES, 4.32 K, 1/10 W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-4321F
R14	RES, 19.6 K, 1/16 W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-1962F
R16	RES, 82.0 Ω, 1/10 W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-82R0F
T1	TRANSFORMER, Flyback, 25 µH Primary, 500 nH Leakage, 3:1, SMT	UMEC	UTB02205s
U1	IC, ISOLATOR, DC DC External Switch, Freq Control, 2 Digital Ch, SO20 WB	Silicon Labs	Si88621ED-IS

Contact Information

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
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