



# STL8N65M5

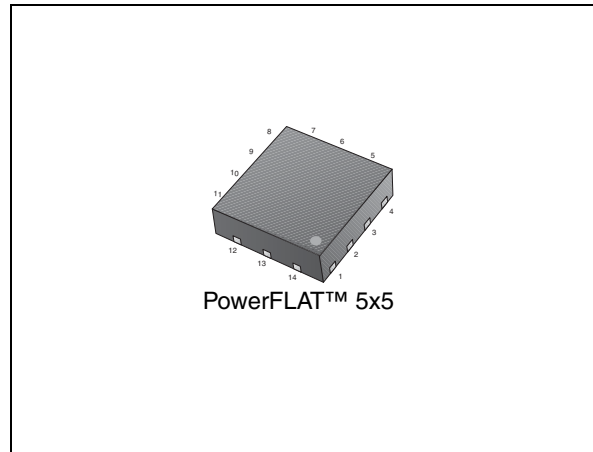
N-channel 650 V, 0.56  $\Omega$ , 7 A MDmesh™ V  
Power MOSFET in PowerFLAT™ 5x5

## Features

| Order code | V <sub>DSS</sub> @<br>T <sub>Jmax</sub> | R <sub>DS(on)</sub><br>max | I <sub>D</sub>     |
|------------|---|----------------------------|--------------------|
| STL8N65M5  | 710 V                                   | < 0.6 $\Omega$             | 7 A <sup>(1)</sup> |

1. The value is rated according to R<sub>thj-case</sub>

- Worldwide best R<sub>DS(on)</sub> \* area
- Higher V<sub>DSS</sub> rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



## Applications

- Switching applications

## Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

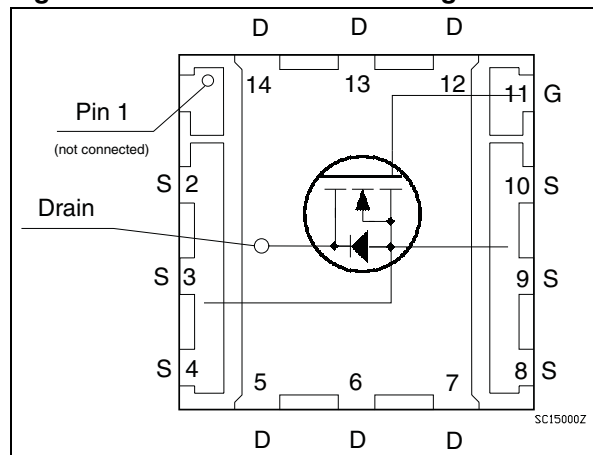


Table 1. Device summary

| Order code | Marking | Package        | Packaging     |
|------------|---------|----------------|---------------|
| STL8N65M5  | 8N65M5  | PowerFLAT™ 5x5 | Tape and reel |

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol             | Parameter  | Value       | Unit             |
|--------------------|--|-------------|------------------|
| $V_{DS}$           | Drain-source voltage ( $V_{GS} = 0$ )  | 650         | V                |
| $V_{GS}$           | Gate-source voltage  | $\pm 25$    | V                |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$   | 7           | A                |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$  | 4.4         | A                |
| $I_D^{(2)}$        | Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$   | 1.4         | A                |
| $I_D^{(2)}$        | Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$  | 0.6         | A                |
| $I_{DM}^{(2),(3)}$ | Drain current (pulsed)   | 5.6         | A                |
| $P_{TOT}^{(2)}$    | Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$  | 2.5         | W                |
| $P_{TOT}^{(1)}$    | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$  | 70          | W                |
| $I_{AR}$           | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)                                   | 2           | A                |
| $E_{AS}$           | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 120         | mJ               |
| $dv/dt^{(4)}$      | Peak diode recovery voltage slope  | 15          | V/ns             |
| $T_{stg}$          | Storage temperature  | - 55 to 150 | $^\circ\text{C}$ |
| $T_j$              | Max. operating junction temperature  | 150         | $^\circ\text{C}$ |

1. The value is rated according to  $R_{thj-case}$
2. When mounted on FR-4 board of  $1\text{ inch}^2$ , 2oz Cu
3. Pulse with limited by safe operating area.
4.  $I_{SD} \leq 7\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{Peak} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

**Table 3. Thermal data**

| Symbol              | Parameter                            | Value | Unit                      |
|---------------------|--------------------------------------|-------|---------------------------|
| $R_{thj-case}$      | Thermal resistance junction-case max | 1.78  | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb max  | 60    | $^\circ\text{C}/\text{W}$ |

1. When mounted on  $1\text{ inch}^2$  FR-4 board, 2 oz Cu

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

| Symbol        | Parameter  | Test conditions   | Min. | Typ. | Max.     | Unit                           |
|---------------|--|---|------|------|----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ( $V_{GS} = 0$ )  | $I_D = 1\text{ mA}$   | 650  |      |          | V                              |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = 650\text{ V}$<br>$V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$ |      |      | 1<br>100 | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 25\text{ V}$  |      |      | 100      | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$                         | 3    | 4    | 5        | V                              |
| $R_{DS(on)}$  | Static drain-source on resistance                | $V_{GS} = 10\text{ V}, I_D = 3.5\text{ A}$                              |      | 0.56 | 0.6      | $\Omega$                       |

**Table 5. Dynamic**

| Symbol            | Parameter                             | Test conditions  | Min. | Typ. | Max. | Unit     |
|-------------------|---------------------------------------|--|------|------|------|----------|
| $C_{iss}$         | Input capacitance                     | $V_{DS} = 100\text{ V}, f = 1\text{ MHz},$<br>$V_{GS} = 0$   | -    | 690  | -    | pF       |
| $C_{oss}$         | Output capacitance                    |  |      | 18   |      | pF       |
| $C_{rss}$         | Reverse transfer capacitance          |  |      | 2    |      | pF       |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance time related   | $V_{DS} = 0\text{ to }520\text{ V}, V_{GS} = 0$  | -    | 17   | -    | pF       |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance energy related |  |      | 52   |      | pF       |
| $R_G$             | Intrinsic gate resistance             | $f = 1\text{ MHz open drain}$  | -    | 2.4  | -    | $\Omega$ |
| $Q_g$             | Total gate charge                     | $V_{DD} = 520\text{ V}, I_D = 3.5\text{ A},$<br>$V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 15</a> ) | -    | 15   | -    | nC       |
| $Q_{gs}$          | Gate-source charge                    |  |      | 3.6  |      | nC       |
| $Q_{gd}$          | Gate-drain charge                     |  |      | 6    |      | nC       |

- $C_{oss\text{ eq}}$ , time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
- $C_{oss\text{ eq}}$ , energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                | Min. | Typ. | Max | Unit |
|--------------|---------------------|--|------|------|-----|------|
| $t_{d(off)}$ | Turn-off delay time | $V_{DD} = 400\text{ V}$ , $I_D = 4\text{ A}$ , |      | 50   |     | ns   |
| $t_r(V)$     | Rise time           | $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$   | -    | 14   | -   | ns   |
| $t_{c(off)}$ | Cross time          | (see <a href="#">Figure 16</a> ),              |      | 20   |     | ns   |
| $t_{f(i)}$   | Fall time           | (see <a href="#">Figure 19</a> )               |      | 11   |     | ns   |

**Table 7. Source drain diode**

| Symbol          | Parameter                     | Test conditions   | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|---|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |   | -    |      | 7    | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |   | -    |      | 28   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 7\text{ A}$ , $V_{GS} = 0$                        | -    |      | 1.5  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$  | -    | 200  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       | $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 16</a> )    |      | 1.6  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |   |      | 16   |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$  | -    | 263  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       | $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ | -    | 1.9  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      | (see <a href="#">Figure 16</a> )                            |      | 15   |      | A             |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

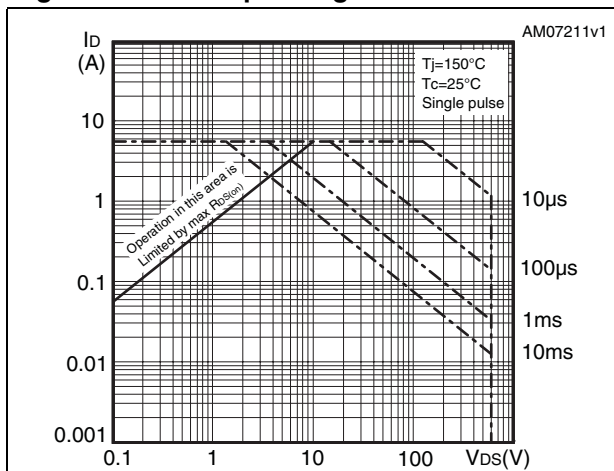


Figure 3. Thermal impedance

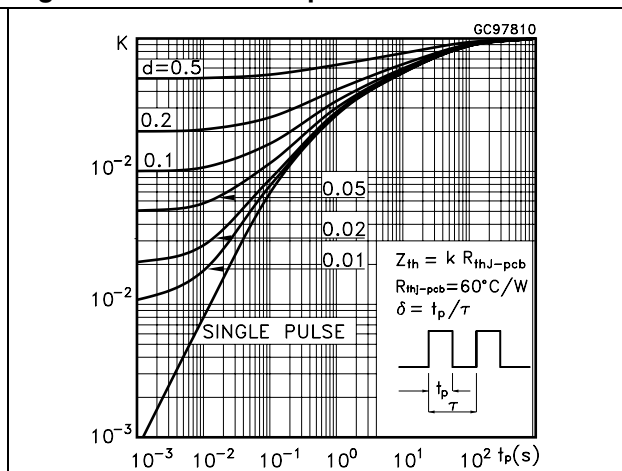


Figure 4. Output characteristics

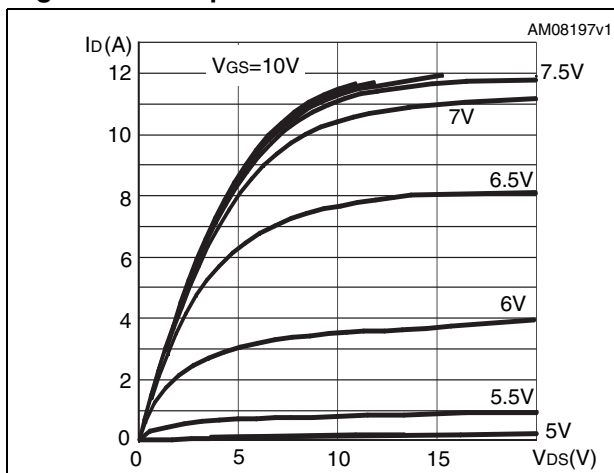


Figure 5. Transfer characteristics

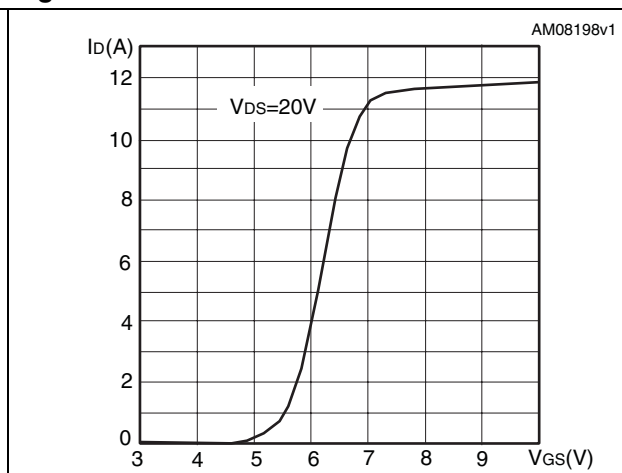


Figure 6. Gate charge vs gate-source voltage

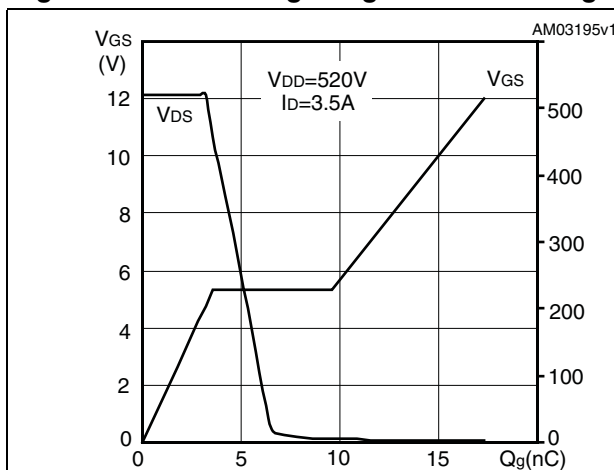


Figure 7. Static drain-source on resistance

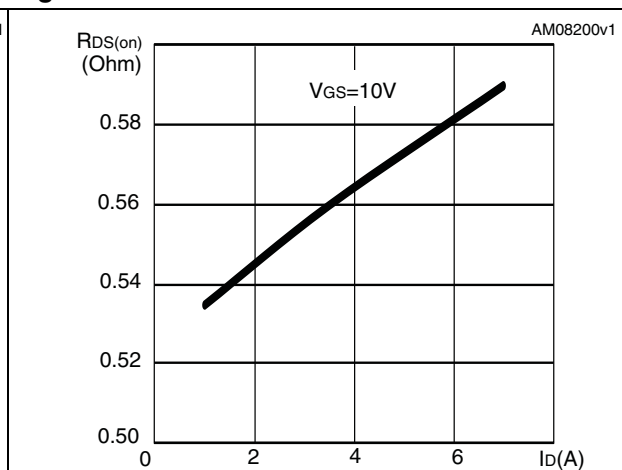


Figure 8. Capacitance variations

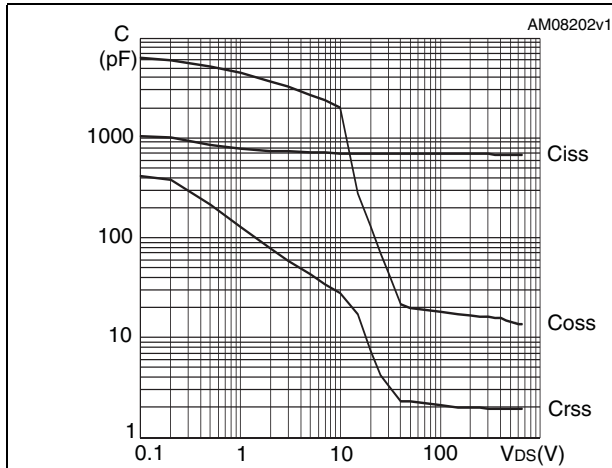


Figure 9. Output capacitance stored energy

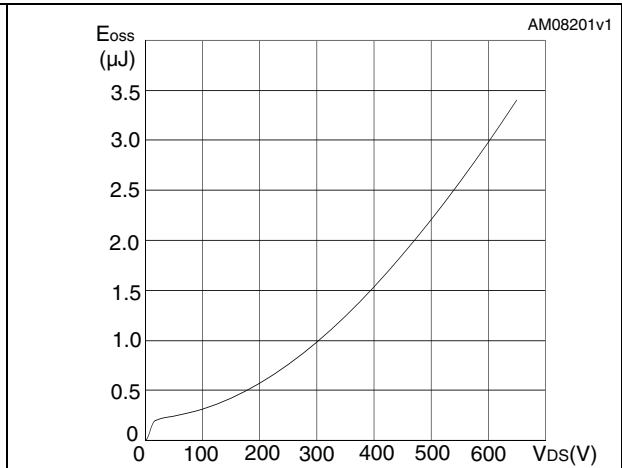


Figure 10. Normalized gate threshold voltage vs temperature

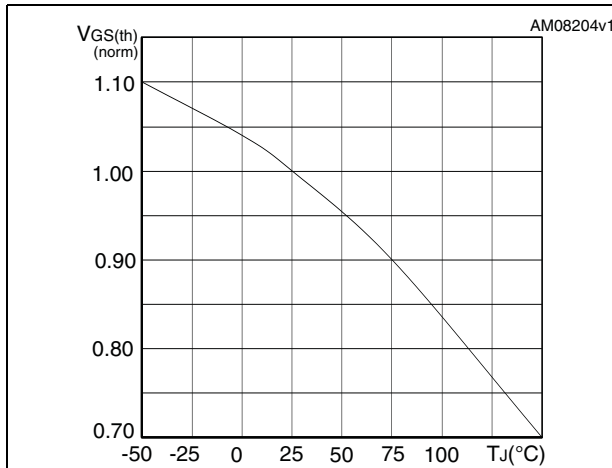


Figure 11. Normalized on resistance vs temperature

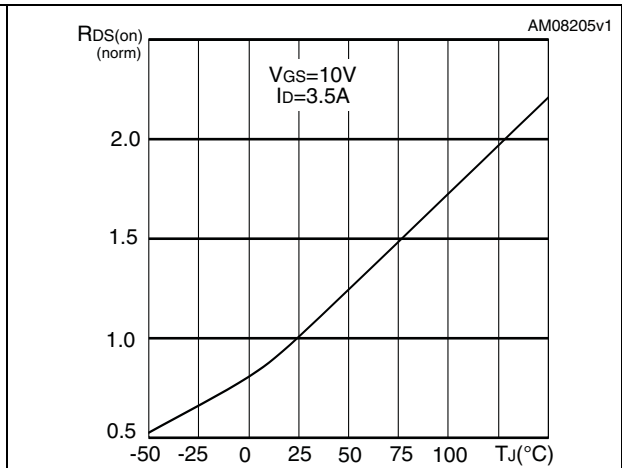


Figure 12. Switching losses vs gate resistance (1)

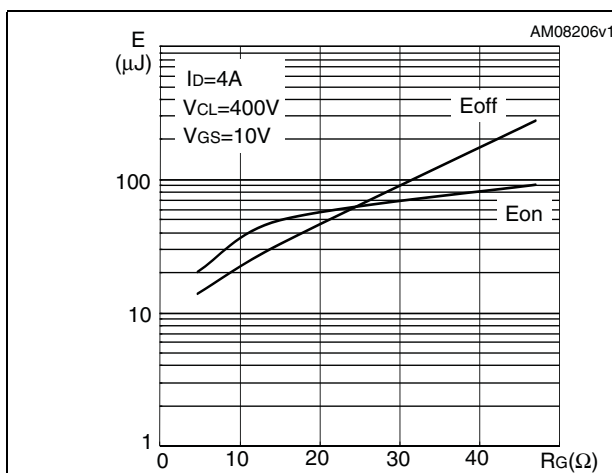
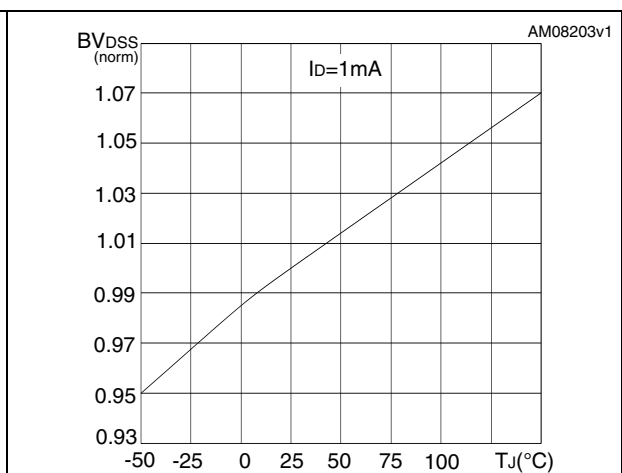


Figure 13. Normalized B<sub>VDSS</sub> vs temperature



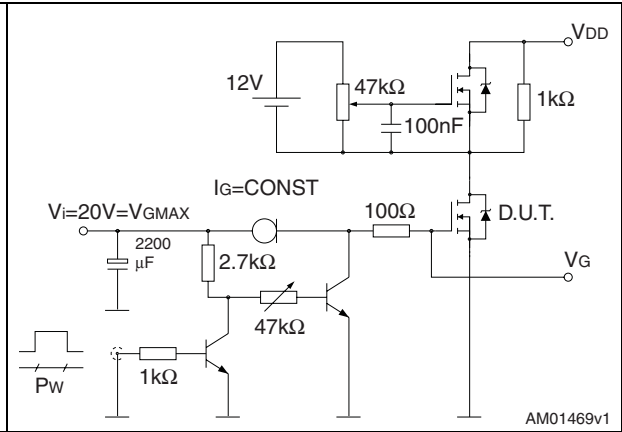
1. E<sub>on</sub> including reverse recovery of a SiC diode

### 3 Test circuits

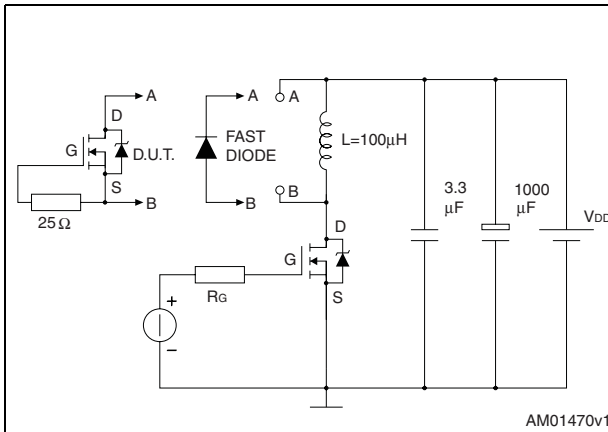
**Figure 14. Switching times test circuit for resistive load**



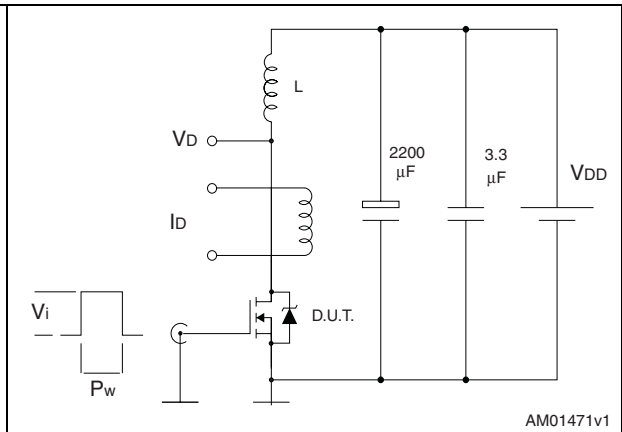
**Figure 15. Gate charge test circuit**



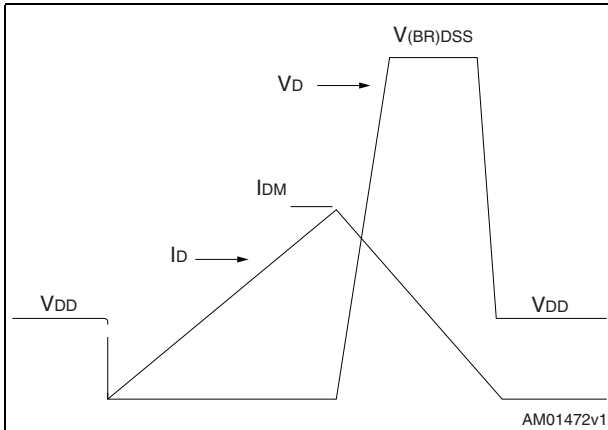
**Figure 16. Test circuit for inductive load switching and diode recovery times**



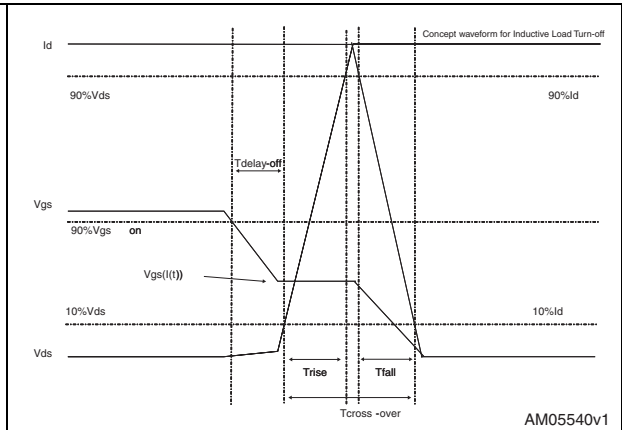
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x5 mechanical dimensions

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 0.80 | 0.90 | 1.0  |
| A1   | 0    | 0.02 | 0.05 |
| A3   |      | 0.24 |      |
| D    | 4.90 | 5.0  | 5.10 |
| E    | 4.90 | 5.0  | 5.10 |
| E2   | 2.49 | 2.57 | 2.64 |
| e    | 1.22 | 1.27 | 1.32 |
| b    | 0.43 | 0.51 | 0.58 |
| c    | 0.64 | 0.71 | 0.79 |

Figure 20. PowerFLAT™ 5x5 mechanical drawing

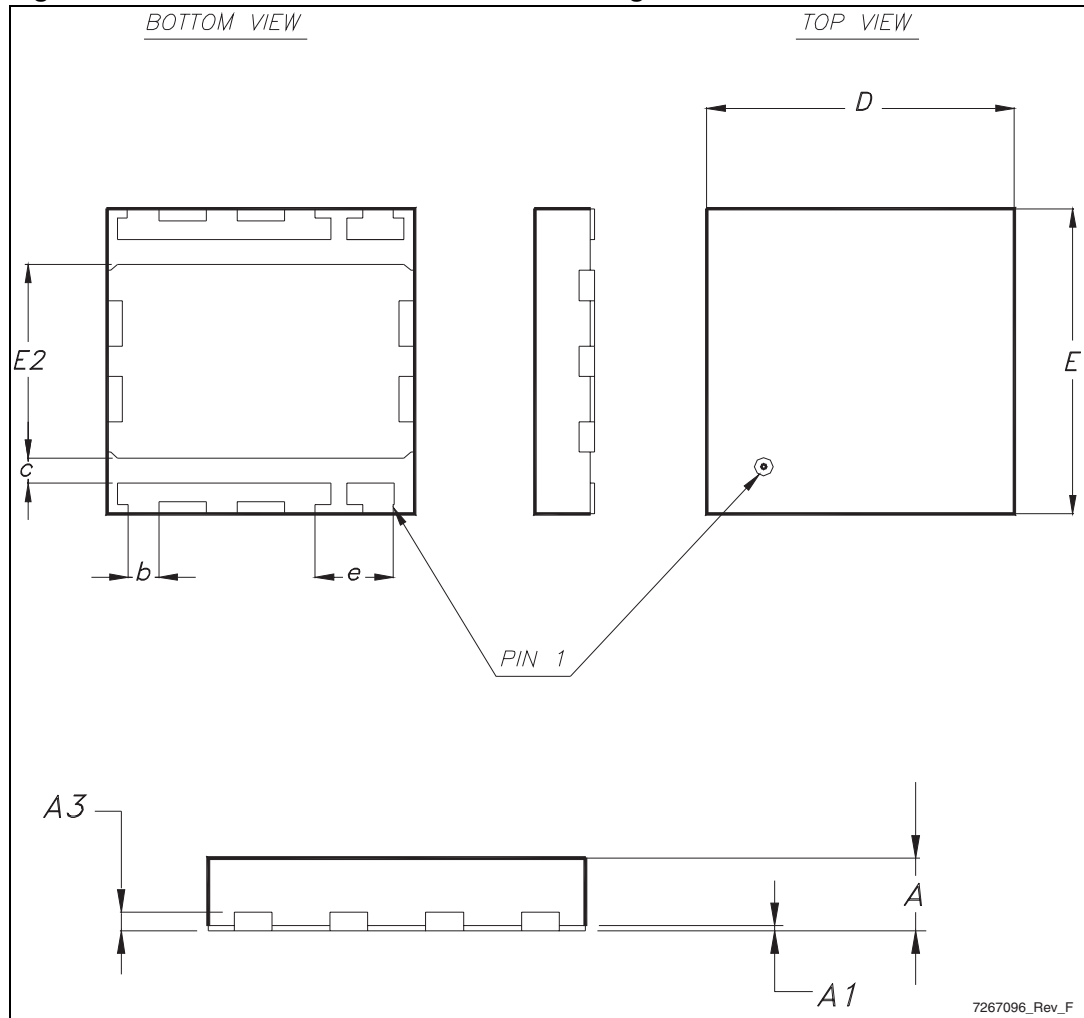
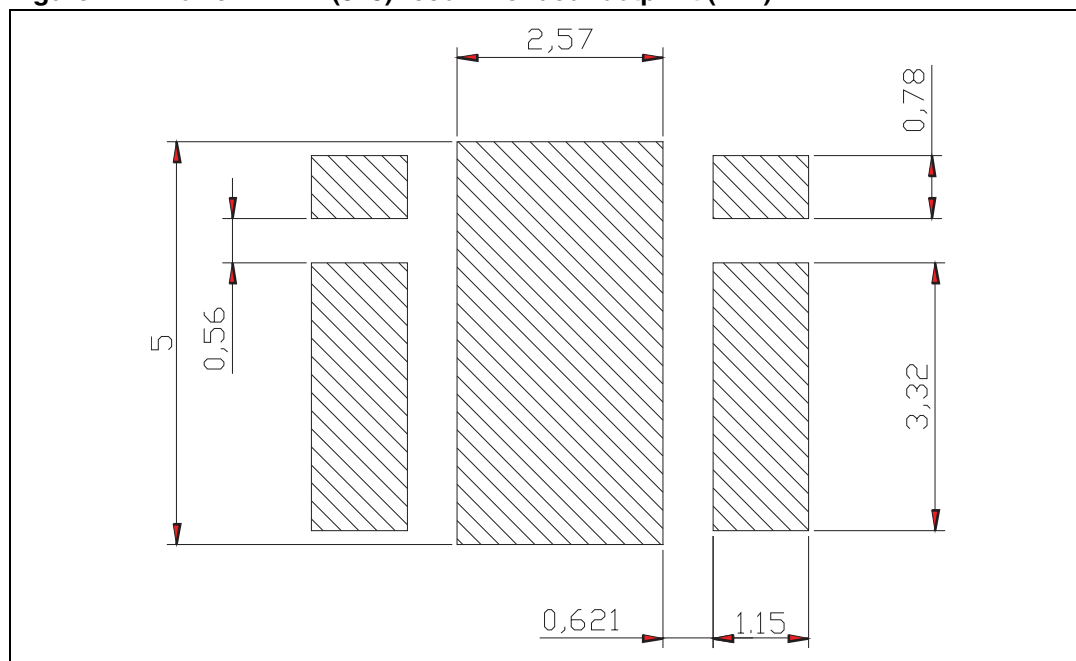


Figure 21. PowerFLAT™(5x5) recommended footprint (mm)



## 5 Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes   |
|-------------|----------|---|
| 05-Jul-2011 | 1        | First release   |
| 07-Jul-2011 | 2        | Updated <a href="#">Figure 1</a> .  |
| 08-Aug-2011 | 3        | Updated <a href="#">Figure 3: Thermal impedance</a> . and $R_{thj-pcb}$ value in <a href="#">Table 3: Thermal data</a> .<br>Minor text changes. |

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