

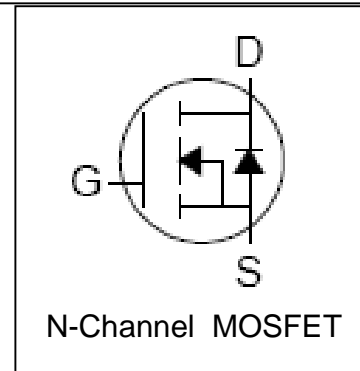
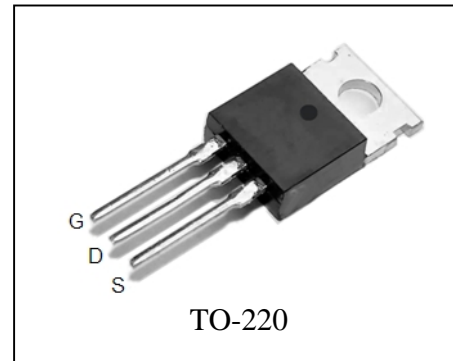
Features

- 70V/85A,
 $R_{DS(ON)} = 6m$ (Typ.) @ $V_{GS} = 10V$
- Super High Dense Cell Design
- Ultra Low On-Resistance
- 100% avalanche tested
- Lead Free and Green Devices Available
 (RoHS Compliant)

Applications

- Power Supply

Pin Description



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
Common Ratings ($T_C = 25^\circ C$ Unless Otherwise Noted)			
V_{DSS}	Drain-Source Voltage	70	V
V_{GSS}	Gate-Source Voltage	± 25	
T_J	Maximum Junction Temperature	175	$^\circ C$
T_{STG}	Storage Temperature Range	-55 to 175	$^\circ C$
I_S	Diode Continuous Forward Current	$T_C = 25^\circ C$ 85 ^①	A
Mounted on Large Heat Sink			
I_{DP}	300 μs Pulse Drain Current Tested	$T_C = 25^\circ C$ 340 ^②	A
I_D	Continuous Drain Current ($V_{GS} = 10V$)	$T_C = 25^\circ C$ 85 ^①	A
		$T_C = 100^\circ C$ 63	
P_D	Maximum Power Dissipation	$T_C = 25^\circ C$ 125	W
		$T_C = 100^\circ C$ 62.5	W
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1.2	$^\circ C/W$
Drain-Source Avalanche Ratings			
E_{AS} ^③	Avalanche Energy, Single Pulsed	256	mJ

Electrical Characteristics ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	RU7085R			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	70			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=70V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			1	μA
					30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	2	3	4	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 25V, V_{DS}=0V$			± 100	nA
$R_{DS(ON)}^{(4)}$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=40A$		6	8	m Ω
Diode Characteristics						
$V_{SD}^{(4)}$	Diode Forward Voltage	$I_{SD}=20A, V_{GS}=0V$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD}=40A, di_{SD}/dt=100A/\mu s$		45		ns
Q_{rr}	Reverse Recovery Charge			90		nC
Dynamic Characteristics ⁽⁵⁾						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$		1.6		Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=35V,$ Frequency=1.0MHz		3650		pF
C_{oss}	Output Capacitance			980		
C_{riss}	Reverse Transfer Capacitance			265		
$t_{d(ON)}$	Turn-on Delay Time			40		
t_r	Turn-on Rise Time	$V_{DD}=35V, R_L=0.8\Omega,$ $I_{DS}=40A, V_{GEN}=10V,$ $R_G=4.7\Omega$		136		
$t_{d(OFF)}$	Turn-off Delay Time			184		
t_f	Turn-off Fall Time			96		
Gate Charge Characteristics ⁽⁵⁾						
Q_g	Total Gate Charge	$V_{DS}=56V, V_{GS}=10V,$ $I_{DS}=40A$		65		nC
Q_{gs}	Gate-Source Charge			15		
Q_{gd}	Gate-Drain Charge			24		

Notes: ① Calculated continuous current based on maximum allowable junction temperature. Package Limitation current is 75A.

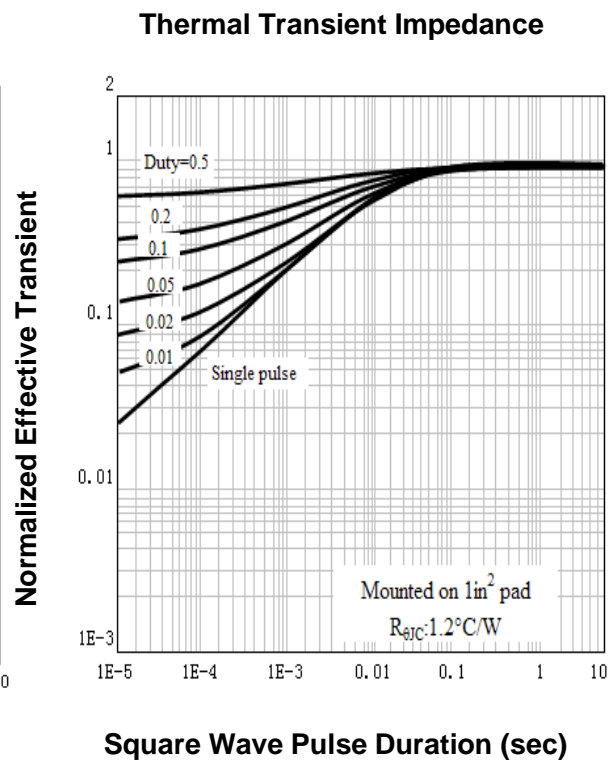
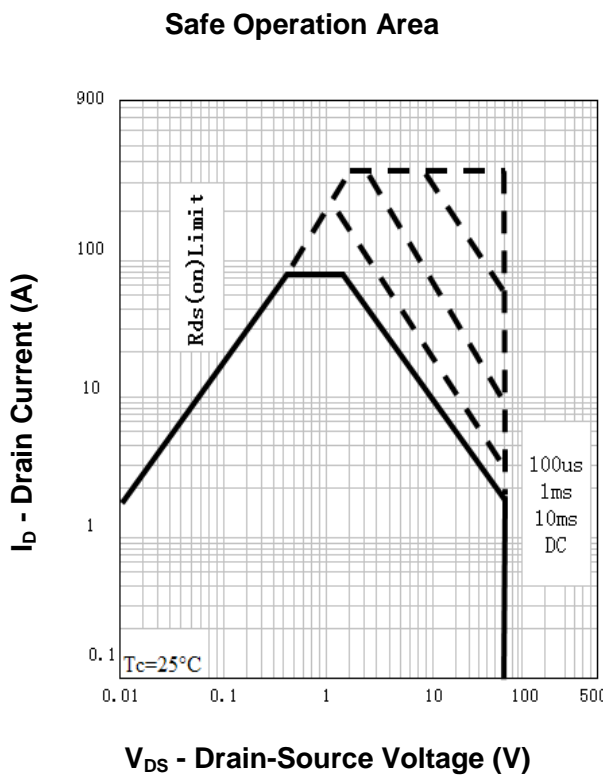
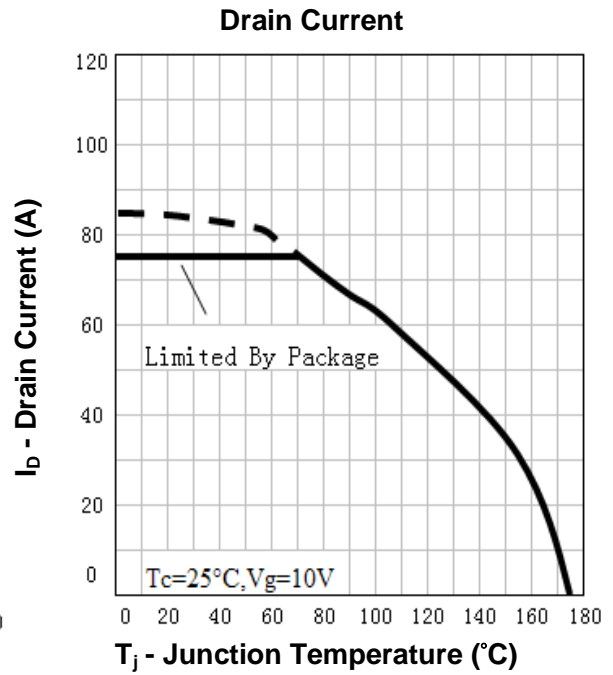
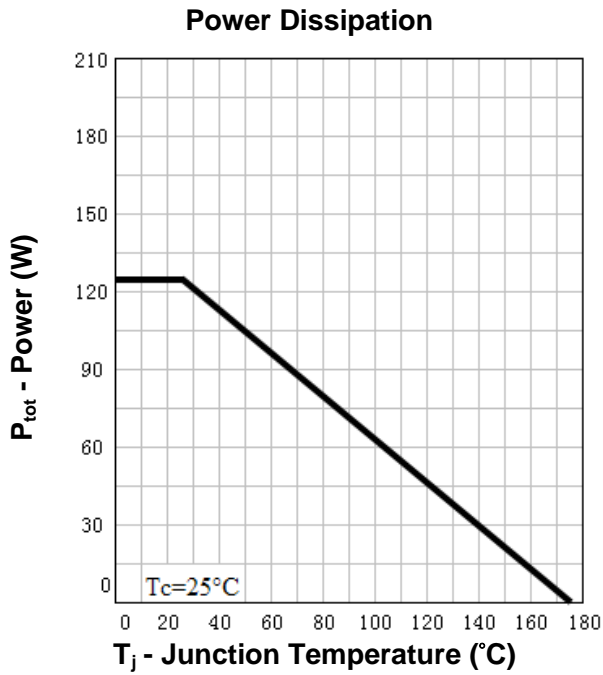
② Pulse width limited by safe operating area.

③ Limited by $T_{Jmax}, I_{AS}=32A, V_{DD}=48V, R_G=50\Omega$, Starting $T_J=25^\circ\text{C}$.

④ Pulse test; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

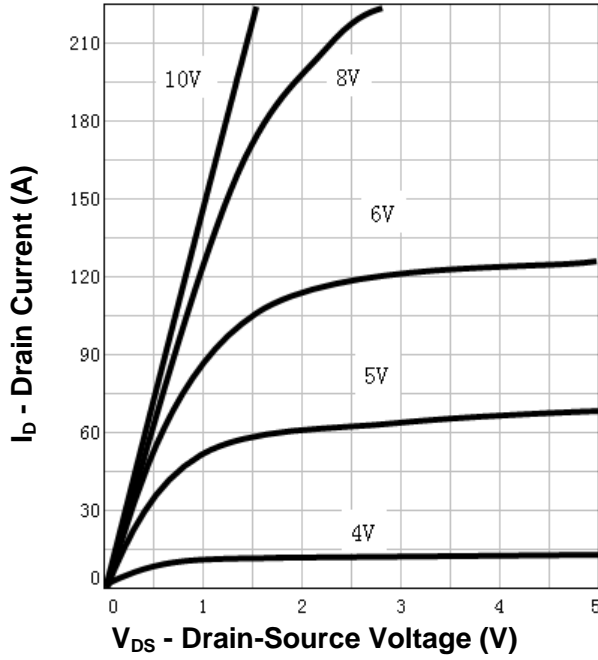
⑤ Guaranteed by design, not subject to production testing.

Typical Characteristics

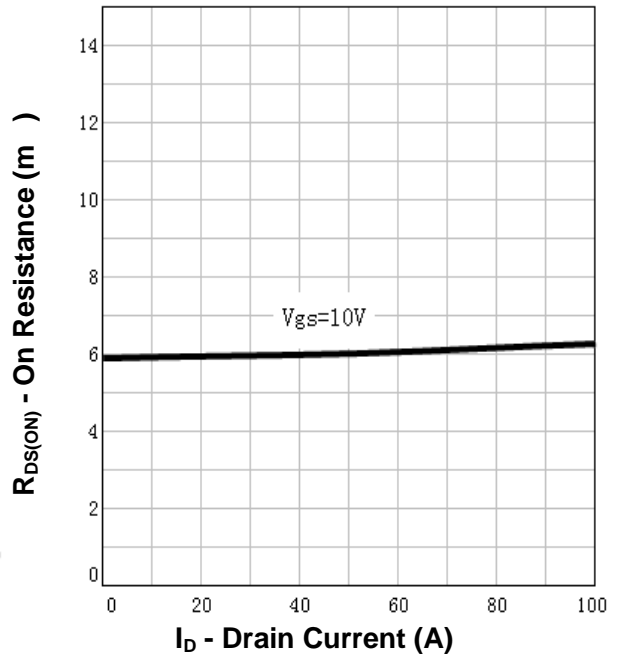


Typical Characteristics

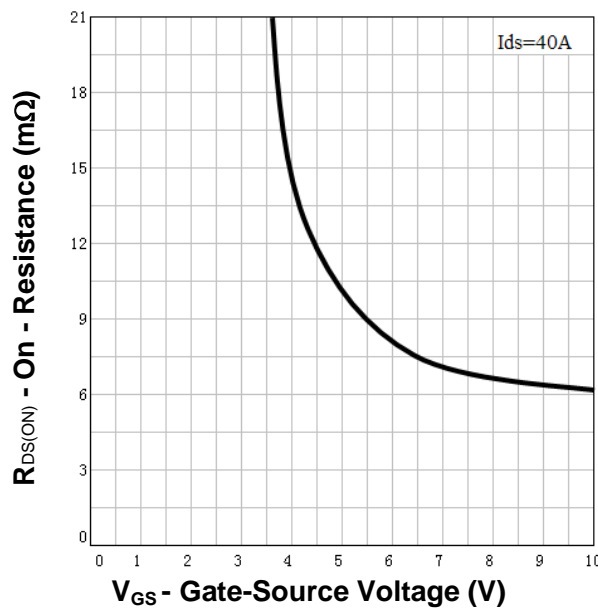
Output Characteristics



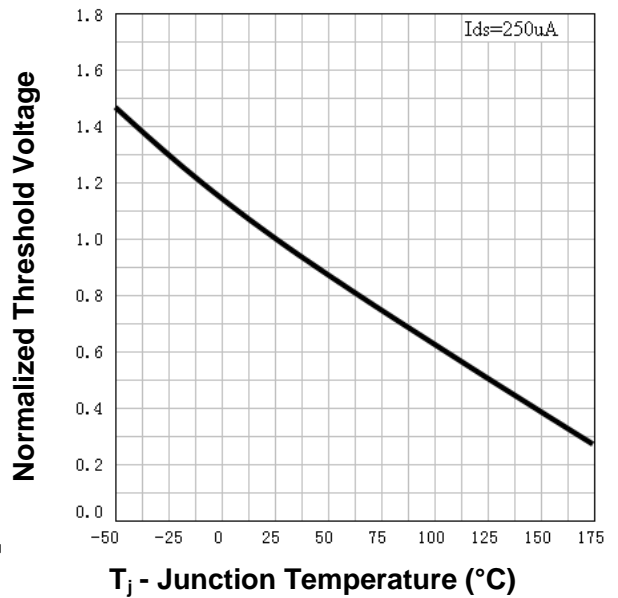
Drain-Source On Resistance



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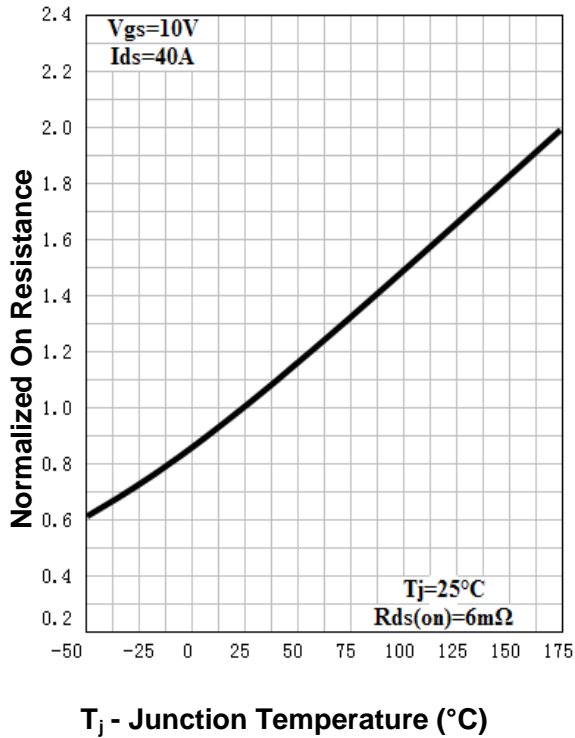


Gate Threshold Voltage

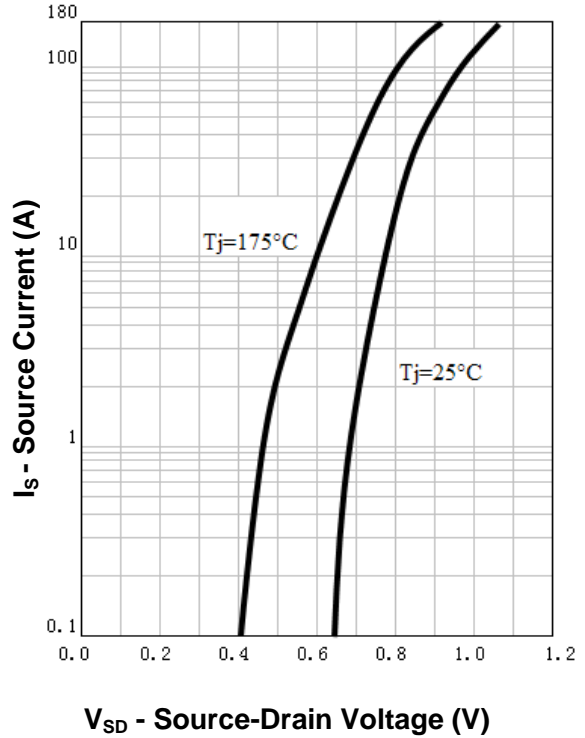


Typical Characteristics

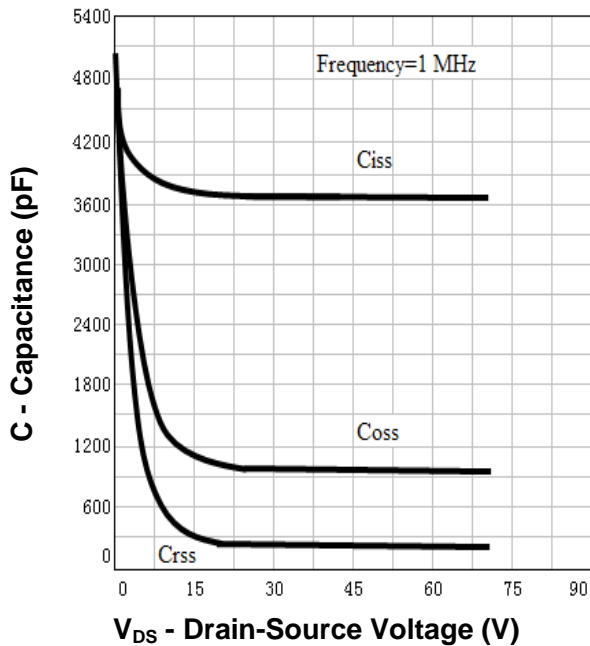
Drain-Source On Resistance



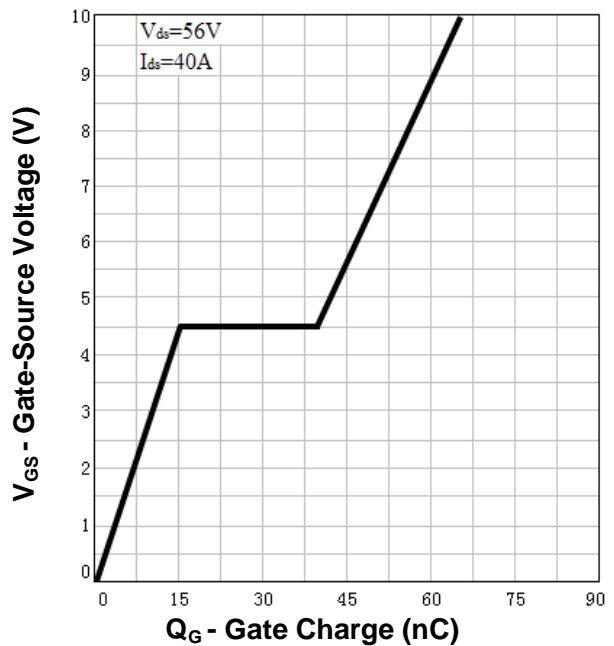
Source-Drain Diode Forward



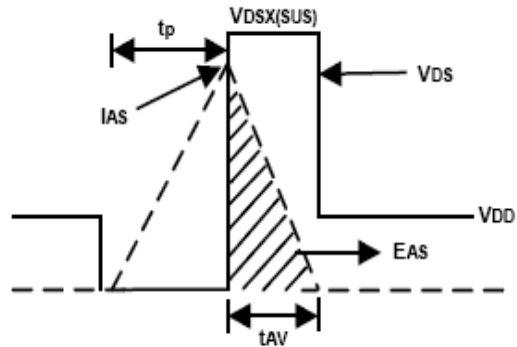
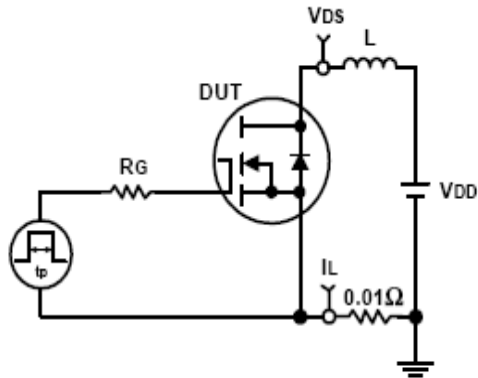
Capacitance



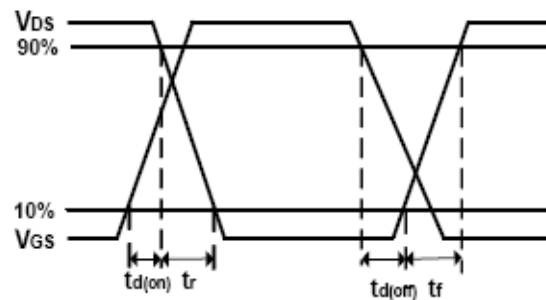
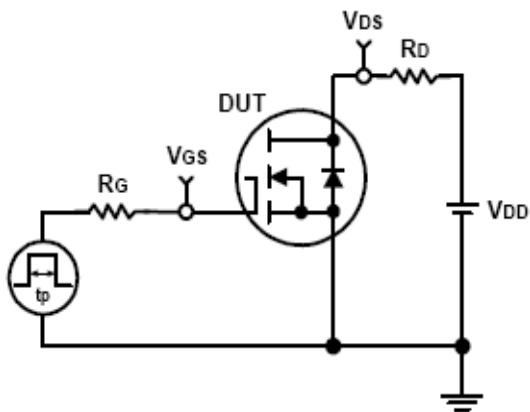
Gate Charge



Avalanche Test Circuit and Waveforms



Switching Time Test Circuit and Waveforms



Ordering and Marking Information

Device	Marking	Package	Packaging	Quantity	Reel Size	Tape width
RU7085R	RU7085R	TO-220	Tube	50	-	-

Package Information

TO-220FB-3L



SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185	$\phi p1$	1.40	1.50	1.60	0.055	0.059	0.063
A1	1.27	1.30	1.33	0.050	0.051	0.052	e	2.54BSC			0.1BSC		
A2	2.35	2.40	2.50	0.093	0.094	0.098	e1	5.08BSC			0.2BSC		
b	0.77	-	0.90	0.030	-	0.035	H1	6.40	6.50	6.60	0.252	0.256	0.260
b2	1.23	-	1.36	0.048	-	0.054	L	12.75	-	13.17	0.502	-	0.519
C	0.48	0.50	0.52	0.019	0.020	0.021	L1	-	-	3.95	-	-	0.156
D	15.40	15.60	15.80	0.606	0.614	0.622	L2	2.50REF.			0.098REF.		
D1	9.00	9.10	9.20	0.354	0.358	0.362	ϕp	3.57	3.60	3.63	0.141	0.142	0.143
DEP	0.05	0.10	0.20	0.002	0.004	0.008	Q	2.73	2.80	2.87	0.107	0.110	0.113
E	9.70	9.90	10.10	0.382	0.389	0.398	$\theta 1$	5°	7°	9°	5°	7°	9°
E1	-	8.70	-	-	0.343	-	$\theta 2$	1°	3°	5°	1°	3°	5°
E2	9.80	10.00	10.20	0.386	0.394	0.401							

ALL DIMENSIONS REFER TO JEDEC STANDARD
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS

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