MYSON TECHNOLOGY MTD655

5 Port 10M/100M Hub With 2 port Switch

FEATURES

- IEEE802.3 Clause 9 and IEEE802.3u Cluse 27 compliant.
- Provide 4 RMII (Reduced Media Independent Interface) ports and 1 MII port.
- Provide 2 inter_repeater stacking bus for 10M and 100M port expansion each.
- Support stacking to 4 units without any external arbitration logic (if use external arbitration logic, theoretically can stack to 6 units and up) .
- Build_in 2 port switch controller, support up to 2048 MAC addresses filtering database.
- Optional back_pressure flow control
- Optional up_link_switch port function (in slave hub), support 100FX 2km distance extension in 100FD mode.
- Meet Class_2 repeater specification for 100M_hub.
- Use simple and low cost asynchronous SRAM (high speed ASRAM 128k*8 : one pcs only)
- 128 pin PQFP package, 5V operation voltage.

GENERAL DESCRIPTION

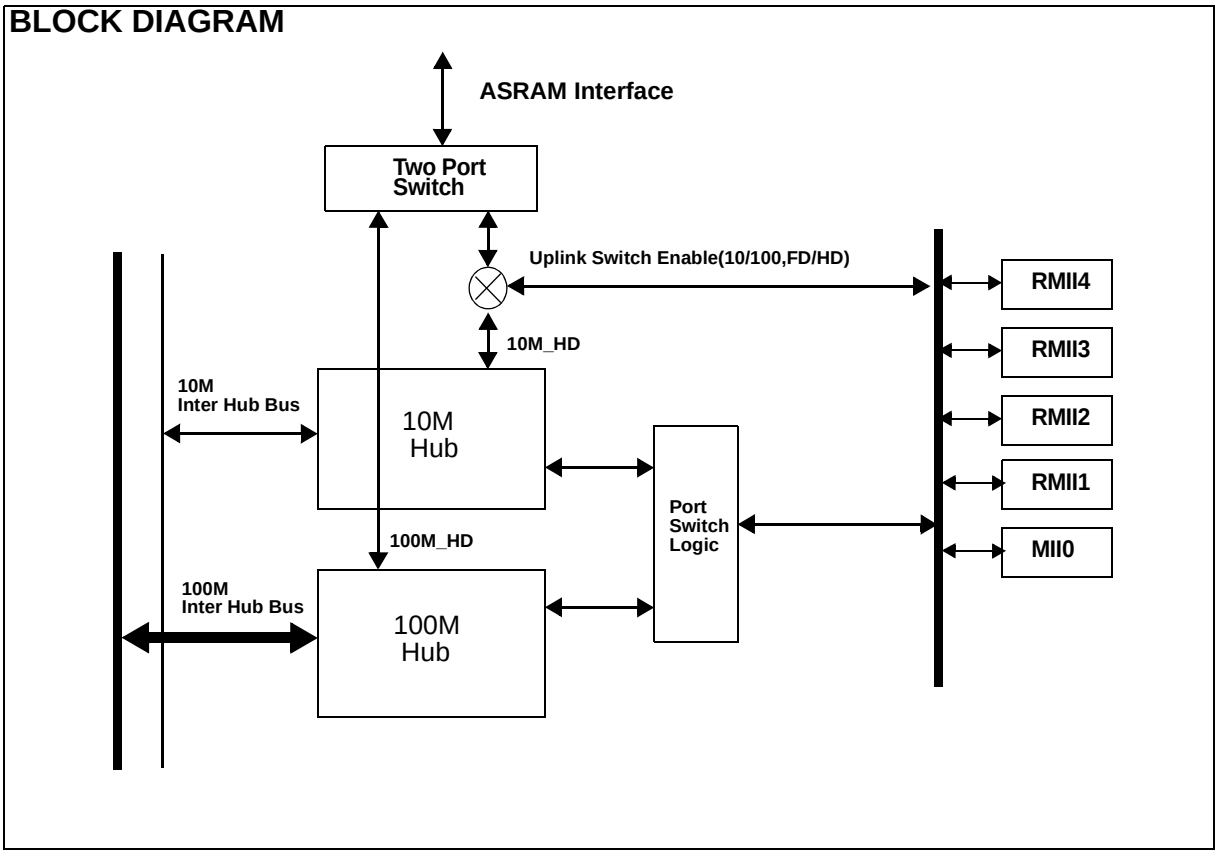
The MTD655 is a highly integrated, 10M/100M dual speed hub with build_in 2 port switch. Support 4 RMII ports and 1 MII port for 10M/100M operation, and meet 100M_hub class_2 spec when connect with external PHYceivers.

The MTD655 provides two Inter-repeater stacking bus for 10M and 100M expansion each, easily stack to 4 units without any external arbitration logic. If using external arbitration logic and proper bus driver, can stack to 6 units and up.

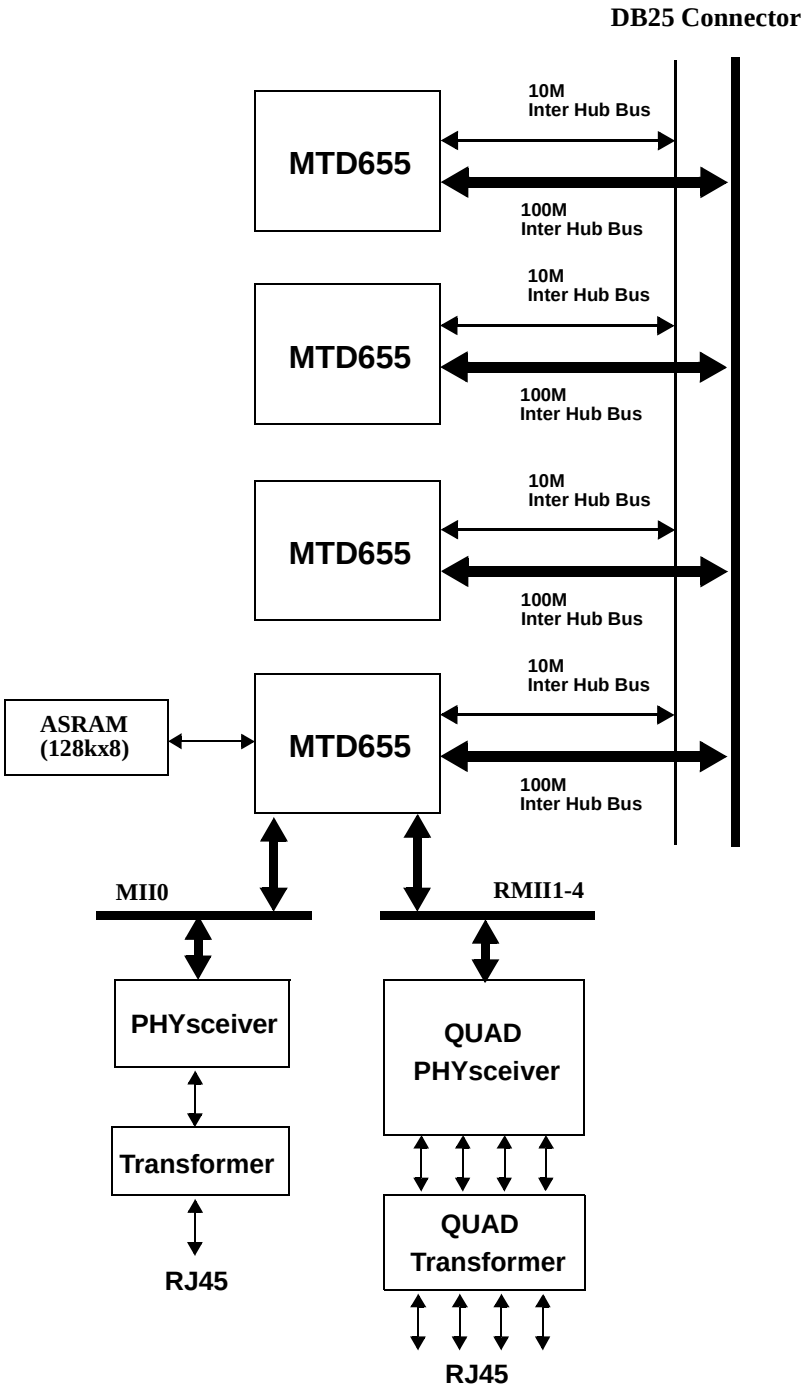
The build_in 2 port switch, support 2k MAC addresses filtering, and use low cost asynchronous high speed SRAM (128k*8) one pcs only for packet buffering. This 2 port switch can also be configured to be up_link switch when hub is under slave mode.

The MTD655 also support an simple and effective LED display function, provide 10M_col, 100M_col, memory_test_fail, and per port's partition status.

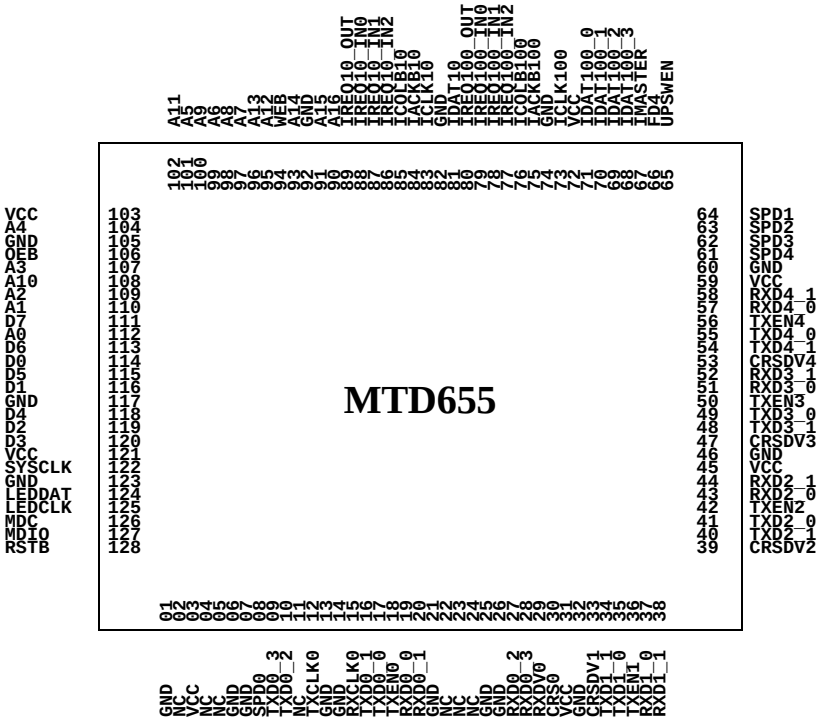
BLOCK DIAGRAM



SYSTEM DIAGRAM



1.0 PIN CONNECTION



1.0 PIN DESCRIPTIONS

MII Port Interface Pins (port0)			
Name	**Pin Number**	**I/O**	**Descriptions**
RXD0_0	19	I	Port0 MII receive data bit_0.
RXD0_1	20	I	Port0 MII receive data bit_1.
RXD0_2	27	I	Port0 MII receive data bit_2.
RXD0_3	28	I	Port0 MII receive data bit_3.
CRS0	30	I	Port0 MII asynchronous carrier indicator from PHY device.
RXDV0	29	I	Port0 MII synchronous receive data valid signal from PHY device.
RXCLK0	15	I	Port0 MII receive clock.
TXEN0	18	O	Port0 MII transmit enable signal.
TXD0_0	17	O	Port0 MII transmit data bit_0.
TXD0_1	16	O	Port0 MII transmit data bit_1.
TXD0_2	10	O	Port0 MII transmit data bit_2.
TXD0_3	9	O	Port0 MII transmit data bit_3.
TXCLK0	12	I	Port0 MII transmit clock.

RMII Port Interface Pins (port1 ~port4)			
Name	**Pin Number**	**I/O**	**Descriptions**
CRSDV1	33	I	Port1 RMII receive interface signal, CRSDV1 is asserted high when port1 media is non_idle.
RXD1_0	37	I	Port1 RMII receive data bit_0.
RXD1_1	38	I	Port1 RMII receive data bit_1.
TXEN1	36	O	Port1 RMII transmit enable signal.
TXD1_0	35	O	Port1 RMII transmit data bit_0.
TXD1_1	34	O	Port1 RMII transmit data bit_1.
CRSDV2	39	I	Port2 RMII receive interface signal, CRSDV2 is asserted high when port2 media is non_idle.
RXD2_0	43	I	Port2 RMII receive data bit_0.
RXD2_1	44	I	Port2 RMII receive data bit_1.
TXEN2	42	O	Port2 RMII transmit enable signal.
TXD2_0	41	O	Port2 RMII transmit data bit_0.
TXD2_1	40	O	Port2 RMII transmit data bit_1.
CRSDV3	47	I	Port3 RMII receive interface signal, CRSDV3 is asserted high when port3 media is non_idle.
RXD3_0	51	I	Port3 RMII receive data bit_0.
RXD3_1	52	I	Port3 RMII receive data bit_1.
TXEN3	50	O	Port3 RMII transmit enable signal.
TXD3_0	49	O	Port3 RMII transmit data bit_0.
TXD3_1	48	O	Port3 RMII transmit data bit_1.
CRSDV4	53	I	Port4 RMII receive interface signal, CRSDV4 is asserted high when port4 media is non_idle.

RMII Port Interface Pins (port1 ~port4)			
Name	**Pin Number**	**I/O**	**Descriptions**
RXD4_0	57	I	Port4 RMII receive data bit_0.
RXD4_1	58	I	Port4 RMII receive data bit_1.
TXEN4	56	O	Port4 RMII transmit enable signal.
TXD4_0	55	O	Port4 RMII transmit data bit_0.
TXD4_1	54	O	Port4 RMII transmit data bit_1.

High Speed Asynchronous SRAM Interface Pins			
Name	**Pin Number**	**I/O**	**Descriptions**
WEB	94	O	ASRAM control pin for write (low active).
OEB	106	O	ASRAM control pin for read (low active).
D[7:0]	111,113,115, 118,120,119, 116,114	I/O	ASRAM data bus
A[16:0]	90,91,93,96, 95,102,108, 100,98,97,99 ,101,104,107 ,109,110,112	O	ASRAM address bus

Note: Asynchronous SRAM acess time: 10/12 ns (max)

10M Inter-Bus Interface pins			
Name	**Pin Number**	**I/O**	**Descriptions**
IMASTER	67	I	Master hub selection: when high: means hub internal inter_bus arbiter is enabled and hub internal two_port switch is well conneted to 10M_hub core and 100M_hub core . when low: means hub internal inter_bus arbiter is disabled and hub internal two_port switch is not connected to 10M_hub core and 100M_hub core.
IACKB10	84	I/O	10M Inter-Bus port access acknowledge signal (low active). For master hub, this pin is output; for slave hub is input, or while EXT_ARB jumper was set to “1”, this pin is input from an external arbitration device.
ICOLB10	85	I/O	10M Inter-Bus collision signal (low active). For master hub, this pin can output multi hub collision event to inform all slave hub ; for slave hub, this pin is an input, or while EXT_ARB jumper was set to “1”, this pin is input from an external arbitration device.
IREQ10_IN0	88	I	10M Inter-Bus port access request input.
IREQ10_IN1	87	I	10M Inter-Bus port access request input.
IREQ10_IN2	86	I	10M Inter-Bus port access request input.
IREQ10_OUT	89	O	10M Inter-Bus port access request output.

10M Inter-Bus Interface pins			
Name	**Pin Number**	**I/O**	**Descriptions**
ICLK10	83	I/O	10M Inter-Bus port clock.
IDAT10	81	I/O	10M Inter-Bus port data bit
100M Inter-Bus Interface pins			
Name	**Pin Number**	**I/O**	**Descriptions**
IACKB100	75	I/O	100M Inter-Bus port access acknowledge signal (low active). For master hub, this pin is output; for slave hub is input, or while EXT_ARB jumper was set to "1", this pin is input from an external arbitration device.
ICOLB100	76	I/O	100M Inter-Bus collision signal (low active). For master hub, this pin can output multi hub collision event to inform all slave hub ; for slave hub, this pin is an input, or while EXT_ARB jumper was set to "1", this pin is input from an external arbitration device.
IREQ100_IN0	79	I	100M Inter-Bus port access request input.
IREQ100_IN1	78	I	100M Inter-Bus port access request input.
IREQ100_IN2	77	I	100M Inter-Bus port access request input.
IREQ100_OUT	80	O	100M Inter-Bus port access request output.
ICLK100	73	I/O	100M Inter-Bus port clock.
IDAT100_0	71	I/O	100M Inter-Bus port data bit 0.
IDAT100_1	70	I/O	100M Inter-Bus port data bit 1.
IDAT100_2	69	I/O	100M Inter-Bus port data bit 2.
IDAT100_3	68	I/O	100M Inter-Bus port data bit 3.

LED Interface Pins			
Name	**Pin Number**	**I/O**	**Descriptions**
LEDDAT	124	I/O	LED display serial data out; mapping for LEDCLK signal's burst clock , its serial out data sequence is : (first bit be shifted out is from b00, and end of burst bit is b23) b00: ********** b08: 10hub_col b16: ********** b01: ********** b09: 100hub_col b17: ********** b02: ********** b10: asram_test_fail b18: ********** b03: port0 partition b11: port0 partition b19: port0 rx_activity b04: port1 partition b12: port1 partition b20: port1 rx_activity b05: port2 partition b13: port2 partition b21: port2 rx_activity b06: port3 partition b14: port3 partition b22: port3 rx_activity b07: port4 partition b15: port4 partition b23: port4 rx_activity
LEDCLK	125	I/O	LED display clock signal, the signal is a discontinued clock for LED data serial shift out. Every clock burst have 24 cycles (period : 160 ns), and the clock burst will be repeated with every 42ms.

Miscellaneous Pins			
Name	**Pin Number**	**I/O**	**Descriptions**
RSTB	128	I	System reset input, low active.
SYSCLK	122	I	50MHz system clock input
MDC	126	I/O	MII management clock inout
MDIO	127	I/O	MII management data inout
UPSWEN	65	I	Up_link switch port enabling : one of internal two_port switch port will connect to 100M_hub domain, and another port will redirect to RMII port4.
FD4	66	I	When up_link switch port enabling, this pin is port4's full_deplex indicator, input from PHY. When hign , indicate port4 in running on full_duplex mode. When low, indicate on half_duplex mode.
SPD0	8	I	Port0 speed indicator, input from PHY. SPD0 input low: 100M , input high: 10M.
SPD1	64	I	Port1 speed indicator, input from PHY. SPD1 input low: 100M , input high: 10M.
SPD2	63	I	Port2 speed indicator, input from PHY. SPD2 input low: 100M , input high: 10M.
SPD3	62	I	Port3 speed indicator, input from PHY. SPD3 input low: 100M , input high: 10M.
SPD4	61	I	Port4 speed indicator, input from PHY. SPD4 input low: 100M , input high: 10M.
NC_pin	2,4,5,11,22, 23,24	NC	No connection pins
VCC	3,31,45,59, 72,103,121	PWR	Power pins
GND	1,6,7,13,14, 21,25,26,32, 46,60,74,82, 92,105,117, 123	GND	Ground pins

Power On Configuration Set Up Table			
Name	**Pin Number**	**I/O**	**Descriptions**
NC_11	11	I/O	Port0 MII interface enable : (power on external jumper configuration) - pin floating : Port0 MII interface disable (change to be RMII interface) , not suit for 5 ports daul speed hub application. - external pull_high: Port0 MII interface enable.
TXEN0	18	I/O	Back_pressure disable : (power on external jumper configuration) - external pull_low (default) : normal mode (back_pressure enbale) - external pull_high: back_pressure disable
TXEN2	42	I/O	Auto MII_setting bypass : (power on external jumper configuration) - external pull_low (default) : normal mode (auto MII_setting); after power_on, MTD655 will auto setup PHY devices be forced in half_ duplex mode for repeater apllication. - external pull_high: auto MII_setting bypass
MDC	126	I/O	1522 bytes packet accept enable : (power on external jumper configuration) - external pull_low (default) : normal mode (<=1518 bytes packet accept) - external pull_high: <= 1522 bytes packet accept
LEDCLK	125	I/O	Hub dealy enhance : (power on external jumper configuration) - external pull_low (default) : nomal hub propagation delay mode. - external pull_high: enhanced hub propagational delay mode, for covering long latency PHY devices).
LEDDAT	124	I/O	External arbiter enable : (power on external jumper configuration) - external pull_low (default) : normal mode (inter_repeater bus use internal arbiter) - external pull_high: inter_repeater bus use external arbiter .

2.0 MTD655 FUNCTIONAL DESCRIPTIONS

The MTD655 is conformed to IEEE802.3 chapter 9 and IEEE802.3u clause 27 specifications. The MTD655 provides 4 Redused MII interfaces, 1 MII interface and an embedded two port switch to construct a 10M/100M dual speed Hub application. Two Inter-Bus are also provided for stackable 10M/100M dual speed Hub application. The MTD655 functions are described as followmtd655s:

2.1 Repeat and data handling

4 independent RMII ports and 1 MII port integrated with IEEE802.3 chapter 9 and IEEE802.3u clause 27 repeater functions simultaneously. MTD655 embedded two Hub cores (10M and 100M) ,and each dedicated RMII or MII interface port can get per port's speed information from per port speed input pin, and then MTD655 will switch individual port to their appropriated Hub core functions (10M or 100M). The MTD655 receive packets from each RMII and MII ports, and redirect port's input packet to 10M or 100M Hub core according each port's speed. The internal IEEE802.3 chapter 9 or IEEE802.3u clause 27 repeater main state machine will starts to repeat the input packet to all ports except the input port. If larger than or equal to two ports have input packet simultaneously, this will be treated as a collision, and MTD655 will assert an arbitrary JAM pattern to all ports' output until collision event disappear and network is idle.

2.2 Partition

The MTD655 provides 10M/100M auto partition/reconnection functions to guarantee the network segment performance by means of dectecting a consecutive collisions. Each dedicated RMII or MII port has implement a individual 10M/100M auto partition/reconnection state machine. If port's consecutive collision number over or equal to CClimit (10M CClimit default is 32, 100M CClimit default is 64), this port will be partitioned. Reconnection will occurs after a larger than 512 bit time packet was received or transmitted from this partitioned port without any collision.
When port is under partition state, MTD655 will not accept any input messages from this port (just monitor input message), but will continue output repeated messages to this partition port.
Some new partition criterions are also implement, such as long_collision_partition event, jabber_partition event. In 10M/100M partition state machine, longer than 1024 bit time continueous collision will force port enter partition state. In 100M partition state machine, if port enter jabber_on state, this port will be partitioned. In 10M, jabber_partition function is not implemented.

2.3 Jabber

The jabber protect function is used to prevent an illegally long packet reception. After the MTD655 received a longer than 65536 +/- 6.25% bit times packet, this receive port's receive/transmit path will be inhibited until carrier is no longer detected.

2.4 MII Setting

Due to HUB is an half duplex device, the MTD655 need to force all connected phsical devices to work in half duplex environment. The MTD655 will setting all PHY's SMI register 4's half/full duplex bit during power on, and than restart auto-negotiation procedure to work in half duplex mode, and the PHY's device ID should be set by PCB maker from 5'h07 - 5'h0b(port0-4).

2.5 Inter-Bus Interface

Two Inter-Bus Interface are provided by the MTD655, One is 10M Inter-Bus Interface, the other is 100M Inter-Bus Interface. The Inter-Bus interface is designed for stackable hub application. For each domain, up to 4 MTD655s can be stacked through this Inter-Bus without any external arbitration logic. The Inter-Bus Interface includes IMASTER, IDATA (100M: use IDAT<3:0>, 10M: use only IDAT), REQOUT, REQIN0-2, ICLK, IACKB, ICOLB pins. IMASTER decide which MTD655 can arbitrate the Inter-Bus, and only one MTD655's IMASTER can be tie high in a stackable Hub. IDATA are synchronous with ICLK. The MTD655 output REQOUT to inform Inter-Bus Interface that it need the Inter-Bus right. When IACKB is asserted by Inter-Bus master after REQOUT asserted, the MTD655 which asserted REQOUT will get the bus right and put the transmit data into IDATA. If the MTD655 did not assert

REQOUT , but IACKB is asserted, means this MTD655 can get data from IDATA bus. When only one MTD655 output REQOUT to Inter-Bus Interface, IACKB will be asserted by Inter-Bus master device, If larger than two MTD655's REQOUT were asserted, Inter-Bus master will not assert IACKB , but will assert ICOLB to inform all the connected MTD655s.
The Inter-Bus interface can also be programmed to EXT_ARB mode, using LEDDAT pin's jumper setting. In this mode, Inter-Bus interface need an external arbitration logic to arbitrate Inter-Bus operation. And in this mode, the stackable capability is not limitted by the MTD655's REQIN pins number.

2.6 10M/100M packet Switch
The MTD655 inplements a 10/100M two port switch for 10M/100M packet switching. Total 2K address entrys are provided for packets' SA learning and DA routing; and alsoprovide automatic aging function (aging time = 300secs). The input packet from 10MHub (or 100M Hub) will be stored to external memory first, while packet is good for forward (CRC chech ok, 64Bytes < length > 1518Bytes, and not local packets) , than forward this packet to 100M Hub (or 10M Hub).

2.7 Uplink Switch Port
The MTD655 can config one switch port as an uplink switch port. When UPSWEN pin is high, and IMASTER pin is low, one of the intenal switch port is connect to 100M HUB, the other is connected to RMII port 4. In uplink switch mode, port 4 can work in 10M/100M(from SPD4 pin), half/full duplex(from FD4 pin) mode.

2.8 Memory Interface
The MTD655 use asynchronous SRAM as two port switchs' packet buffers, total has 128K byte external memory for packet buffering.

2.9 MII management
The MTD655 can be managed through MDC, MDIO pins. The MTD655 implements 3 MII registers for function control and status report (see Section 4.0 on page).
The management frame format is compliant to IEEE802.3u clause 22, and the device ID is fixed to 5'h1f internally.

2.10 LED display
The MTD655 implements three display modes, port RX activity, 10/100M domain collision, port partition. The LED data pin LEDDAT is high actived.
One strobe pin LEDCLK(24 burst clock/per 42ms) is used to latch serial LEDDAT information, and user can shift the latched data into byte aligned shift register to drive LEDs.

3.0 Registers
The MTD655 implements 3 MII registers, define as following tables:

TABLE 1. MII registers

REG NO	Bits	Name	R/W	Descriptions	Default
0		**CtlReg0**	**R/W**	**CONTROL REGISTER 0**	
	0			Reserved.	1'b0
	1	DisPar10		Set this bit will disable 10M hub core partition function.	1'b0
	2	DisPar100		Set this bit will disable 100M hub core partition function.	1'b0
	3	DisJab10		Set this bit will disable 10M hub core Jabber function.	1'b0
	4	DisJab100		Set this bit will disable 100M hub core Jabber function.	1'b0
	5-8			Reserved	4'b000
	9	CClimit100		Set "1" will program 100M partition cclimit to 128.	1'b0(64)

TABLE 1. MII registers

REG NO	Bits	Name	R/W	Descriptions	Default
	10	CClimit10		Set "1" will program 10M partition cclimit to 64.	1'b0(32)
	11-15			Reserved	2'b00
1		**CtlReg1**	**R/W**	**CONTROL REGISTER 1**	**16'h0000**
	0-7	DisPort		Set bits "1" disable port 0-7 RMII ports.	8'h000
	8-15			Reserved.	
2				**Reserved**	
3				**Reserved**	
4		**AgeReg**	**R/W**	**AGE REGISTER**	

"R/W" means read/writable.

4.0 Electrical Characteristics

4.1 Absolute Maximum Ratings

Symbol	Parameter	RATING	Unit
V_{CC}	Power Supply Voltage	-0.3 to 6.0	V
V_{IN}	Input Voltage	-0.3 to Vcc+0.3	V
V_{OUT}	Output Voltage	-0.3 to Vcc+0.3	V
T_{STG}	Storage Temperature	-55 to 150	^{o}C

4.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Commercial Power Supply Voltage	4.75	5	5.25	V
	Industrial Power Supply Voltage	4.5	5	5.5	V
V_{IN}	Input Voltage	0	-	Vcc	V
T_{OPR}	Commercial Junction Operating Temperature	0	25	115	^{o}C
	Industrial Junction Operating Temperature	-40	25	125	^{o}C

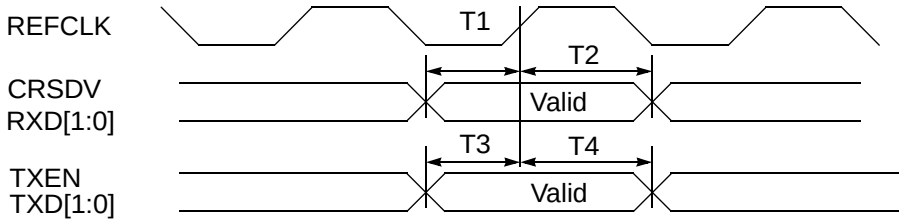
4.3 DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current	no pull-up or down	-1		1	uA
I_{OZ}	Tri-state Leakage Current		-10		10	uA
C_{IN}	Input Capacitance			3		pF
C_{OUT}	Output Capacitance			3		pF
C_{BID3}	Bi-direction buffer Capacitance			3		pF
V_{IL}	Input Low Voltage	CMOS			0.3*Vcc	V
V_{IH}	Input High Voltage	CMOS	0.7*Vcc			V
V_{OH}	Output High Voltage	I_{OL}=2,4,8,12,16,24mA			0.4	V
V_{OL}	Output Low Voltage	I_{OH}=2,4,8,12,16,24mA	3.5			V
R_I	Input Pull-up/down resistance	V_{IL}=0V or V_{IH}=V_{CC}		50		KOhm

(Under recommended operating conditions and Vcc = 4.75 ~ 5.25V, Tj = 0 to +115 ^{o}C)

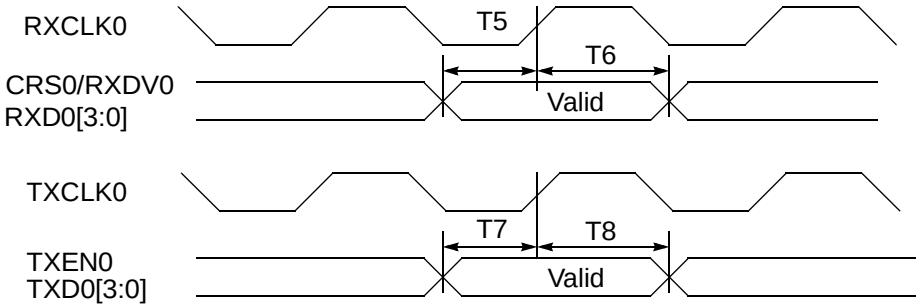
4.4 Electrical Characteristics

FIGURE 1. RMII timing



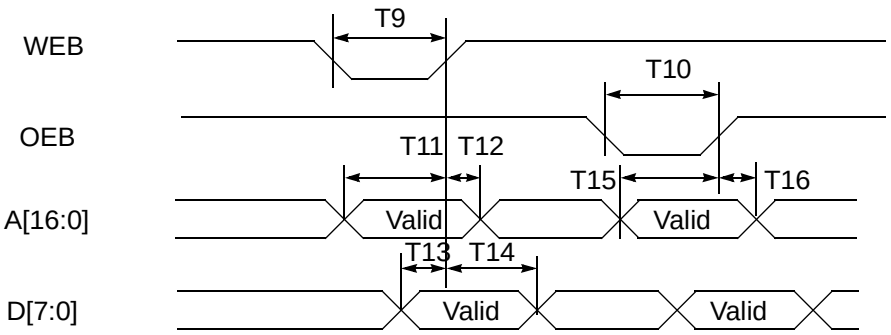
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T1	RMII input setup time	1			nS	
T2	RMII input hold time	1			nS	
T3	RMII output setup time	3			nS	
T4	RMII output hold time	5			nS	

FIGURE 2. MII timing



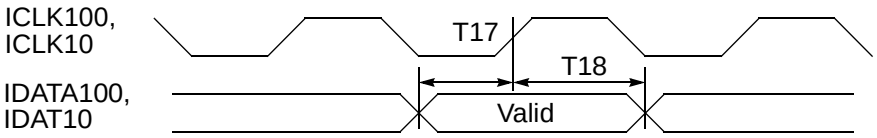
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T5	MII input setup time	10			nS	
T6	MII input hold time	10			nS	
T7	MII output setup time	3			nS	
T8	MII output hold time	5			nS	

FIGURE 3. Memory Interface Timing



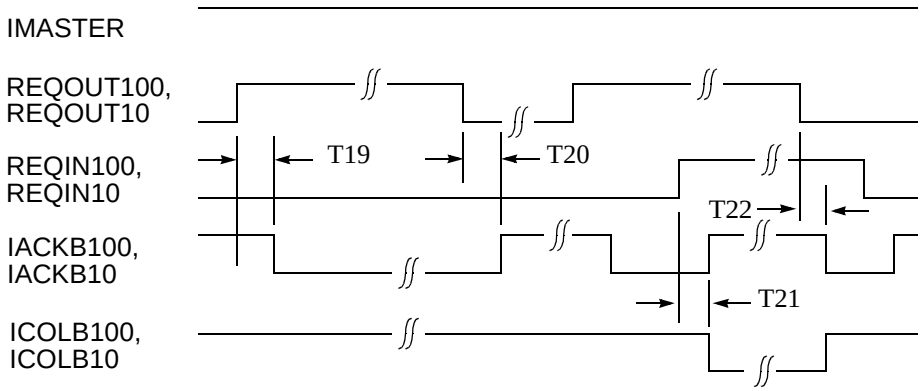
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T9	WEB pulse width	11.5		16	nS	
T10	OEB pulse width		20		nS	
T11	Write Address setup time	10		18.5	nS	
T12	Write Address hold time	1.5		7	nS	
T13	Write Data setup time	10		12	nS	
T14	Write Data hold time	1		4	nS	
T15	Read Address setup time		19.5		nS	
T16	Read Address hold time		0		nS	

FIGURE 4. Inter-Bus Interface timing I



Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T17	Inter-Bus output setup time(100M)	15		20	nS	
	Inter-Bus output setup time(10M)		50		nS	
T18	Inter-Bus output hold time(100M)	20		25	nS	
	Inter-Bus output hold time(10M)		50		nS	

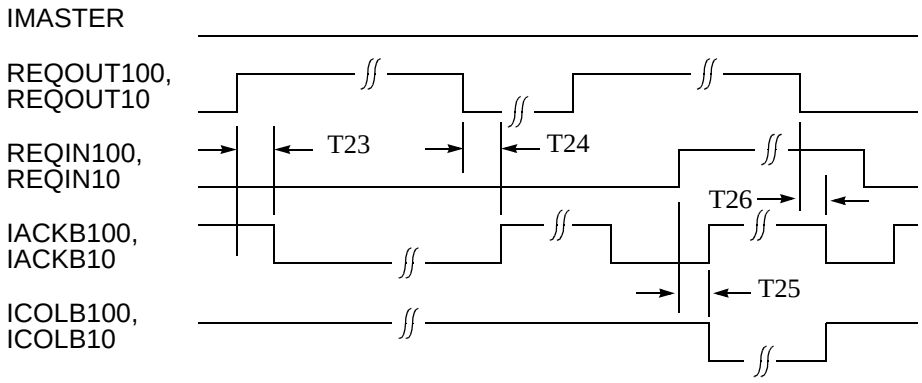
FIGURE 5. Inter-Bus Interface timing II



Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T19	Inter-Bus master REQOUT asserted to IACKB asserted propogation delay	7		20	nS	1
T20	Inter-Bus master REQOUT deas-serted to IACKB deasserted propo-gation delay	0	1	5	nS	1
T21	Inter-Bus master REQIN asserted to IACKB deasserted(ICOLB asserted) propogation delay(SOJ)	5		17	nS	1
T22	Inter-Bus master REQOUT deas-serted to IACKB asserted(ICOLBde-asserted) propogation delay(EOJ)	0	1	5	nS	1

Note 1 : In 10M/100M Inter-Bus interface, T19-T22 have the same value.

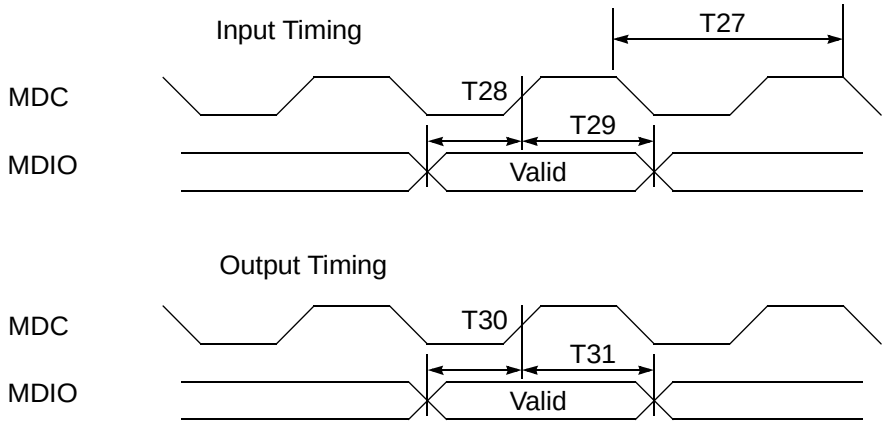
FIGURE 6. Inter-Bus Interface timing III



Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T23	Inter-Bus slave REQOUT asserted to IACKB asserted propogation delay	5		20	nS	2
T24	Inter-Bus slave REQOUT deasserted to IACKB deasserted propogation delay	5		20	nS	2
T25	Inter-Bus slave REQIN asserted to IACKB deasserted(ICOLB asserted) propogation delay(SOJ)	5		20	nS	2
T26	Inter-Bus slave REQOUT deasserted to IACKB asserted(ICOLBdeas-serted) propogation delay(EOJ)	5		20	nS	2

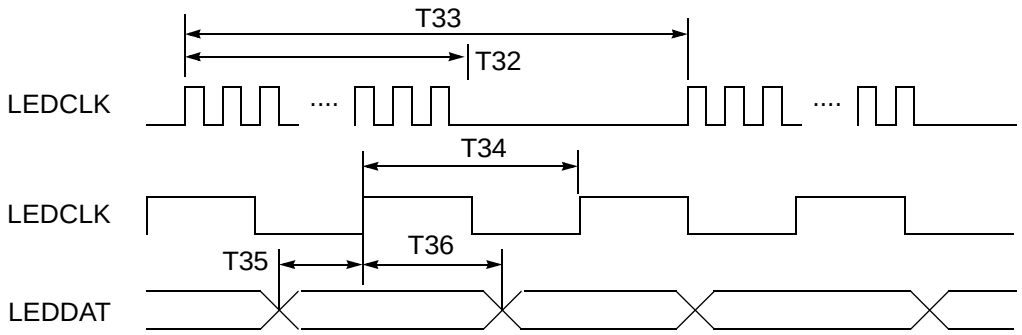
Note 2 : In 10M/100M Inter-Bus interface, T23-T26 have the same value.

FIGURE 7. MII Management timing



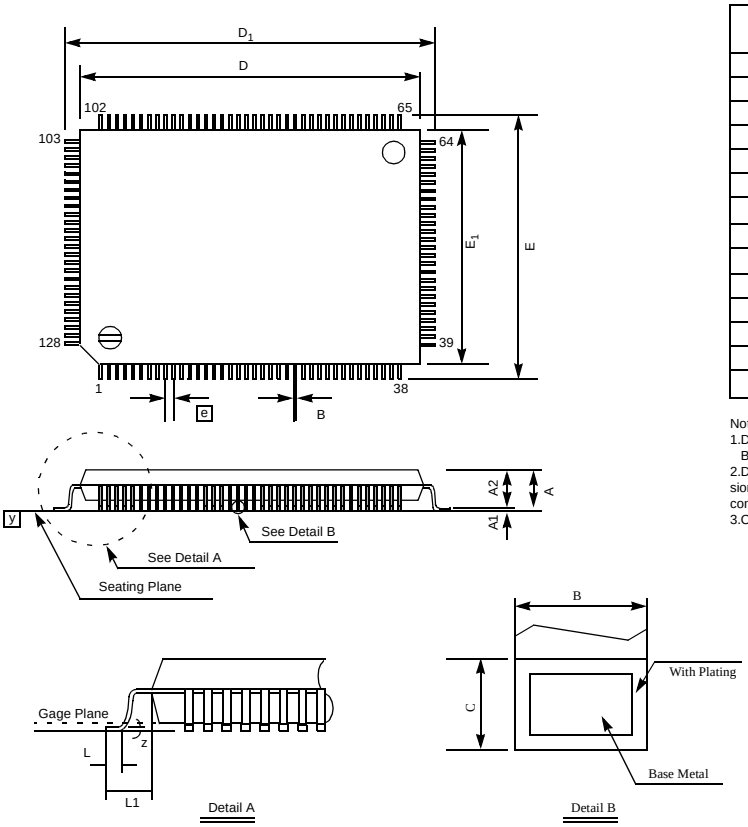
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T27	MDC clock cycle		400		nS	
T28	MDIO input setup time	10			nS	
T29	MDIO input hold time	10			nS	
T30	MDIO output setup time	182		194	nS	
T31	MDIO output hold time	206		218	nS	

FIGURE 8. LED output timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T32	24 LED burst clocks duration		3.84		uS	
T33	LED burst clock cycle time		42		mS	
T34	LED burst clock cycle		160		nS	
T35	LEDDAT to LEDCLK setup time		80		nS	
T36	LEDDAT to LEDCLK setup time		80		nS	

5.0 128 pin PQFP Package Data



Symbol	Dimension in inch			Dimension in mm		
	Min	Norm	Max	Min	Norm	Max
A	-	-	0.134	-	-	3.40
A1	0.010	-	-	0.25	-	-
A2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.50 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
z	0^o	-	7^o	0^o	-	7^o

Note:
1.Dimension D1 & E1 do not include mold protrusion.
But mold mismatch is included. Allowable protrusion is .25mm/.010" per side.
2.Dimension B does not include dambar protrusion. Allowable dambar protrusion .08mm/.003". Total in excess of the B dimemsion at maximum material condition. Dambar cannot be located on the lower radius or the foot.
3.Controlling dimension : Millimeter.