SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MK5025 SYNCHRONOUS TIMING

INTRODUCTION

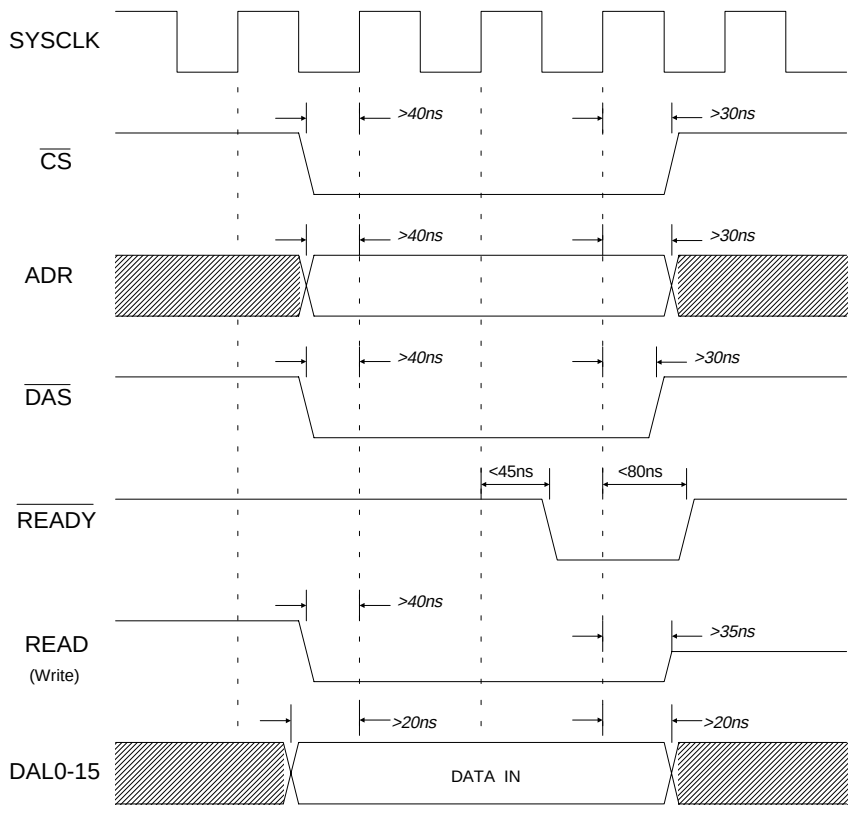
The SGS-Thomson MK5025 X.25 Link Level Controller is a VLSI device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. The MK5025 also supports X.32 (XID) and X.75 as well as single channel LAPD for ISDN with its UI frames and extended addressing capabilities.

PURPOSE

Although the MK5025 Data Sheet and Technical Manual provide detailed asynchronous timing diagrams that specifiy the relationships of the host interface signals to one another, the designer may often find it helpful to know how these timing values relate to the system clock. The purpose of this application brief is to provide a description of the MK5025 host interface as related to SYSCLK (MK5025 pin 28).

Because of the asynchronous nature of the use of this device, the MK5025 production testing is performed to ensure compliance with the asynchronous timing specifications stated in the Data Sheet and Technical Manual. It should be noted that although the synchronous timing diagrams in this document are provided to facilitate the design process, **the timing requirements in the Data Sheet must still be met to ensure proper operation.**

Figure 1: MK5025 Bus Slave Write Cycle



NOTES:

1. Input setup and hold times are in italics. These times are typical minimum values required to or from the particular edge specified in order to be recognized in that cycle.
2. Output delay times are the typical maximum delay from the specified edge to a valid output.

SYNCHRONOUS TIMING

The synchronous timing data contained within this document was derived from a sample of MK5025 devices and guard-banded to allow for process variations. Although these values are not guaranteed or tested in the manufacturing process, the typical MK5025 device performance should meet or exceed these timing values.

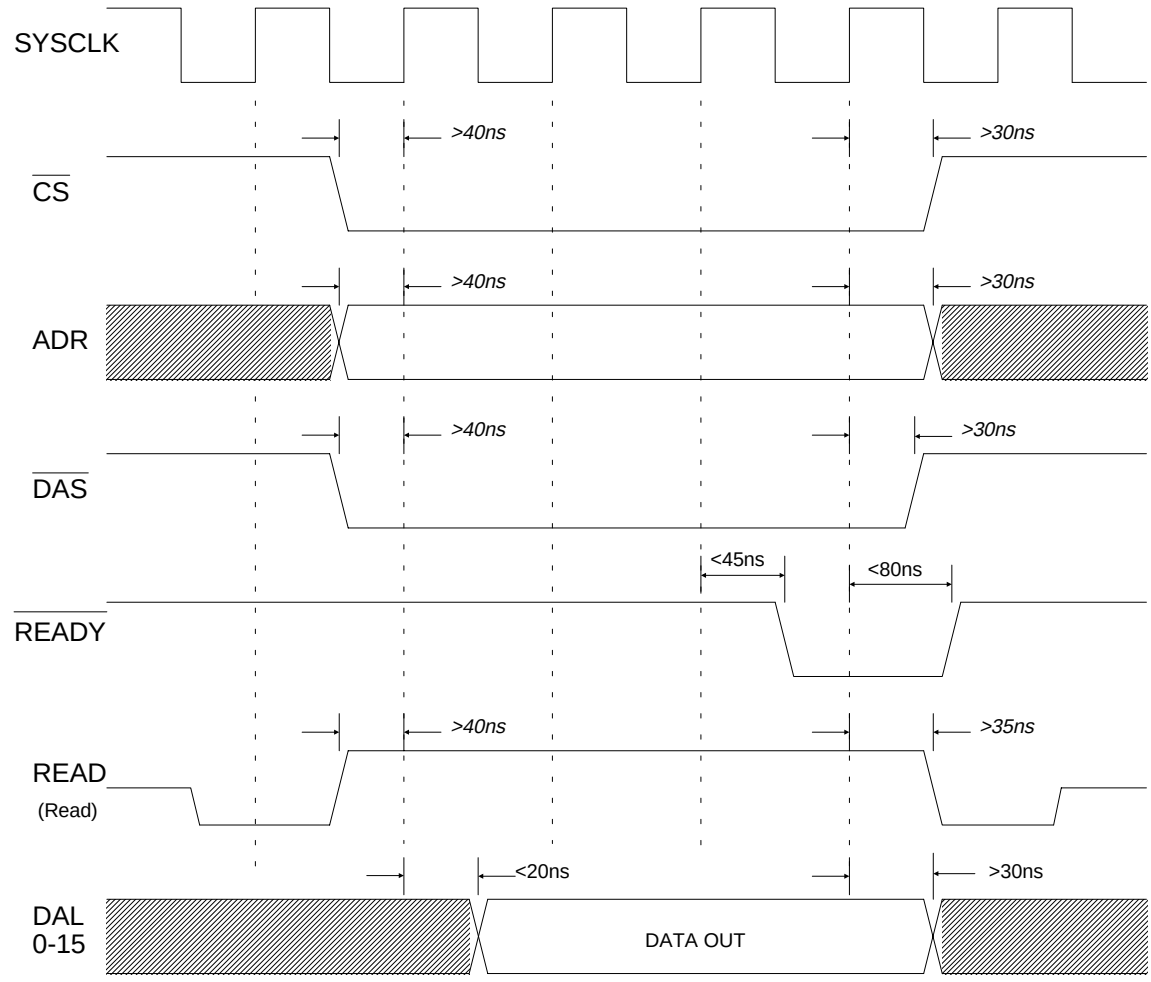
Figures 1 and 2 provide the typical timing relationships, with respect to SYSCLK, for the MK5025 operating as a bus slave. Figures 3 and 4 provide the typical timing relationships, with respect to SYSCLK, for the MK5025 operating as a bus master.

The input setup and hold times given in this document are typical minimum values required to or from the SYSCLK edge indicated in order to be recognized within that SYSCLK cycle. The output delay times are the typical maximum delay from the indicated edge to a valid output state.

CONCLUSION

The MK5025 offers great flexibility to the data communications system designer. The on-chip protocol processing may be used to save the designer much time in implementing standard protocols such as X.25, LAPB, ISDN LAPD, X.32, and X.75, and these synchronous timing diagrams are provided to further facilitate the design process.

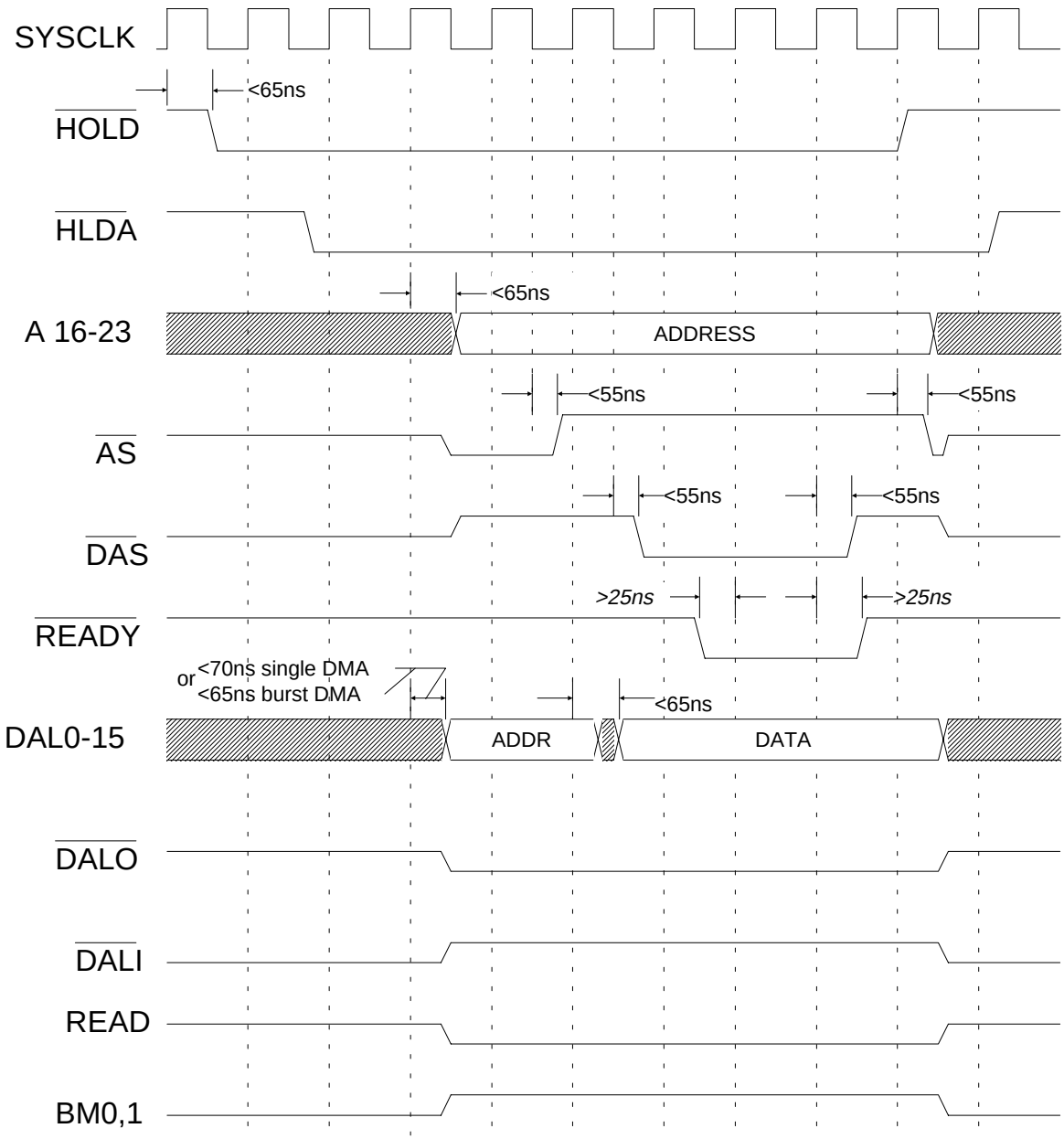
Figure 2: MK5025 Bus Slave Read Cycle



NOTES:

1. Input setup and hold times are in italics. These times are typical minimum values required to or from the particular edge specified in order to be recognized in that cycle.
2. Output delay times are the typical maximum delay from the specified edge to a valid output.

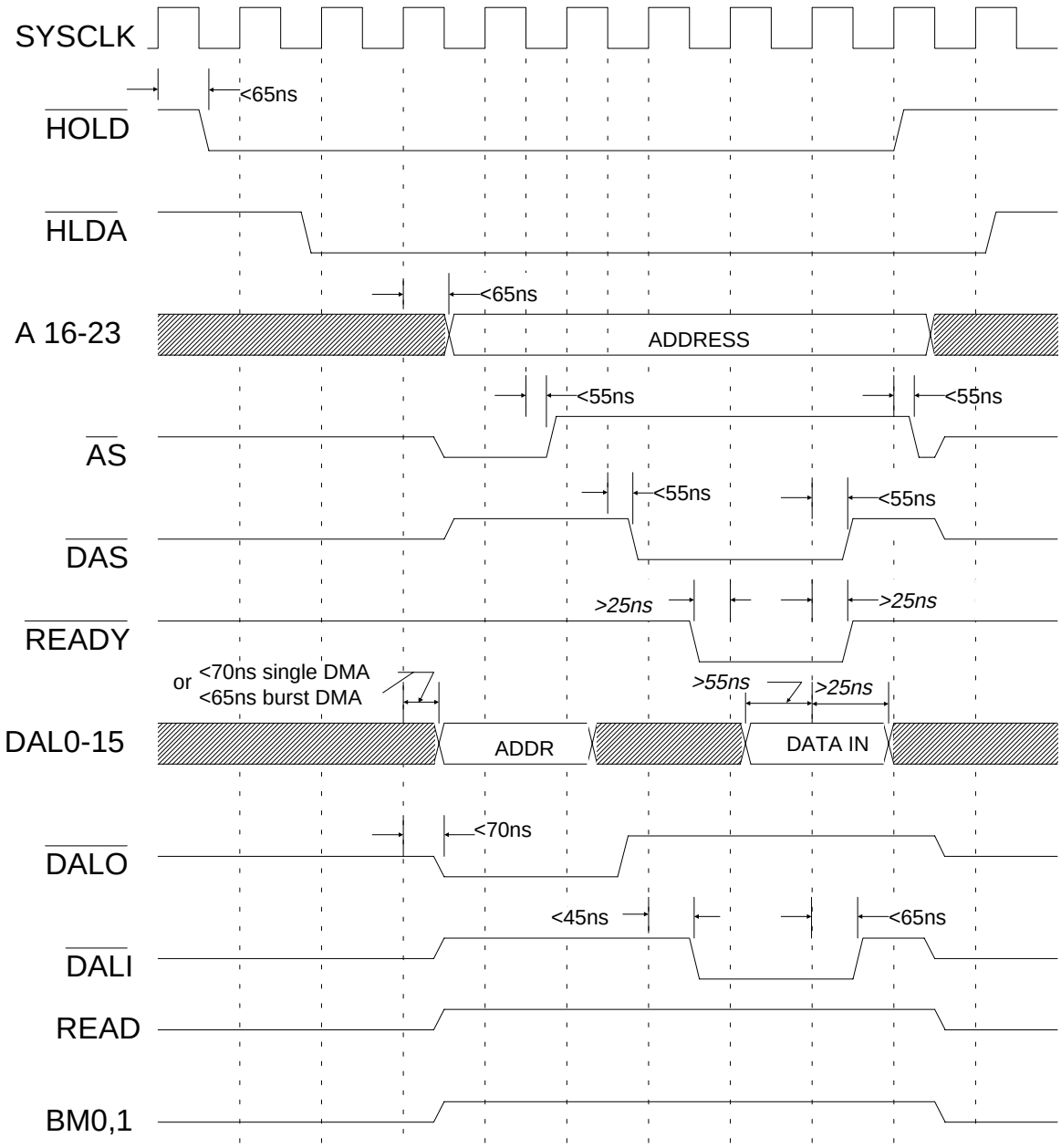
Figure 3: MK5025 Bus Master Write Cycle



NOTES:

1. The typical MK5025 device performance should meet or exceed the typical timing values given above. Asynchronous timing requirements given in the Technical Manual still apply.
2. Input setup and hold times are in italics. These times are typical minimum values required to or from the particular edge specified in order to be recognized in that cycle.
3. Output delay times are the typical maximum delay from the specified edge to a valid output.

Figure 4: MK5025 Bus Master Read Cycle



NOTES:

1. The typical MK5025 device performance should meet or exceed the typical timing values given above. Asynchronous timing requirements given in the Technical Manual still apply.
2. Input setup and hold times are in italics. These times are typical minimum values required to or from the particular edge specified in order to be recognized in that cycle.
3. Output delay times are the typical maximum delay from the specifed edge to a valid output.