# AN4248
# Application note

## 60 W PSU design details for water purifier system

**Harjeet Singh**

## Introduction

This power supply is based on quasi-resonant mode of operation using ST multi-mode controller L6566B. The L6566B is an extremely versatile current-mode primary controller IC, specifically designed for high-performance offline flyback converters. Both fixed-frequency (FF) and quasi-resonant (QR) operation are supported. The user can pick either of the two, depending on application needs.

The device features an externally programmable oscillator: it defines the converter's switching frequency in FF mode and the maximum allowed switching frequency in QR mode. When FF operation is selected, the IC works like a standard current-mode controller with a maximum duty cycle limited at 70% min. The oscillator frequency can be modulated to mitigate EMI emissions. QR operation, when selected, occurs at heavy load and is achieved through a transformer demagnetization sensing input that triggers MOSFET turn-on. Under some conditions, ZVS (zero-voltage switching) can be achieved. The converter's power capability increasing with the mains voltage is compensated by line voltage feed-forward. At medium and light load, as the QR operating frequency equals the oscillator frequency, a function (valley skipping) is activated to prevent further frequency rise and keep the operation as close to ZVS as possible. With either FF or QR operation, at very light load the IC enters a controlled burst-mode operation, to help keep consumption from the mains low and meet energy saving recommendations.

The protection functions included in this device are: not-latched input undervoltage (brownout), output OVP (auto-restart or latch-mode selectable), a first-level OCP with delayed shutdown to protect the system during overload or short-circuit conditions (auto restart or latch-mode selectable) and a second-level OCP that is invoked when the transformer saturates or the secondary diode fails short. A dedicated pin to latch the controller in any abnormal condition is also provided.

The main features of the controller are listed here:

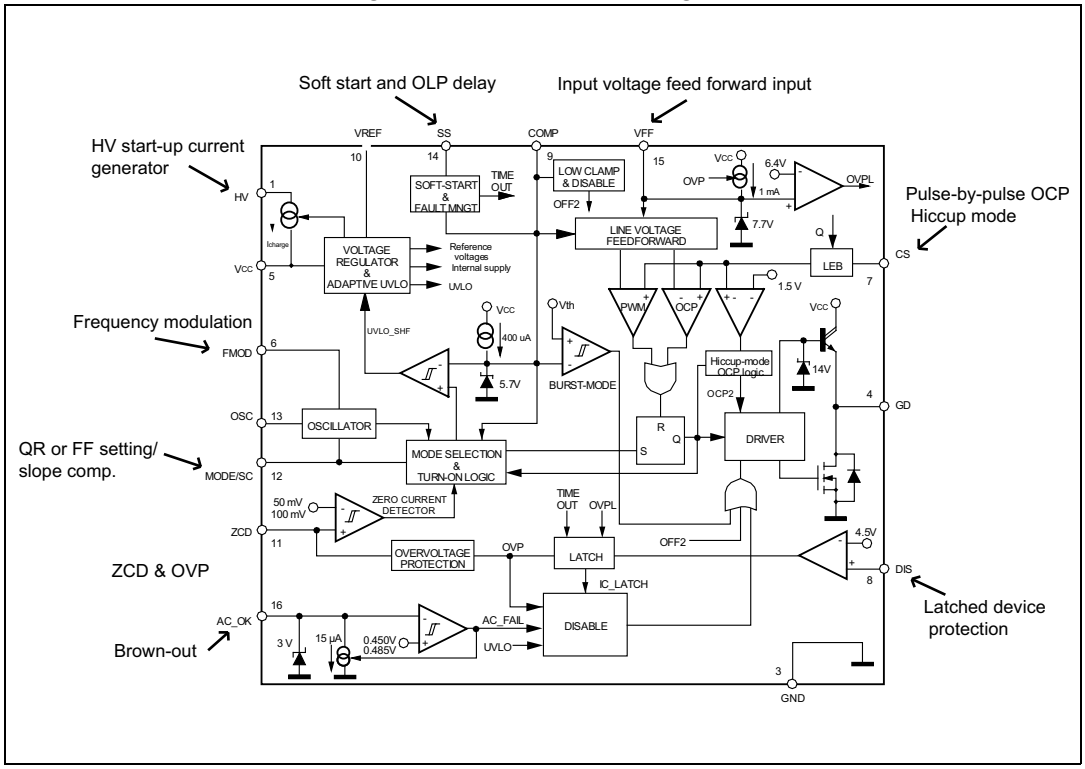
- Selectable multi-mode operation: fixed frequency or quasi-resonant
- On-board 700 V high-voltage startup
- Advanced light load management
- Low quiescent current (< 3 mA)
- Adaptive UVLO
- Line feed-forward for constant power capability vs. mains voltage
- Pulse-by-pulse OCP, shutdown on overload (latched or auto restart)
- Transformer saturation detection
- Programmable frequency modulation for EMI reduction
- Latched or auto restart OVP
- Brownout protection

# Contents

# List of figures

# 1 Block diagram

**Figure 1. L6566B block diagram**



# 2 Electrical specifications

**Table 1. Electrical Specifications**

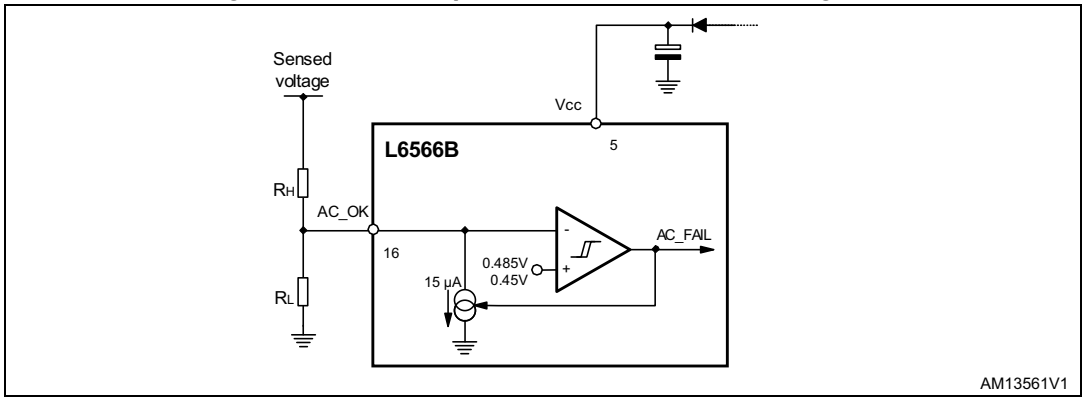
| Parameters | Limits |
|---|---|
| Min operating voltage, $V_{acmin}$ | 90 $V_{ac}$ |
| Max operating voltage, $V_{acmax}$ | 265 $V_{ac}$ |
| Mains overvoltage detection | Overvoltage shutdown above 300 $V_{ac}$ |
| | Converter should withstand 440 $V_{ac}$ |
| Mains frequency, fL | 50 Hz+/-3 Hz |
| Input / output isolation | Yes, galvanic isolation, > 2.7 $_K$V |
| Nominal output voltage, $V_{out}$ | 24 V+/-0.2 V |
| Total output power, $P_{out}$ | 60 W |
| Typical efficiency at 230 $V_{ac}$ | > 85% |
| Output voltage pk-pk ripple | < 150 mV |
| Protection features | Mains brownout protection-auto restart |
| | Mains overvoltage protection-auto restart/latched |
| | Overload and short-circuit protection-auto restart |
| | Output overvoltage protection-auto restart/latched |
| | Over temperature shutdown-latched |
| Topology | Q-resonant flyback converter |
| Reflected voltage of transformer (VR) | 140 V |
| Max ambient temperature | 45° C |
| Enclosure type | Open |

# 3 AC_OK setting for brownout

This pin is used for brownout function when the mains voltage goes below minimum operating level. This is not a latched shutdown. The purpose of this protection feature is to prevent any overheating at the primary side due to brownout condition. A voltage below 0.45 V shuts down (not latched) the IC, lowers its consumption and clears the latch set by latched protections. The IC's operation is re-enabled as the voltage exceeds 0.45 V. The protection is done by using a simple resistor divider network RH and RL. By setting AC_OK pin voltage at 0.45 V with proper selection of divider resistor at < 90 $V_{ac}$, we can make the controller shut down at desired mains undervoltage level.

The brownout comparator is provided with current hysteresis in addition to voltage hysteresis: an internal 15 µA current sink is ON as long as the voltage applied on the AC_OK pin is such that the AC_FAIL signal is high.

**Figure 2. Brownout protection: internal block diagram**




The following relationships can be established for the ON ($Vsen_{ON}$) and OFF ($Vsen_{OFF}$) thresholds of the sensed voltage:

**Equation 1**

$$\frac{Vsen_{ON} - 0.485}{R_H} = 15 \cdot 10^{-6} + \frac{0.485}{R_L} \qquad \frac{Vsen_{OFF} - 0.45}{R_H} = \frac{0.45}{R_L}$$

From the above relations, we derive the upper resistor and lower resistor values of the divider network as below:

**Equation 2**

$$R_H = \frac{Vsen_{ON} - 1.078 \cdot Vsen_{OFF}}{15 \cdot 10^{-6}} \qquad R_L = R_H \frac{0.45}{Vsen_{OFF} - 0.45}$$

After calculating, referring to the schematic we have following values :

R4 = R9 = R13 = 330 K, R21 = 5.1 K and R22 = 510E approximately.

# 4 Mains feed-forward setting

The VFF pin is used to feed the controller the input voltage information and accordingly the internal current sense threshold is decided. The purpose of feed-forward input is to maintain the constant input power of converter throughout the wide mains variation and fixes the output overload current threshold constant throughout the wide mains variations.

The linear dynamics of the pin ranges from 0 to 3 V. A voltage higher than 3 V makes the IC stop switching. If VFF function is not desired, tie the pin to GND (pin 3) directly if a latch-mode output OVP is not required (see pin 11, ZCD) or through a 10 k min resistor if a latch-mode OVP is required. Bypass the pin with a capacitor to GND (pin 3) to reduce noise pick-up. The following figure shows the internal circuit of the controller for feed-forward function and the variation of current sense threshold (Vcsx) versus mains voltage variations (VFF signal).

**Figure 3. L6566B mains feed-forward section**

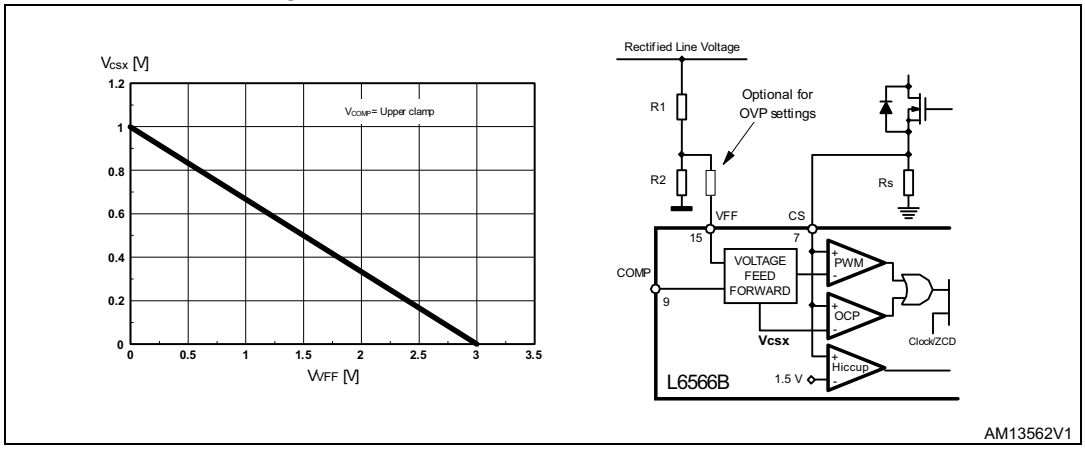
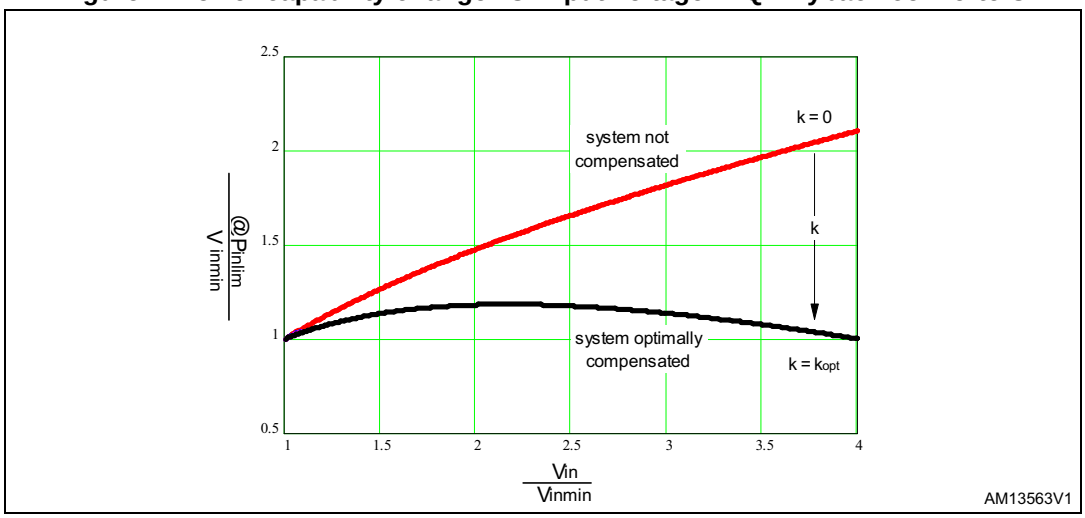



**Figure 4. Power capability change vs. input voltage in QR flyback converters**




The optimum value of k, $k_{opt}$, which minimizes the power capability variations over the input voltage range, is the one that provides equal power capability at the extremes of the range. The approximation of this parameter is:

**Equation 3**

$$k_{opt} = 3 \cdot \frac{V_R}{V_{inmin} \cdot V_{inmax} + (V_{inmin} + V_{inmax}) \cdot V_R}$$

Where $V_{inmin}$ and $V_{inmax}$ is the rectified DC voltage at minimum and maximum mains voltage. $V_R$ is the reflected voltage. The parameter $K_{opt}$ is used to calculate the resistor divider values connected to VFF pin (RVFF_H and RVFF_L), Which gives the following values, referring to the schematic (normally same resistor divider network of AC_OK pin can also be used by splitting RVFF_L into two values):

We have RVFF = 1M, RVFF_L = 510 E;

R4 = R9 = R13 = 330 K, R21 = 5.1 K and R22 = 510E approximately.

Accordingly, we can calculate the sense resistor value connected at the MOSFET source as per the equations below:

**Equation 4**

$$Rs = \frac{1 - \frac{k_{opt}}{3} V_{inmin}}{I_{PKpmax}}$$

Where Ipkpmax is the peak drain current at $V_{acmin}$.

We have following parameters in our design:

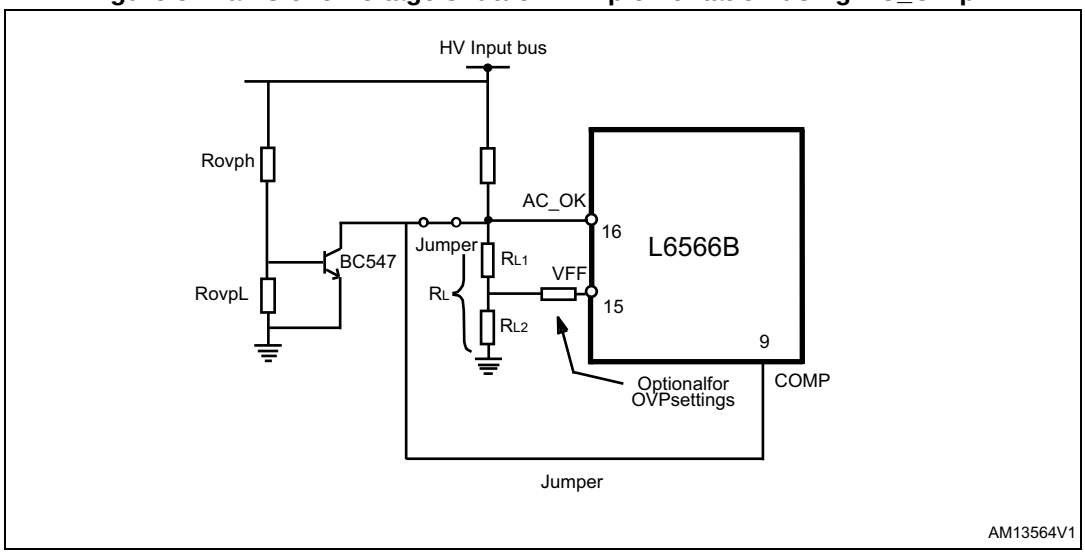
- $V_{inmin}$ = 90√2 = 127 V
- $V_{inmax}$ = 265√2= 375 V
- $I_{pkp}$ = 2.2 A
- $V_R$ = 140 V

Which gives: $k_{opt}$ = 0.0035 and hence Rs = 0.39 Ω. In the schematic R35 = R36 = R29 = 1.2E, R30 = 10E.

# 5 Mains overvoltage shutdown

This feature is important to integrate in the SMPS where supply variations are quite large and to avoid any damage to the converter ensure that the converter stops working when the line voltage goes beyond a certain level. This can be achieved by using various pins, such as the AC_OK , DIS OR COMP pins. In this design, we are implementing the circuit with the AC_OK /COMP pin to retain the option of either auto restart or latched shutdown is desired. The user can choose to use the corresponding jumper in the circuit.

**Figure 5. Mains overvoltage shutdown implementation using AC_OK pin**




Referring to the above circuit, with a simple bipolar BC547 and resistor divider network, we can generate an inhibit signal to active mains OVP protection:

$V_{be\_sat}$= 0.6-0.7 V, taking typical value of 0.65 V

we have

- $V_{mains\_OVP}$=300 $V_{ac}$, means 300 √2= 424 Vdc
- With $R_{ovpH}$= 1M, $R_{ovp}$=1.5 K

Referring to the schematic, we have

- R3 = R8 = R12 = 330 K, R16 = 1.5 K

# 6 Overload delay and shutdown

The Soft start (SS) pin is responsible for providing the soft start during startup as well as delayed shutdown during overload period. This is important for some types of loads which require inrush current for a certain duration like printer load. In this design, the appropriate value 100 nF is connected at the SS pin. The time to charge capacitor C17 from 0 V to 2 V sets the soft start time during startup. The time taken is approximated as follows:

**Equation 5**

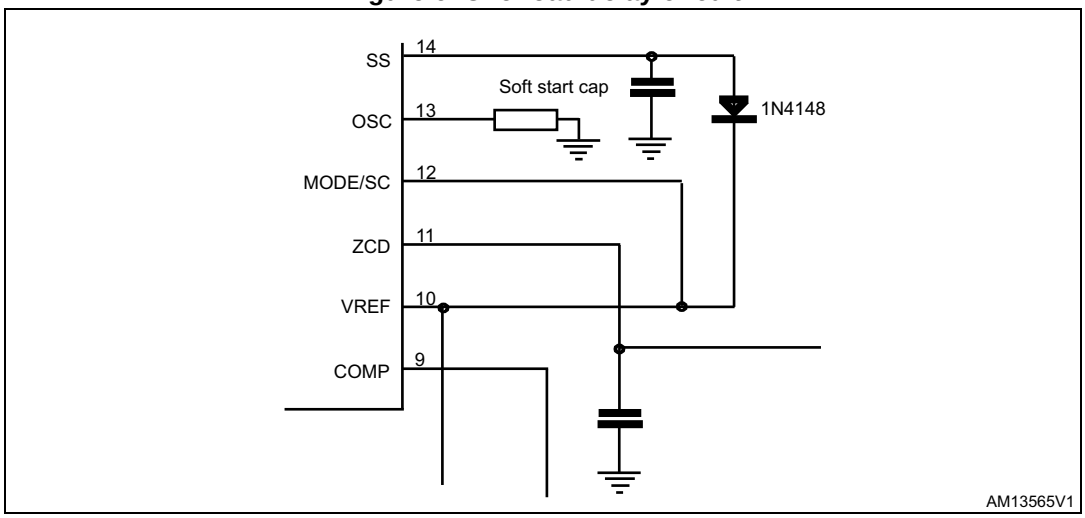
$$T_{SS} = \frac{Css}{I_{SS1}} V_{csx}(V_{VFF}) = \frac{Css}{I_{SS1}}\left(1 - \frac{V_{VFF}}{3}\right)$$

Where $I_{ss1}$ is the current sourced by the internal current generator.

In case of overload at output, the capacitor voltage rises above 2 V and when the capacitor voltage reaches 5 V, the device shuts down. But during this time the soft start capacitor is charged with internal current generator at a current of $I_{SS2} = I_{SS1} / 4$. So this amount of time is allowed for overload duration.

As the voltage at the soft start capacitor continuous to increase in case of overload and reaches 6.4 V, the device will be latched. To avoid this condition, we normally connect the SS pin to Vref via a diode, so that in any case the device voltage is clamped to 5 V+Vbe drop = 5.7 V. This is shown in the figure below:

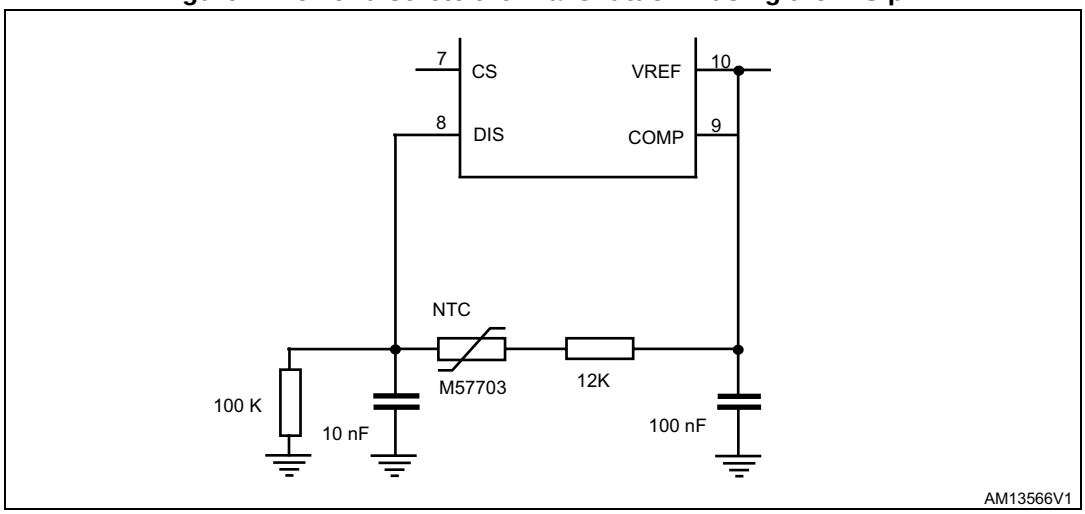
**Figure 6. Overload delay circuit**



# 7 Overtemperature shutdown

It is very simple to achieve overtemperature shutdown using the DIS pin. This protection is latched disabled. We need to recycle the $V_{CC}$ voltage to restart the device. A simple circuit using NTC, which is mounted on the MOSFET/rectifier heat sink can be used as shown below. During normal temperature conditions, the voltage at the DIS pin is set lower than 4.5 V. As the temperature of the power device increases, NTC resistance falls and voltage at the DIS pin starts increasing. As the voltage reaches at 4.5 V, the device gets shut down and latched.

**Figure 7. Power discrete thermal shutdown using the DIS pin**



# 8 Output overvoltage protection (ZCD setting)

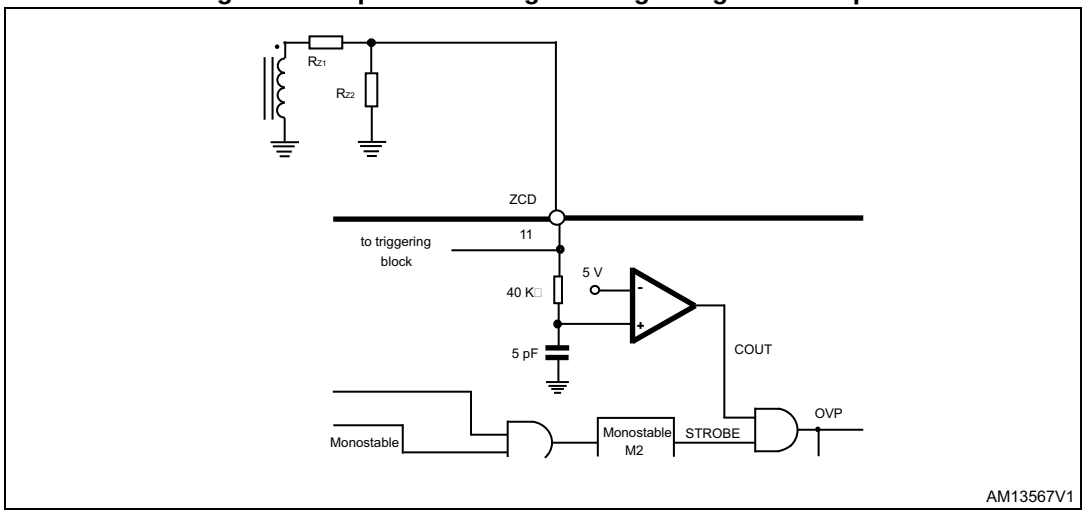
There are two functions of the ZCD pin:

- De-magnetizing input in QR operation by taking feedback from auxiliary winding
- Sensing output voltage reflection through auxiliary winding and initiate output overvoltage shutdown at desired output OVP level

The zero current detection (ZCD) and triggering blocks switch on the external MOSFET if a negative-going edge falling below 50 mV is applied to the input (pin 11, ZCD). To do so the triggering block must be previously armed by a positive-going edge exceeding 100 mV. This feature is usually used for sensing transformer demagnetization in QR operation to start another switching cycle. The signal for the ZCD input is obtained from the transformer's auxiliary winding used also to supply the L6566B. The triggering block is blanked for TBLANK = 2.5 µs after MOSFET's turnoff to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously.

The same pin also performs OVP protection. The resistor divider network at the ZCD pin sets the OVP level where protection is required. If the voltage on the pin exceeds an internal 5 V reference, a comparator is triggered, an overvoltage condition is assumed and the device is shut down. An internal current generator is activated that sources 1 mA out of the VFF pin (15). If the VFF voltage is allowed to reach 2 Vbe over 5 V, the L6566B will be latched off. If the impedance externally connected to pin 15 is so low that the 5+2VBE threshold cannot be reached or if some means is provided to prevent that, the device will be able to restart after the $V_{CC}$ has dropped below 5 V. So in that case this OVP protection by ZCD pin will be auto restart type. On the other hand if VFF pin is grounded with a 10 K resistor, in that case as soon as ZCD senses 5 V due to overvoltage at output, the internal current generator starts providing current to the VFF pin and voltage of VFF pin reaches 6.4 V. In that case the device gets latched due to output OVP. So both auto restart as well as latched shutdown protections are possible.

**Figure 8. Output overvoltage setting using Z the CD pin**




The ZCD pin will be connected to the auxiliary winding through a resistor divider RZ1, RZ2 as shown above. The divider ratio kOVP = RZ2 / (RZ1 + RZ2) will be chosen equal to:

**Equation 6**

$$k_{OVP} = \frac{5}{Vout_{OVP}} \frac{Ns}{Naux}$$

Where

- $Vout_{OVP}$ = output voltage level that is to activate the protection
- Ns = number of turns of secondary winding
- Naux = number of turns of the auxiliary winding

The value of RZ1 will be such that the current sourced by the ZCD pin is within the rated capability of the internal clamp:

**Equation 7**

$$R_{Z1} \geq \frac{1}{3 \cdot 10^{-3}} \frac{Naux}{Np} Vin_{max}$$

where

- $Vin_{max}$= maximum DC input voltage.

Referring to the schematic, RZ1=R17 and RZ2=R25. Based on the above relations and transformer turns ratio, R17=47 K and R25=10 K.

# 9 Basic power stage calculations

The power supply specifications are:

- $V_{acmin}$ = 90 $V_{ac}$
- $V_{acmax}$ = 265 $V_{ac}$

Taking the approximate minimum and maximum rectified voltage:

- $V_{inmin}$ = 90√2 = 127 $V_{dc}$
- $V_{inmax}$ = 265√2 = 374 $V_{dc}$
- $V_{out}$ = 24 V, $I_{out}$ = 2.5 A

Maximum output power, $P_{out}$ = $V_{out}$ x $I_{out}$ = 60 W

Overall system efficiency, η = 0.85

Minimum switching frequency, $f_{swmin}$ = 60 KHz

Since the operation is QR, the primary inductance of transformer can be calculated with the following equation:

**Equation 8**

$$L_{pmax} = \frac{1}{\left[\sqrt{2 \cdot P_{in\ max} \cdot f_{sw\ min}} \cdot \left(\frac{1}{V_{in\ min}} + \frac{1}{V_R}\right) + \pi \cdot f_{sw\ min} \cdot \sqrt{C_d}\right]^2},$$

The converter is operating in DCM. For approximate value, we can simply neglect Cd implications, so we have:

**Equation 9**

$$Pin_T = \frac{\left(\frac{Vin\ V_R}{Vin + V_R}\right)^2}{2 f_{sw} Lp}$$

Considering the transformer efficiency up to 95%, ηT = 0.95, we have

- PinT = 63 W

We approximate, Lp = 500 uH.

- $P_{inmax}$ = $P^{out}$/η = 70.5 W

Peak primary current can be calculated with below equation:

**Equation 10**

$$I_{PKp} = \sqrt{\frac{2 \cdot P_{in}}{L_p \cdot f_{sw}}}$$

$I_{pkp}$ = 2.2 A

Primary duty cycle;

**Equation 11**

$$D = \frac{1}{V_{in}} \cdot \sqrt{2 \cdot P_{in} \cdot L_p \cdot f_{sw}}$$

D = 0.51

Secondary duty cycle:

**Equation 12**

$$D' = \frac{1}{V_R} \cdot \sqrt{2 \cdot P_{out} \cdot L_p \cdot f_{sw}}$$

D' = 0.43

Secondary peak current can be calculated with below equation:

**Equation 13**

$$I_{PKs} = \frac{2 \cdot I_{DCs}}{D'}$$

$I_{pks}$ = 11.63A

Primary side DC current can be calculated with below equation:

**Equation 14**

$$I_{DCp} = \frac{1}{2} \cdot I_{PKp} \cdot D$$

$I_{DCp}$ = 0.56A

Output average current:

**Equation 15**

$$I_{DCs} = \frac{P_{out}}{V_{out}}$$

$I_{DCs}$ = 2.5 A

Primary side RMS current can be calculated with below equation:

**Equation 16**

$$I_{RMSp} = I_{PKp} \cdot \sqrt{\frac{D}{3}}$$

$I_{RMSp}$ = 0.9 A

Secondary RMS current can be calculated with below equation:

**Equation 17**

$$I_{RMSs} = I_{PKs} \cdot \sqrt{\frac{D'}{3}}$$

$I_{RMSs}$ = 4.4 A

Peak MOSFET voltage, Vds = $V_{inmax}$+ VR+Spike,

Where Vinmax should be taken where mains OVP cut is required, lets take it at 420 V.

So $V_{ds}$ = 420+140+100 = 660 V, use an 800 V MOSFET to obtain a good, safe margin.

Select STP10NK80Z.

Rectifier max reverse voltage:

**Equation 18**

$$V_{REV} = V_{out} \cdot \left(1 + \frac{V_{PKmax}}{V_R}\right)$$

- $V_{rev}$ = 96 V
- Use 120 V Schottky
- Select 2xSTPS20120CFP parallel

# 10 Transformer specifications

## 10.1 General description and characteristics

- Application type: consumer, home appliance
- Transformer type: open
- Coil former: horizontal type, 6+6 pins
- Max. temp. rise: 45 ºC
- Max. operating ambient temperature: 50 ºC
- Mains insulation: in acc. with EN60950

## 10.2 Electrical characteristics

- Converter topology: QR flyback
- Core type: ETD34, N87 or equivalent
- Typical operating frequency: 100 kHz
- Primary inductance: 500 µH±10% at 1 kHz-0.25 V (a)
- Leakage inductance: 5 µH Max at 100 kHz-0.25 V (b)
- Measured between pins 3-1
- Measured between pins 3-1 with secondary windings shorted

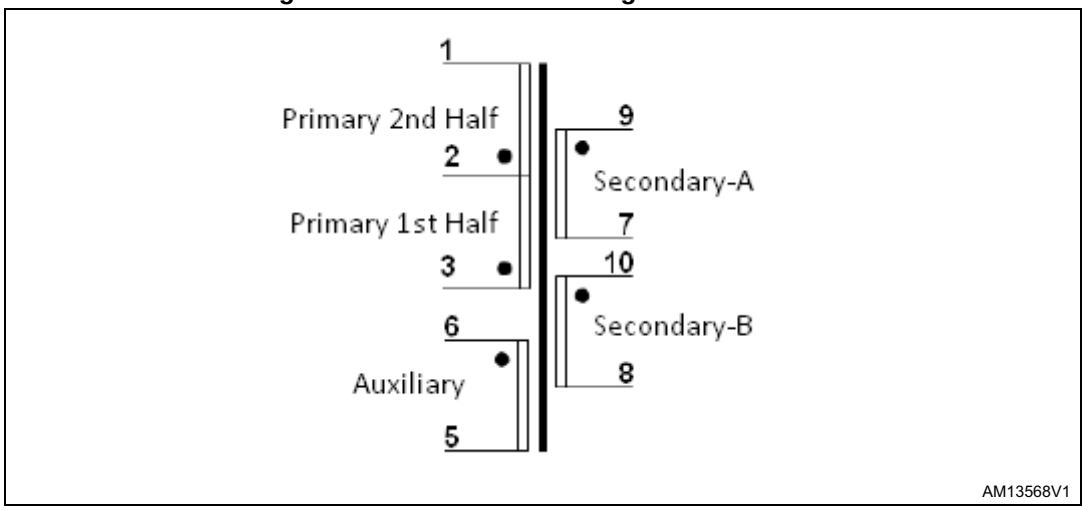
## 10.3 Winding details

**Table 2.**

| Pins | Winding | RMS current | Number of turns | Wire gauge |
|---|---|---|---|---|
| 3-2 | Primary 1st Half | 0.9 Arms | 30 | 4XAWG27 |
| 9-7 | Secondary-A | 2.3 Arms | 11 | 6XAWG22 |
| 10-8 | Secondary-B | 2.3 Arms | 11 | 6XAWG22 |
| 2-1 | Primary 1st half | 0.9 Arms | 30 | 4XAWG27 |
| 6-5 | Auxiliary | 0.05 Arms | 6 | 1XAWG32 |

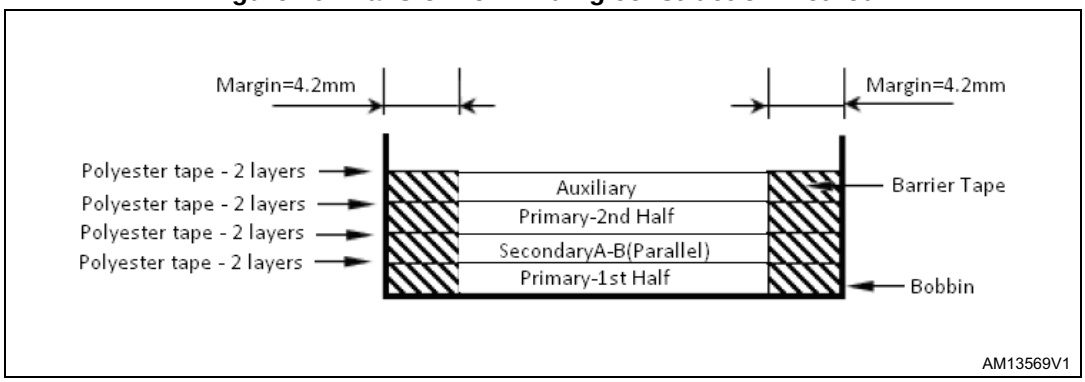
*Note: Secondary windings are wound between primary 1st half and primary 2nd half layers. Secondary windings A and B are in parallel.*

**Figure 9. Transformer windings & termination**




## 10.4 Winding construction

**Figure 10. Transformer winding construction method**



# 11 Control loop

Opto coupler CTR = 1.

Required phase margin > 50°.

*Figure 11* shows the resulting bode plot with the selection of following compensation values:

- $C_{comp}$ = C21 = 5.6 nF
- $R_{fb.}$= R31 = 0 E
- $C_{fb}$ = C20 = 330 nF
- $R_{opto}$ = R24 = 1.2 K
- $R_{bias}$ = R27 = 2.2 K

**Figure 11. Magnitude and phase plot at 230 $V_{ac}$, full load 60 W**

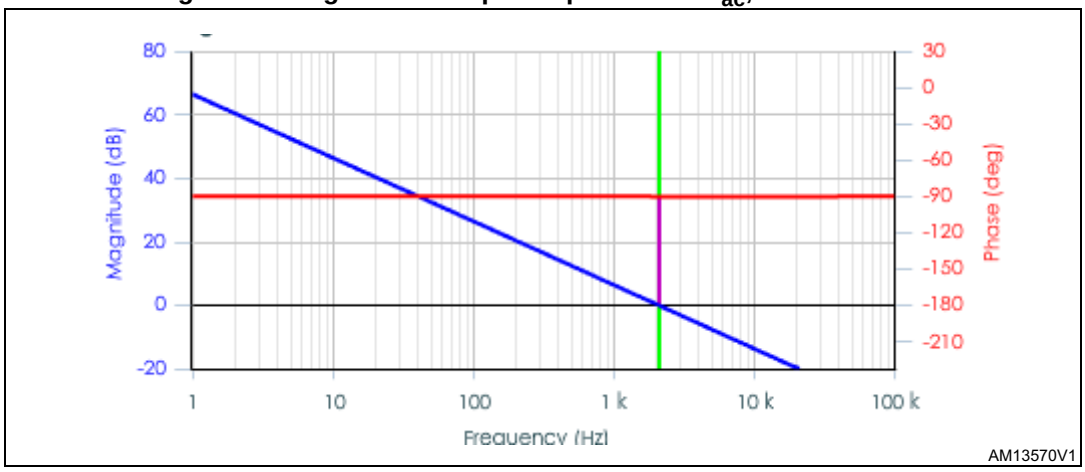



**Figure 12. Magnitude and phase plot at 230 $V_{ac}$, light load 6 W**

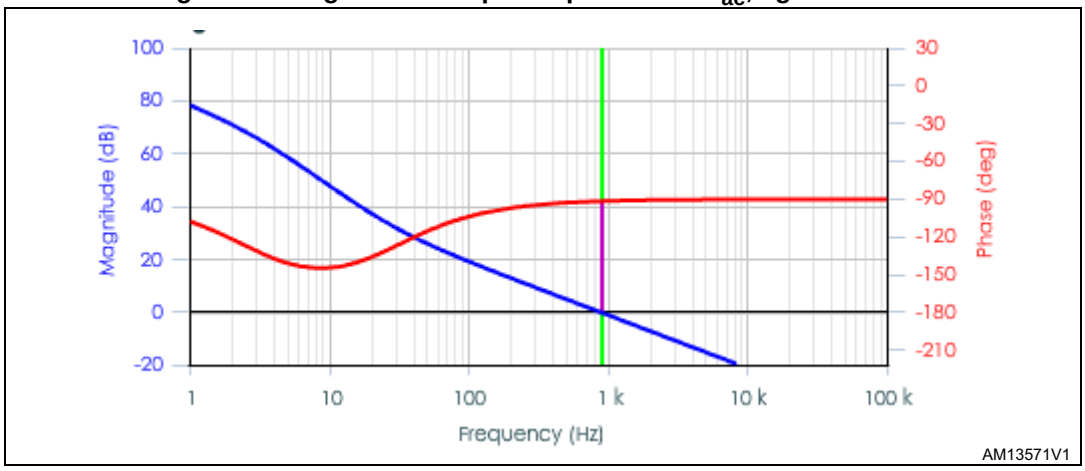


**Figure 13. Magnitude and phase plot at 115 $V_{ac}$, full load 60 W**

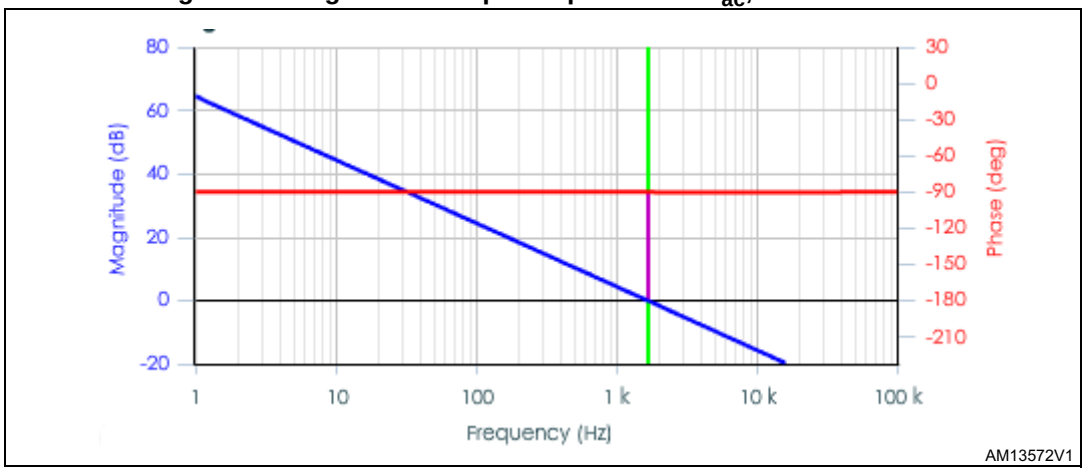
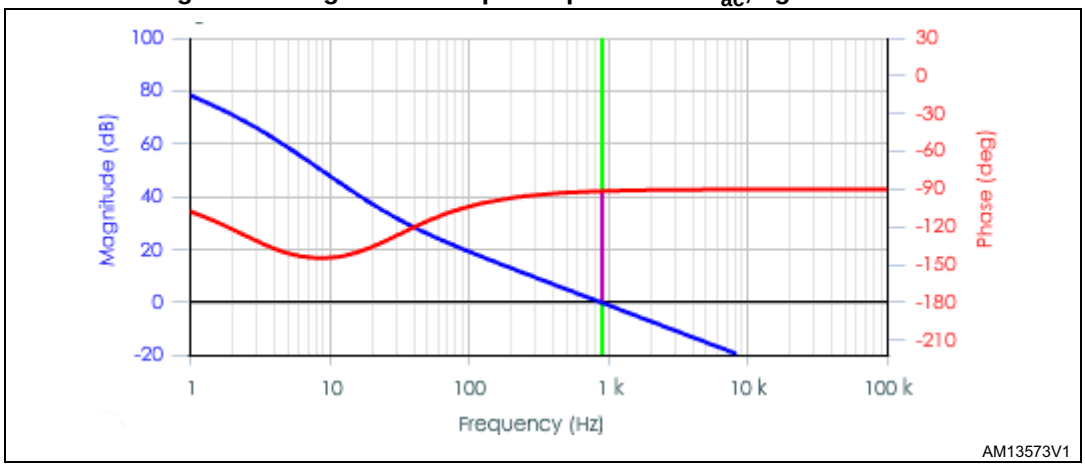
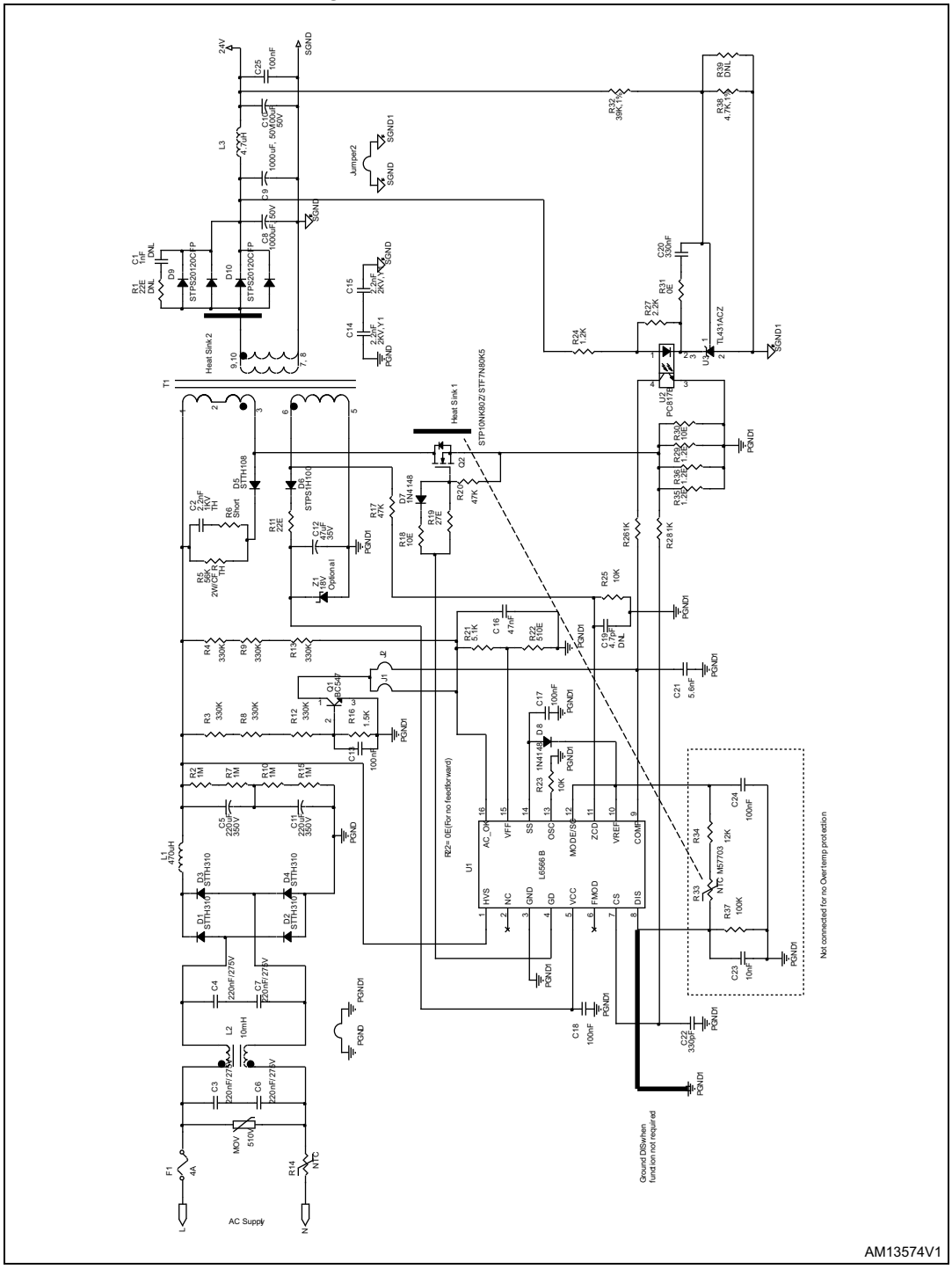



**Figure 14. Magnitude and phase plot at 115 $V_{ac}$, light load 6 W**



# 12 Schematic diagram

**Figure 15. Electrical schematic**



# 13 Bill of material

**Table 3. Bill of material**

| Sr no | Part reference | Part description | Make |
|---|---|---|---|
| 1 | R2 | Resistor 1 M, SMD 1206 | |
| 2. | R7 | Resistor 1 M, SMD 1206 | |
| 3 | R10 | Resistor 1 M, SMD 1206 | |
| 4 | R15 | Resistor 1 M, SMD 1206 | |
| 5 | R3 | Resistor 330 K, SMD 1206 | |
| 6 | R8 | Resistor 330 K, SMD 1206 | |
| 7 | R12 | Resistor 330 K, SMD 1206 | |
| 8 | R4 | Resistor 330 K, SMD 1206 | |
| 9 | R9 | Resistor 330 K, SMD 1206 | |
| 10 | R13 | Resistor 330 K, SMD 1206 | |
| 11 | R16 | Resistor 1.5 K, SMD 1206 | |
| 12 | R21 | Resistor 5.1 K, SMD 1206 | |
| 13 | R22 | Resistor 510 E, SMD 1206 | |
| 14 | R17 | Resistor 47 K, SMD 0805 | |
| 15 | R25 | Resistor 20K, SMD 0805 | |
| 16 | R23 | Resistor 10K, SMD 0805 | |
| 17 | R37 | Resistor 100K, SMD 0805 | |
| 18 | R26 | Resistor 1 K, SMD 0805 | |
| 19 | R28 | Resistor  1 K, SMD 0805 | |
| 20 | R34 | Resistor 12 K, SMD 0805 | |
| 21 | R35 | Resistor 1.2 E, SMD 1206, 1% | |
| 22 | R36 | Resistor 1.2 E, SMD 1206, 1% | |
| 23 | R29 | Resistor 1.2 E, SMD 1206, 1% | |
| 24 | R30 | Resistor 10 E, SMD 1206 | |
| 25 | R18 | Resistor 10 E, SMD 0805 | |
| 26 | R11 | Resistor 22 E, SMD 0805 | |
| 26 | R19 | Resistor 27 E, SMD 0805 | |
| 27 | R20 | Resistor 47 K, SMD 0805 | |
| 28 | R24 | Resistor 1.2 K, SMD 0805 | |
| 29 | R27 | Resistor 2.2 K, SMD 0805 | |
| 30 | R32 | Resistor 39 K, SMD 0805, 1% | |
| 31 | R38 | Resistor 4.7 K, SMD 0805, 1% | |

Table 3. Bill of material (continued)

| Sr no | Part reference | Part description | Make |
|---|---|---|---|
| 32 | R5 | Resistor 56 K, 2 W CFR through hole | |
| 33 | R39 | Resistor DNL | |
| 34 | R6 | Resistor DNL Through hole, 0.25 W | |
| 35 | R1 | Resistor 22E, SMD 1206 DNL | |
| 36 | R31 | Resistor 0E, SMD 0805 | |
| 36 | C3 | Capacitor 220Nf/275 V, X2 through hole | |
| 37 | C6 | Capacitor 220Nf/275 V, X2 through hole | |
| 38 | C4 | Capacitor 220Nf/275 V, X2 through hole | |
| 39 | C7 | Capacitor 220Nf/275 V, X2 through hole | |
| 40 | C2 | Capacitor ceramic disc type 2.2Nf/1 KV through hole | |
| 41 | C13 | Capacitor 100Nf, 0805 | |
| 42 | C24 | Capacitor 100Nf, 0805 | |
| 43 | C17 | Capacitor 100Nf, 0805 | |
| 44 | C18 | Capacitor 100Nf, 0805 | |
| 45 | C25 | Capacitor 100Nf, 0805 | |
| 46 | C22 | Capacitor 330Pf, 0805 | |
| 47 | C21 | Capacitor 5.6Nf, 0805 | |
| 48 | C19 | Capacitor 4.7Pf, 0805 DNL | |
| 49 | C23 | Capacitor 10Nf, 0805 | |
| 50 | C16 | Capacitor 47Nf, 0805 | |
| 51 | C20 | Capacitor 330Nf, 0805 | |
| 52 | C1 | Capacitor 1Nf , 1206 DNL | |
| 53 | C14 | Capacitor 2.2Nf/2 KV, Y1 through hole | |
| 54 | C15 | Capacitor 2.2Nf/2 KV, Y1 through hole | |
| 55 | C5 | Capacitor elect 220Uf/350 V through hole | |
| 56 | C11 | Capacitor elect 220Uf/350 V through hole | |
| 57 | C12 | Capacitor elect 47Uf/35 V through hole | |
| 58 | C8 | Capacitor elect 1000Uf/50 V low ESR through hole | |
| 59 | C9 | Capacitor elect 1000Uf/50 V low ESR through hole | |
| 60 | C10 | Capacitor elect 100Uf/50 V through hole | |
| 61 | D1 | Diode STTH310, package DO-201AD | |
| 62 | D2 | Diode STTH310, package DO-201AD | |
| 63 | D3 | Diode STTH310, package DO-201AD | |
| 64 | D4 | Diode STTH310, package DO-201AD | |
| 65 | D6 | Diode STTH1R02, package DO-41 | |

**Table 3. Bill of material (continued)**

| Sr no | Part reference | Part description | Make |
|---|---|---|---|
| 66 | D5 | Diode STTH108, package DO-41 | |
| 67 | D7 | Diode 1N4148 SMD | |
| 68 | D8 | Diode 1N4148 SMD | |
| 69 | D9 | Diode Schottky STPS20120CFP, package TO-220FPAB | ST |
| 70 | D10 | Diode Schottky STPS20120CFP, package TO-220FPAB | ST |
| 71 | U1 | PWM controller L6566B, package SO-16 | ST |
| 72 | U3 | Reference voltage IC TL431ACZ, package TO-92 | ST |
| 73 | U2 | Optocoupler PC817B , package DIP-4 | |
| 74 | Q2 | MOSFET STP10NK80Z, package TO-220AC, or STF7N80K5, package TO-220FP | ST |
| 75 | Q1 | Transistor BC547, package TO-92 | |
| 76 | L1 | DC side inductor 470 Uh Drum type | |
| 77 | L2 | Common mode filter 10 Mh | |
| 78 | L3 | DC side inductor 4.7 Uh drum type | |
| 79 | T1 | Transformer ETD34 | |
| 80 | F1 | Mains fuse glass type 4 A | |
| 81 | R14 | NTC | |
| 82 | R33 | NTC M57703 | |
| 83 | MOV | 510 Vrms rated, S10K510 | Epcos |
| 84 | Z1 | Zener 22 V/0.5 W (optional) | |

# 14 Test results

**Table 4. Test results**

| Load % | $V_{ac}$(V) | $I_{ac}$(A) | Pin(W) | Vo(V) | Io(A) | Po(W) | % η |
|---|---|---|---|---|---|---|---|
| 25 | 100 | 0.260 | 17.30 | 24.47 | 0.602 | 14.73 | 85.15 |
| | 180 | 0.163 | 17.27 | 24.46 | 0.602 | 14.72 | 85.26 |
| | 230 | 0.138 | 17.80 | 24.45 | 0.602 | 14.72 | 82.69 |
| | 265 | 0.129 | 18.00 | 24.45 | 0.602 | 14.72 | 81.77 |
| 50 | 100 | 0.495 | 34.10 | 24.44 | 1.202 | 29.38 | 86.15 |
| | 180 | 0.298 | 33.60 | 24.42 | 1.202 | 29.35 | 87.36 |
| | 230 | 0.250 | 33.80 | 24.42 | 1.201 | 29.33 | 86.77 |
| | 265 | 0.228 | 34.00 | 24.42 | 1.201 | 29.33 | 86.26 |
| 75 | 100 | 0.752 | 52.30 | 24.40 | 1.807 | 44.09 | 84.30 |
| | 180 | 0.446 | 50.01 | 24.40 | 1.807 | 44.09 | 88.16 |
| | 230 | 0.367 | 50.00 | 24.39 | 1.806 | 44.05 | 88.10 |
| | 265 | 0.330 | 50.01 | 24.38 | 1.806 | 44.03 | 88.04 |
| 100 | 100 | 0.990 | 70.80 | 24.30 | 2.400 | 58.32 | 82.37 |
| | 180 | 0.574 | 66.80 | 24.34 | 2.404 | 58.51 | 87.59 |
| | 230 | 0.470 | 66.10 | 24.35 | 2.404 | 58.54 | 88.56 |
| | 265 | 0.428 | 66.20 | 24.36 | 2.404 | 58.56 | 88.46 |

– Average efficiency at Full load over entire mains operation: 86.75%
– Full load Efficiency at nominal input 230 $V_{ac}$: 88.56%

# 15 Functional check

The flyback waveforms are analyzed (refer to *Figure 16* through *Figure 31*) during steady-state operation of the SMPS. The waveforms are captured at different load conditions - 25%, 50%, 75% and 100% at different operating mains voltage, starting from 100 $V_{ac}$ to 265 $V_{ac}$.

*Note: CH1: drain current; CH2: $V_{cc}$ voltage; CH3: COMP Pin; CH4: drain-source voltage.*

**Figure 16. Condition 1: $V_{ac}$ = 100 V; $I_{out}$ = 0.6 A**


AM13575V1

Figure 17. Condition 2: $V_{ac}$ = 100 V; $I_{out}$ = 1.2 A


AM13576V1

Figure 18. Condition 3: $V_{ac}$ = 100 V; $I_{out}$ = 1.8 A


AM13577V1

Figure 19. Condition 4: $V_{ac}$ = 100 V; $I_{out}$ = 2.4 A


AM13578V1

Figure 20. Condition 5: $V_{ac}$ = 180 V; $I_{out}$ = 0.6 A


AM13579V1

Figure 21. Condition 6: $V_{ac}$ = 180 V; $I_{out}$ = 1.2 A


AM13580V1

Figure 22. Condition 7: $V_{ac}$ = 180 V; $I_{out}$ = 1.8 A


AM13581V1

Figure 23. Condition 8: $V_{ac}$ = 180 V; $I_{out}$ = 2.4 A


AM13582V1

Figure 24. Condition 9: $V_{ac}$ = 230 V; $I_{out}$ = 0.6 A


AM13583V1

Figure 25. Condition 10: $V_{ac}$ = 230 V; $I_{out}$ = 1.2 A


AM13584V1

Figure 26. Condition 11: $V_{ac}$ = 230 V; $I_{out}$ = 1.8 A


AM13585V1

Figure 27. Condition 12: $V_{ac}$ = 230 V; $I_{out}$ = 2.4 A


AM13587V1

Figure 28. Condition 13: $V_{ac}$ = 265 V; $I_{out}$ = 0.6 A


AM13586V1

Figure 29. Condition 14: $V_{ac}$ = 265 V; $I_{out}$ = 1.2 A


AM13588V1

Figure 30. Condition 15: $V_{ac}$ = 265 V; $I_{out}$ = 1.8 A


AM13589V1

Figure 31. Condition 16: $V_{ac}$ = 265 V; $I_{out}$ = 2.4 A


AM13590V1

# 16 Holdup test

The mains input is interrupted at loaded conditions to observe the holdup capability of SMPS. Referring to the waveform in *Figure 32*, the converter is able to deliver the load in case 4 cycles of 50 Hz mains supply at 230 $V_{ac}$ are missing.

This is important in cases of interruption or dips in the mains supply voltage. The input bulk capacitors should have enough capacitance to ensure no interruption of output power delivery to the load in case of missing AC cycles. A holdup time of at least 2 missing AC cycles (i.e. 40 ms) are enough for any SMPS to pass this criterion. In the present design, the SMPS is able to provide more than 2 cycles.

# 17 Soft start test

*Figure 33* shows the output voltage rise at the time the mains supply is supplied to converter. The test is conducted at 230 $V_{ac}$ nominal.

# 18 Short-circuit test

The output is short-circuited and the converter is powered at 230 $V_{ac}$, the power supply enters protection mode. In case of output short, there are two different possible situations that the controller must handle: if the coupling between the secondary winding and the auxiliary winding is good, as soon as the output voltage drops, the auxiliary voltage drops as well and the IC supply voltage falls below the undervoltage lockout threshold, causing the L6566B to stop switching. It remains in the off-state until the voltage on the $V_{CC}$ pin decreases below the $V_{CC}$ restart threshold (5 V), then the HV startup turns on and charges the $V_{CC}$ capacitor; as soon as the turn-on threshold is reached, the converter restarts. If the short is still there, the converter just attempts to restart but it stops for a long period. Restart attempts are repeated indefinitely until the short is removed. This provides a very low frequency hiccup working mode, limiting the current flowing at the secondary side (less than 1 Arms) preventing the power supply from overheating, which could destroy it.

In the case where the coupling between the auxiliary and secondary winding is poor, some spikes on the auxiliary voltage may keep $V_{CC}$ above the UVLO threshold for a period long enough to damage the converter. In this case the L6566B detects a short-circuit by monitoring the control pins: in the case of a short, the COMP pin goes high, and an internal comparator activates a current source that restarts charging the soft-start capacitor from the initial 2 V level. If the voltage on this pin reaches 5 V, the L6566B stops operation and it restarts with a startup sequence when the $V_{CC}$ voltage drops below the $V_{CC}$ restart level (5 V), entering into the so-called “Hiccup mode”.

*Figure 34* through *Figure 37* shows the converter switching behavior during short-circuited output. The waveforms are captured at different time scales to clearly understand the operation during short-circuit.

In *Figure 34* , we can observe the behavior of the $V_{CC}$ voltage as described above. In *Figure 35*, the waveforms are triggered in different time scale, where single switching pulses are spaced with 150 us.

*Figure 36* & *37* displays more clearly the single pulse timing and peak values of drain-source voltage with leakage spike overshoot and peak drain current values. Triggered at different levels corresponding to different Ton instants. Looking to figure 22, maximum drain current is limited to 2.7 A peak approx and there is no saturation effect observed in transformer.

The overall operation is safe and average input power from the mains drops to negligible values.

**Figure 32. Hold up test CH1: load current 2.4 A max; CH4: AC Input 230 V**

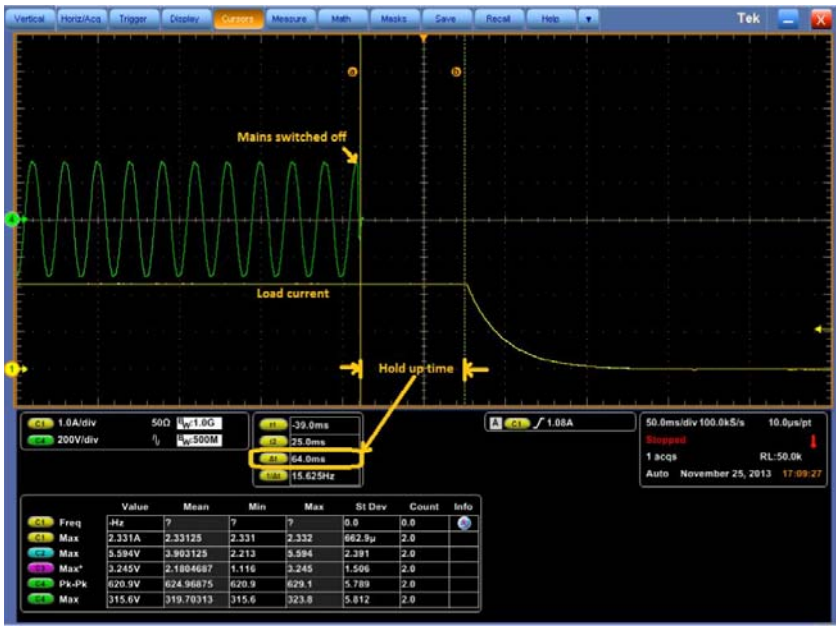


**Figure 33. Output soft start CH1: load current; CH2: output voltage, 24 Vmax**


AM13592V1

**Figure 34. Output short circuit (hiccup mode)**


CH1: drain current; CH2: Vcc voltage; CH3: COMP pin; CH4: drain-source voltage

AM13593V1

**Figure 35. Switching attempts during hiccup mode**

CH1: drain current; CH2: Vcc voltage; CH3: COMP pin; CH4: drain-source voltage

AM13594V1

**Figure 36. Single switching pulse ($V_{drain}$ and $I_{drain}$)**

CH1: drain current; CH2: Vcc voltage; CH3: COMP pin; CH4: drain-source voltage

AM13595V1

**Figure 37. Single switching pulse-no saturation of transformer**


CH1: Drain current; CH2: Vcc Voltage; CH3: COMP pin ; CH4: Drain-source voltage AM13596V1

# 19 Burst mode

*Figure 38* and *Figure 39* shows the operation of converter during no load conditions. When there is very light load or no load at output, L6566B COMP pin voltage goes below 2.65 V, the IC get disabled and power consumption goes is reduced. As soon as COMP pin voltage rises above this threshold, the switching attempts takes place.

So during this conditions the input power from mains goes in range of mW. The AC input power consumptions are mentioned below at extreme line operating conditions.

**Figure 38. Burst mode operation at 100 $V_{ac}$**


CH3: COMP pin; CH4: drain-source voltage; input power < 300 mW

GIPG040420141336R

**Figure 39. Burst mode operation at 265 $V_{ac}$**


CH3: COMP pin; CH4: drain-source voltage; input power < 300 mW

GIPG040420141342RV

*Note: Above no load power consumptions are measured with resistors (R2, R3, R7,R8, R10, R12, R15 & R16) connected at rectified dc bus input and causing additional power losses. The standby losses can be further go down by increasing the value of resistors as well as removing in case no line-line withstanding and mains brownout features are required.*

# 20 Temperature rise test

The temperature of the main components like power discrete and magnetic are observed until gets saturated at constant level after continuous working of power supply unit. Below is the temperature of main components at nominal input of 230 $V_{ac}$:

**Table 5. Temperature rise test**

| Location of thermal sensor | Measured temperature( °C) |
|---|---|
| MOSFET Q2(STP10NK80Z) case | 51.8 |
| Schottky D9, D10 case | 64.2 |
| Transformer(T1) core | 65.0 |

# 21 Reference


– L6566B datasheet
– AN1326: L6565 quasi-resonant controller

# 22 Revision history

Table 6. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 08-May-2014 | 1 | Initial release. |