

AN4218 Application note

Hardware design guideline power supply and voltage measurement

Introduction

This document provides useful hints and suggestions about the implementation of the STMicroelectronics 32-bit microcontroller devices in an automotive system. The main focus has been set on the power supply concept and the connection to signals from different power domains.

Due to the harsh conditions in the automotive environment several precautions have to be taken into account to ensure the robustness of the system. This is especially important when defining its power supply concept.

This document shows test cases defined by car makers, which are intended to reproduce the system behavior in the real automotive environment, it also shows good practices to cope with them as well as bad practices and their influence on the system robustness.

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AN4218 System overview

1 System overview

1.1 Overview

Figure 1 shows a system, consisting of a microcontroller, a system basis chip, a physical layer transceiver and load drivers.

The System-Basis-Chip (SBC) generates the power-supply for the other devices in the system and communicates via serial-parallel interface (SPI) with the microcontroller (SPC- μ C).

The physical layer transceiver (e.g. standalone CAN-transceiver) is supplied by the SBC and transfers data from and to the microcontroller via logic-level signals. Through the CAN-bus it is connected to other CAN-transceivers in the car, which have their own independent power supply.

Dedicated drivers for high-power loads (light-bulbs, LEDs, door locks, mirror folds, H-bridge drivers etc.) are also connected to the microcontroller power supply and communicate with it by SPI.

Several peripherals of the microcontroller are used to monitor voltages like the battery voltage, either by a logic-level input/output or an analog-to-digital convertor (ADC).

The inductances LS1 to LS4 are the parasitic wire inductances of the supply lines. Capacitances are added to either protect the supply against distortions or to stabilize the voltage generated the by voltage controller inside the SBC.

Protection resistors are added at the monitor inputs of the microcontroller.

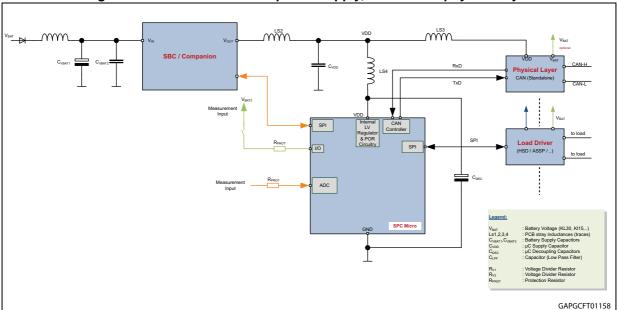


Figure 1. Microcontroller with power supply, drivers and physical layer

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1.2 Car-battery power supply (V_{BAT}) transients

In the following chapters tests are shown used in the automotive industry to check if a system consisting of a microcontroller and its power supply are able to withstand the harsh automotive application environment. These tests simulate transients on the battery power supply. They may happen due to switch-on or switch-off the energy consumers along the battery supply line with its huge inductance. Since these loads may consume large currents the magnetic energy stored in the supply cable is huge and its change results in high induced voltages.

As example requirements from the International-Standard-Organization (ISO) and some European car manufacturers are described. The influences of these tests have been measured on a system according to Figure~1, in which a voltage regulator, either standalone or as part of a System-Basis-Chip (SBC), generates out of the battery voltage (V_{BAT}) the supply voltage for the microcontroller (V_{DD}).

The power-up reset cell of a microcontroller ensures that the microcontroller is put into a well-defined state, when the supply voltage is switched on. The following conditions on the microcontroller power supply should be avoided:

Figure 2. Brown out

Figure 3. Non strictly rising ramp

VDD

VDD

VDD

OV

GAPGCFT01159

Figure 4. Slow ramp

Figure 5. Residual voltage

VDD VDD VDD OV GAPGCFT01161

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1.2.1 Example battery supply test pulses

Example test pulses can be found in test specification defined either by the ISO or various car makers (see *Appendix A: Reference documents*).

Engine cranking low voltage on battery-supply

This test is included in all reference documents. It tests the behavior of the system with a sharp voltage drop and ringing, which can be seen during the engine cranking.

As an example the Volkswagen test specification VW80000: 2009-10, defines the test pulse E11:

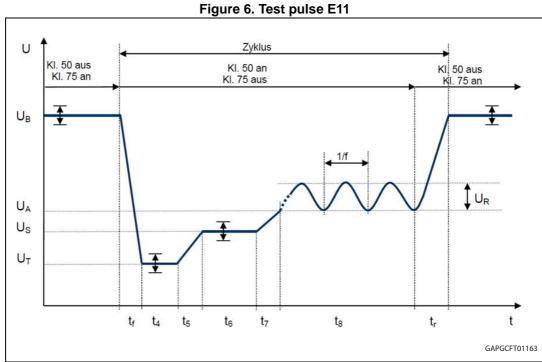


Table 1. Parameters sharp test pulse E11

Parameter	Test pulse (sharp)
U _B	11.0 V
U _T	3.2 V
U _S	5.0 V
U _A	6.0 V
U _R	2 V
t _f	≤ 1 ms
t ₄	19 ms
t ₅	≤ 1 ms
t ₆	329 ms
t ₇	50 ms

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Parameter	Test pulse (sharp)
t ₈	10 s
t _r	100 ms
f	2 Hz
R _i	0.01 Ω
Pause between test cycles	2 s
Number of test cycles	10

Table 1. Parameters sharp test pulse E11 (continued)

As shown in *Table 1* the 'sharp' pulse E11 on V_{BAT} (U_{B}) drops down to 3.2 V (U_{T}).

Car-battery supply voltage slow ramp-up

This test can be found in all reference documents and is intended to test the device behavior with a very slow battery voltage ramp (0.5 V/min). A proper power-up-reset has to be guaranteed.

Car-battery supply voltage slow ramp-down

This test can be found in all reference documents and is intended to test the device behavior with a very slow battery voltage ramp (0.5 V/min). A proper device shut-down has to be guaranteed.

Reverse car-battery supply voltage

This tests the system behavior when the power supply is reversed.

1.2.2 Power-up-reset requirements of the SPC microcontrollers

V_{DD} ramp-up/ ramp-down (microcontroller supply)

Figure 7 and Table 2 show as example basic requirements for the microcontroller power supply (V_{DD}) ramp-up/ ramp-down (for actual values please refer to the associated device datasheet). The values below are derived from the SPC560B40x/50x, SPC560C40x/50x datasheet and SPC560P34x, SPC560P40x datasheet (see Appendix A: Reference documents).

These microcontroller supply requirements have to be fulfilled by the voltage regulator supplying the microcontroller.

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V_{DD_HV}(MAX)
V_{DD_HV}(MAX)
V_{PORH}(MAX)
POWER UP FUNCTIONAL RANGE POWER DOWN

GAPGCFT01164

Figure 7. V_{DD} ramp-up/ ramp-down (SPC560Bxx, SPC560Cxx, – example only)

Table 2. V_{DD} ramp specification (SPC560P34x, SPC560P40x – example only)

Symbol	Parameter	Minimum	Maximum
TV _{DD}	Slope characteristics on all V_{DD} during power up with respect to ground (V_{SS})	3 V/s	0.5 V/μs

2 Good practices of system power supply

2.1 Microcontroller power supply reactions on V_{BAT} transients

This section shows the measurements done on a system-basis-chip L99PM62GXP, which provides the power supply (V_{DD}) to the microcontroller.

In addition to the microcontroller power supply this device provides also an NRESET output, which should be used to drive the microcontroller NRESET input for achieving maximum reliability of the microcontroller power-up state.

The measurements have been taken from the STMicroelectronics In-Application-Validation-Report of the L99PM62GXP. This document is available on request.

2.1.1 L99PM62GXP block diagram

Figure 8 shows a typical ST system-basis chip, which contains voltage regulators to generate the supply for the microcontroller (output V1). Additionally it provides physical layer interfaces (LIN, CAN), a serial-parallel interface and various high-side and low-side drivers.

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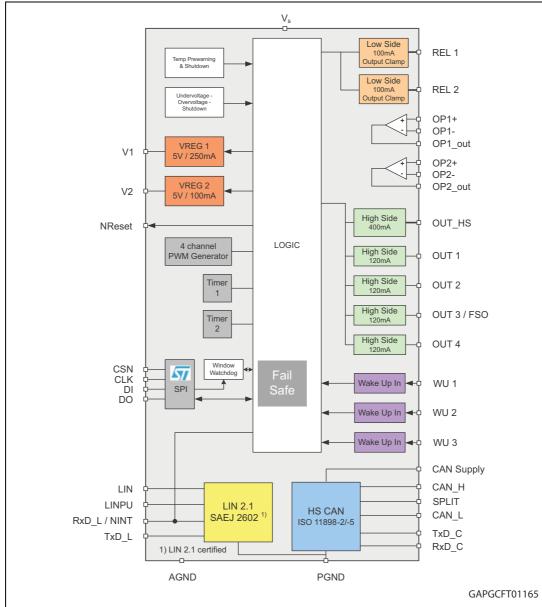


Figure 8. L99PM62GXP block diagram

2.1.2 Measurement setup

Oscilloscope Power Waveform Power supply generator supply Vboard Vbat Out1 **Companion Board** Out2 **USB** Out3 Out4 Loads L99PM62GXP Out_HS ST7 Daughterboard REL1 REL2 5V2 GAPGCFT01166

Figure 9. Measurement setup

2.1.3 Measurement results

These measurements show the microcontroller power supply $(V_{DD}-V1)$ and the NRESET output of the L99PM62GXP, if it is subject to the above defined test pulses.

Engine cranking low voltage

The parameter specification can be found in *Table 1*.

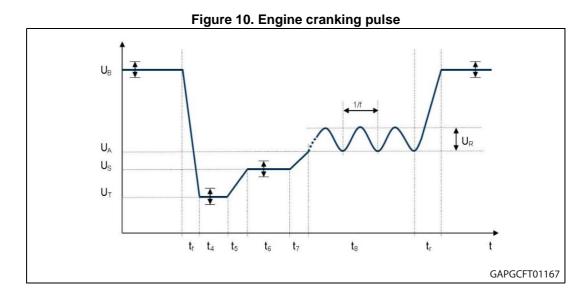




Figure 11. Measurement over the entire pulse

Line 1 (RST): NRESET output
Line 2 (V1): microcontroller power supply V_{DD}
Line 3 (VBAT): system power supply (V_{BAT})
Line 4 (OUT_HS): high-side driver output
Line D4 (CSN): SPI-logic signal chip-select-not
Line D5 (OUT_LS): low-side driver output
Line D7 (FSO): fail-safe state (internal signal)

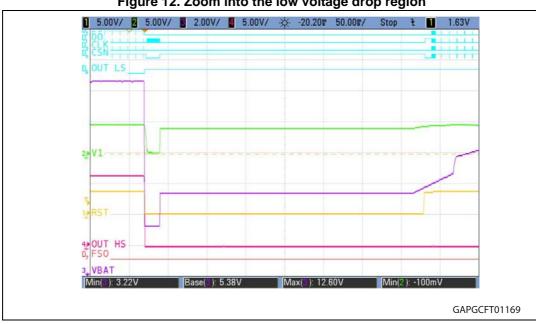


Figure 12. Zoom into the low voltage drop region

Line 1 (RST): NRESET output
Line 2 (V1): microcontroller power supply V_{DD}
Line 3 (VBAT): system power supply (V_{BAT})
Line 4 (OUT_HS): high-side driver output
Line D4 (CSN): SPI-logic signal chip-select-not
Line D5 (OUT_LS): low-side driver output
Line D7 (FSO): fail-safe state (internal signal)



During the V_{BAT} drop to 3.2 V, V1 (V_{DD}) goes to 0 V and switches on after V_{BAT} has reached L99PM62GXP reset threshold. In this case the NRESET output is pulled low and goes to high 2 ms after V1 has reached the NRESET high threshold.

Conclusion

The steep drop of V1 to 0 V in addition with the fast rising slope of V1 after V_{BAT} has recovered ensures a correct power-up reset of the microcontroller.

The NRESET output goes low to put the microcontroller into reset condition; it goes to high after V1 has reached the microcontrollers operating region.

The correct power-down / power-up sequence ensures that the microcontroller is always in a defined state. This is additionally supported by the NRESET signal.

Supply voltage slow ramp-up



Figure 13. V_S voltage ramp up (0.5 V/min)

As long as V_{BAT} is below the L99PM62GXP reset threshold, V1 remains at 0 V. After V_{BAT} has reached the reset threshold of 3.1 V, V1 is switched on with a fast slope. As soon as the NRESET threshold is reached NRESET goes to high.

Conclusion

The fast slope of V1 above the power-up-reset threshold of the microcontroller ensures a correct power-up-reset of the microcontroller, depending only on the capacitors at the V1 node and not on the battery voltage slope.

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Line 1 (RESET): NRESET output Line 2 (V1): microcontroller power supply V_{DD} Line 4 (VBAT): system power supply (V_{BAT})

The NRESET goes high after V1 has reached the operating region of the microcontroller. The correct power-up sequence ensures that the microcontroller is always in a defined state. This is additionally supported by the NRESET signal.

Supply voltage slow ramp-down

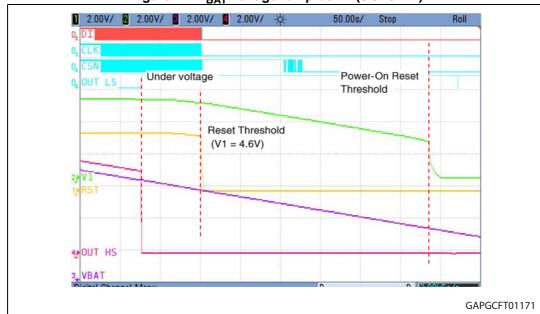


Figure 14. V_{BAT} voltage ramp down (0.5 V/min)

1. Line 1 (RST): NRESET output
Line 2 (V1): microcontroller power supply V_{DD}
Line 3 (VBAT): system power supply (V_{BAT})
Line 4 (OUT_HS): high-side driver output
Line D6 (OUT_LS): low-side driver output
Lines Dx (DI, CLK, CSN): SPI interface signals

As soon as V_{BAT} reaches the NRESET threshold, NRESET goes low and remains there until V_{BAT} is 0 V.

V1 goes to 0 V with a fast slope, when V_{BAT} is at the power-on-reset threshold of the L99PM62GXP.

Conclusion

The NRESET goes low after V1 has left the operating region of the microcontroller. Therefore the microcontroller is always in a defined state.

The fast falling slope of V1 above the power-up-reset threshold to 0 V of the microcontroller ensures a correct state of the microcontroller during V1 and V_{BAT} switch-off.

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3 Application circuits

3.1 Reference circuit

A system containing the microcontroller, the power supply generation, physical layer, load drivers and a measurement unit for permanent enabled battery supply (e.g. KL30) is shown in *Figure 15*.

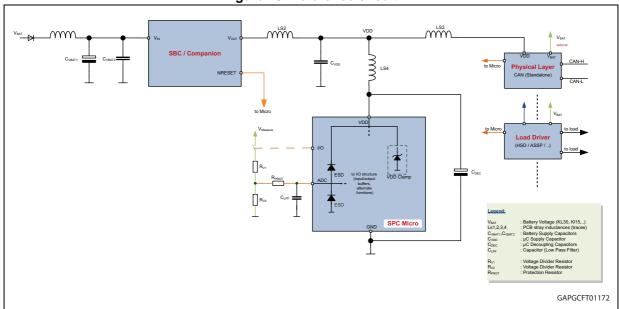


Figure 15. Reference circuit

3.2 Implementation suggestions

Besides the above mentioned requirements for the microcontroller power supply generation special care has to be taken on the following system parts.

3.2.1 Measurement of an permanently enabled power-supply (V_{MEASURE})

Since $V_{MEASURE}$ is permanently supplied, while the supply for the microcontroller system (V_{BAT}) can be turned off, it must be made sure, that the power-up functionality of the microcontroller is not influenced.

Additional the microcontroller pins have to be protected against ISO-pulses, which may damage the microcontroller. These ISO-transients are defined in ISO 7637-2:2011(E).

Note: The calculations and values used are examples only. For the actual values please refer to the latest datasheet of the used device.

Calculation of R_{V1/2} for ADC

The voltage divider has to be dimensioned such that no overvoltage condition at the analog-to-digital-convertor (ADC) input can occur. Especially it must be ensured, that the voltage at the ADC is never higher than at the V_{DD} , which supplies the ADC pin.

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For further information please consult the actual datasheet of the used microcontroller.

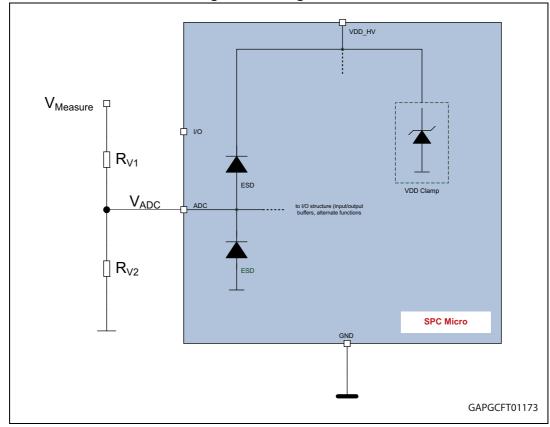


Figure 16. Voltage divider

Example 1:

Maximum $V_{ADC} = 5.0V$

Maximum $V_{MEASURE} = 40V$

$$\Rightarrow \frac{R_{V2}}{(R_{V1} + R_{V2})} = \frac{5.0V}{40V}$$

Insertion of a series protection resistor (R_{PROT})

The series resistor R_{PROT} prevents current injection spikes into the microcontroller and its ESD-diodes if an ISO-transient occurs.

These ISO-transients are defined in ISO 7637-2:2011(E).

The values used in the following calculations are examples only. Please consult the actual datasheet of the used device for the latest requirements.

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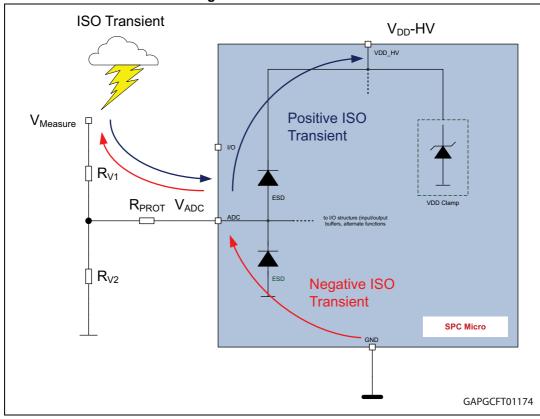


Figure 17. ISO transients

Example 2:

ISO-pulse 3b generates a maximum voltage of 100 V and uses an interior resistor of 50 Ω (R_I) at pin V_{MEASURE}. Neglecting R_I this leads to:

$$100V \cdot \frac{5V}{40V} = 12.5V$$

at the ADC-pin.

This voltage is clamped to V_{DD} + 0.7 V (typical ESD-diode drop). With V_{DD} = 5 V this clamp voltage is 5.7 V.

The maximum injected current at any pin derived from the absolute maximum ratings is 10 mA, so the series protection resistor (R_{PROT}) has to be at least

$$R_{PROT} = \frac{12.5V - 5.7V}{10mA} = 680\Omega$$

to clamp the positive pulse.

For the negative ISO-Pulse the calculation is similar: the ISO-Pulse 3a generates a negative voltage of -150 V over 50 Ω (R_I). Neglecting R_I the resulting voltage before R_{PROT} is

$$-150V \cdot \frac{5V}{40V} = -18.75V$$

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This is clamped to -0.7 V by the internal ESD-diode to ground, so $R_{\mbox{\footnotesize{PROT}}}$ has to be at least

$$R_{PROT} = \frac{-18.75V - (-0.7V)}{-10mA} = 1.805k\Omega$$

As can be seen from above calculations, the negative ISO pulse requires a series protection resistor of at least 2 k Ω to limit the injected current to the absolute maximum ratings. If the injected current has to be limited to ± 5 mA the required series protection resistor has to be at least 4 k Ω .

A larger resistor is recommended to cover the worst-case conditions.

This calculation applies for low-impedance voltage dividers at V_{MEASURE}.

A simplified calculation can be used for higher resistive R_{V1}:

• For the positive ISO-pulse:

$$R_{V1} \, = \, \frac{100 \, V - 5.7 \, V}{10 \, mA} \, = \, 9.42 k \Omega$$

• For the negative pulse:

$$R_{V1} \, = \frac{-150V - (-0.7V)}{-10mA} \, = \, 14.93k\Omega$$

So for $R_{V1} > 15 \text{ k}\Omega$ (30 k Ω for 5mA injection current), the series protection resistor can be omitted, but it protects the microcontroller input in case of a damaged R_{V1} .

Figure 18 shows a simulation of a negative 150 V ISO pulse. 'V(meas)' is the voltage at the $V_{MEASURE}$ pin, 'V(adc)' at V_{ADC} and 'Ix(xuc:IO)' the current that flows out of the microcontroller pin.

The resistor divider uses R_{V1} = 15 k Ω and R_{V2} = 2.2 k Ω .

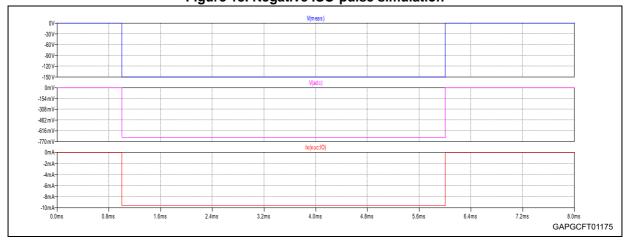


Figure 18. Negative ISO-pulse simulation

As can be seen in *Figure 18* the current out of the microcontroller with a negative ISO-pulse of 150 V does not increase above 10 mA.

Please refer to the latest datasheet of the used device for further information. Especially a possible impact on the accuracy of the analog-to-digital-convertor has to be taken into account.

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Low pass filter

The low-pass filter, which consists of R_{PROT} and C_{LPF} , has to be dimensioned such that the bandwidth of the ADC is not exceeded, since otherwise aliasing-artifacts may be observed.

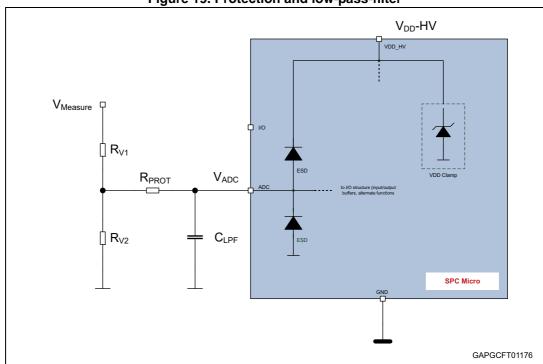


Figure 19. Protection and low-pass-filter

Figure 20 shows a simulation of the frequency (amplitude damping and phase) at V_{ADC} with R_{V1} = 15 kΩ, R_{V2} = 2.2 kΩ, R_{PROT} = 680 Ω and C_{LPF} = 1 nF. The input voltage is 15 V with an AC-Amplitude of 1 V (the voltage divider-by-8 causes an initial 18dB reduction).



Figure 20. Amplitude and phase over frequency

Divider disconnection switch

A switch at V_{MEASURE} avoids backward supplying from a powered V_{MEASURE} source to the unpowered microcontroller through the ESD diode of the input pin.

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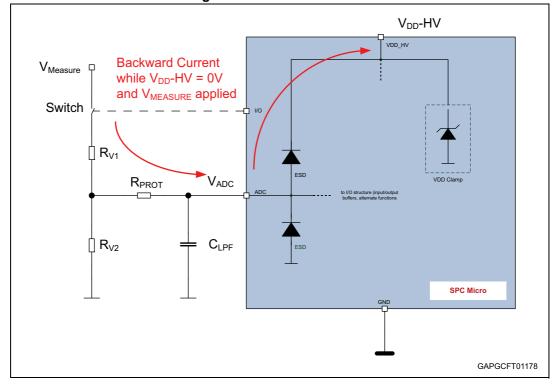


Figure 21. Backward current

With a current flowing through the ESD-diode, the voltage at pin V_{ADC} would be one V_{BE} (0.7 V_{typ}) higher than V_{DD} -HV, thus violating the absolute maximum rating of 0.3 V_{max} .

3.2.2 Bad practices

An example of a badly designed $V_{\mbox{\scriptsize MEASURE}}$ measurement interface is shown in the *Figure 22*.

The circuit does not contain a protection resistor R_{PROT} and no low-pass-filter.

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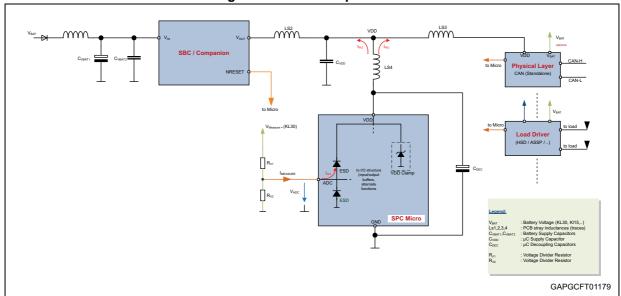


Figure 22. Bad example circuit

Calculation of R_{V1/2} for ADC

The calculation for the voltage divider is done in the same way as for the example with R_{PROT} .

In addition to this, also the ADC-protection regarding ISO-transients has to be taken into account.

Effects of the bad V_{MEASURE} implementation

Sensitivity to ISO transients

Any ISO pulse voltage (e.g. +100 V, - 150 V) applied to pin V_{MEASURE} is applied to the device pin and its ESD protection diode directly via R_{V1} . If R_{V1} is not high resistive enough (see example above), the microcontroller might be damaged.

Sensitivity to Electro-Magnetic-Injection (EMI)

All EMI-distortions at the pin V_{MEASURE} are coupled into the microcontroller pin via the voltage divider and may distort the microcontroller. A capacitor at the microcontroller pin improves this by adding a low resistive path to ground for high frequencies.

Residual voltage at V_{DD} in power down condition

A residual voltage at V_{DD} might happen if the current flowing from $V_{MEASURE}$ to V_{DD} via the microcontroller ESD protection diode is not actively sunk to ground.

Since the V_{DD} -net supplies other components in the system (e.g. physical layer, high load drivers etc.) they will get affected as well.

Absolute maximum ratings of the ESD-protection diode

In power down condition the absolute maximum voltage rating (e.g. 0.3 V) as well as the absolute maximum current rating (e.g. $75 \mu A$) may constantly be violated. The voltage and currents given above are examples only, for the actual values please refer to the associated datasheet.

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System reliability

The ESD-diodes inside of the microcontroller are designed for short discharge pulses only, not to sustain a constant current over time. Therefore the maximum continuous voltage drop over them is specified in the absolute maximum ratings to be not higher than 0.3 V. In this case only a very limited current is flowing through them.

A continuous current may lead to a degrading effect on these diodes over time.

3.2.3 Physical layer

Physical layer interfaces such as CAN-transceiver and LIN-transceivers may not have a reverse protection from the physical layer to its power supply, which may be connected to the microcontroller-supply (V_{DD}-HV). Since the physical layer is driven by other members on the bus this may lead to residual voltages while the microcontroller is not supplied.

CAN-transceiver without reverse protection show the backward current through an unprotected CAN-biasing net to the unpowered microcontroller-supply (V_{DD}). In a carnetwork the CAN-bus is expected to be always supplied even while the microcontroller is not.

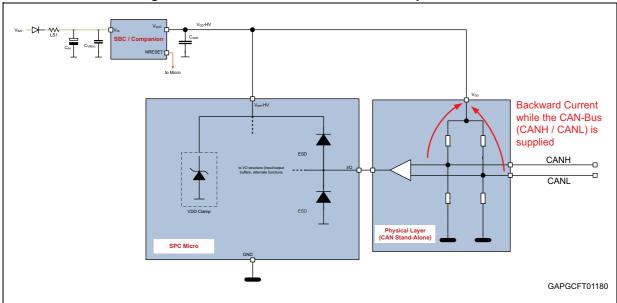


Figure 23. CAN-transceiver without reverse protection

Reference documents AN4218

Appendix A Reference documents

1. 32-bit Power Architecture[®] based MCU for automotive powertrain applications (SPC560P34x, SPC560P40x — Doc ID 18078)

- 2. 32-bit MCU family built on the embedded Power Architecture[®] (SPC564A74B4, SPC564A74L7, SPC564A80B4, SPC564A80L7 Doc ID 15399)
- 3. 32-bit MCU family built on the Power Architecture[®] for automotive body electronics applications (SPC560D30x, SPC560D40x Doc ID 16315)
- 4. 32-bit MCU family built on the Power Architecture[®] for automotive body electronics applications (SPC560B40x, SPC560B50x, SPC560C40x, SPC560C50x Doc ID 14619)
- 5. 32-bit MCU family built on the Power Architecture[®] for automotive body electronics applications (SPC560B54x, SPC560B60x, SPC560B64x Doc ID 15131)
- 6. 32-bit MCU family built on the Power Architecture[®] for automotive body electronics applications (SPC564Bxx, SPC56ECxx Doc ID 17478)
- 7. 32-bit Power Architecture® microcontroller for automotive SIL3/ASILD chassis and safety applications (SPC56EL60x, SPC56EL54x, SPC564L60x, SPC564L54x Doc ID 15457)
- 8. 32-bit Power Architecture[®] microcontroller for automotive SIL3/ASILD chassis and safety applications (SPC56EL70L3, SPC56EL70L5, SPC564L70L3, SPC564L70L5 Doc ID 023953)
- 9. 32-bit Power Architecture[®] based MCU with 320 KB Flash memory and 20 KB RAM for automotive chassis and safety applications (SPC560P34L1, SPC560P34L3, SPC560P40L1, SPC560P40L3 Doc ID 16100)
- 32-bit Power Architecture[®] based MCU with 576 KB Flash memory and 40 KB SRAM for automotive chassis and safety applications(SPC560P44L3, SPC560P44L5, SPC560P50L3, SPC560P50L5 Doc ID 14723)
- 11. 32-bit Power Architecture[®] based MCU with 1088 KB Flash memory and 80 KB RAM for automotive chassis and safety applications (SPC56AP60x, SPC56AP54x, SPC560P60x, SPC560P54x Doc ID 18340)
- 12. 32-bit Power Architecture[®] based MCU for automotive powertrain applications (SPC563M64L5, SPC563M64L7 Doc ID 14642)
- 13. Power management IC with LIN and high speed CAN (L99PM62GXP, Doc ID 15136)
- 14. ISO 7637-2:2011(E)
- 15. ISO16750-2:2006
- 16. BMW GS95024-2-1
- 17. Renault 36-00-808 / 2010
- 18. VW 80000: 2009-10

AN4218 Revision history

Revision history

Table 3. Document revision history

Date	Revision	Changes
04-Mar-2013	1	Initial release.
17-Sep-2013	2	Updated Disclaimer.

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