

Product Summary

V _{(BR)DSS}	R _{DS(ON)} max	I _D max T _A = +25°C
40V	12mΩ @ V _{GS} = 10V	11.5A
	15mΩ @ V _{GS} = 4.5V	10.3A

Description and Applications

This MOSFET has been designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Backlighting
- Power Management Functions
- DC-DC Converters

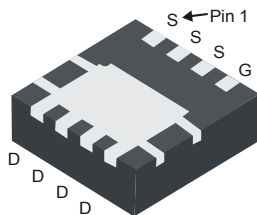
Features and Benefits

- Low R_{DS(ON)} – ensures on state losses are minimized
- Small form factor thermally efficient package enables higher density end products
- Occupies just 33% of the board area occupied by SO-8 enabling smaller end product
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

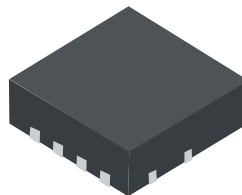
Mechanical Data

- Case: POWERDI 3333-8
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208③
- Weight: 0.072 grams (approximate)

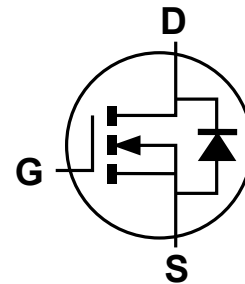
POWERDI 3333-8



Bottom View



Top View



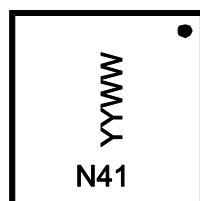
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMN4010LFG-7	POWERDI 3333-8	2000/Tape & Reel
DMN4010LFG-13	POWERDI 3333-8	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
 3. Halogen- and Antimony-free “Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



N41= Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last digit of year (ex: 13 = 2013)
 WW = Week code (01 ~ 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	40	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	11.5 9.2	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	14.2 11.4	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	2	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	80	A
Avalanche Current (Note 7) $L = 0.1\text{mH}$			I_{AS}	27	A
Avalanche Energy (Note 7) $L = 0.1\text{mH}$			E_{AS}	37	mJ

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Total Power Dissipation (Note 5)			P_D	0.93	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state		$R_{\theta JA}$	137	$^\circ\text{C/W}$
	$t < 10\text{s}$			89	
Total Power Dissipation (Note 6)			P_D	2.45	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state		$R_{\theta JA}$	52	$^\circ\text{C/W}$
	$t < 10\text{s}$			34	
Thermal Resistance, Junction to Case (Note 6)			$R_{\theta JC}$	3	
Operating and Storage Temperature Range			T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

- Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate
 7. I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep $T_J = 25^\circ\text{C}$

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	40	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	1	μA	V _{DS} = 32V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	1.0	—	3.0	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(on)}	—	—	12	mΩ	V _{GS} = 10V, I _D = 14A
		—	—	15		V _{GS} = 4.5V, I _D = 11A
Diode Forward Voltage	V _{SD}	—	0.72	—	V	V _{GS} = 0V, I _S = 14A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iSS}	—	1810	—	pF	V _{DS} = 20V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	135	—	pF	
Reverse Transfer Capacitance	C _{rSS}	—	112	—	pF	
Gate Resistance	R _g	—	1.7	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	17	—	nC	V _{DS} = 20V, I _D = 14A
Total Gate Charge (V _{GS} = 10V)	Q _g	—	37	—	nC	
Gate-Source Charge	Q _{gs}	—	5.6	—	nC	
Gate-Drain Charge	Q _{gd}	—	7.1	—	nC	
Turn-On Delay Time	t _{D(on)}	—	5.1	—	ns	V _{GS} = 10V, V _{DS} = 20V, R _G = 6Ω, I _D = 14A
Turn-On Rise Time	t _r	—	13	—	ns	
Turn-Off Delay Time	t _{D(off)}	—	36	—	ns	
Turn-Off Fall Time	t _f	—	13	—	ns	
Body Diode Reverse Recovery Time	t _{rr}	—	12.2	—	nS	I _F = 3A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q _{rr}	—	5.4	—	nC	I _F = 3A, di/dt = 100A/μs

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

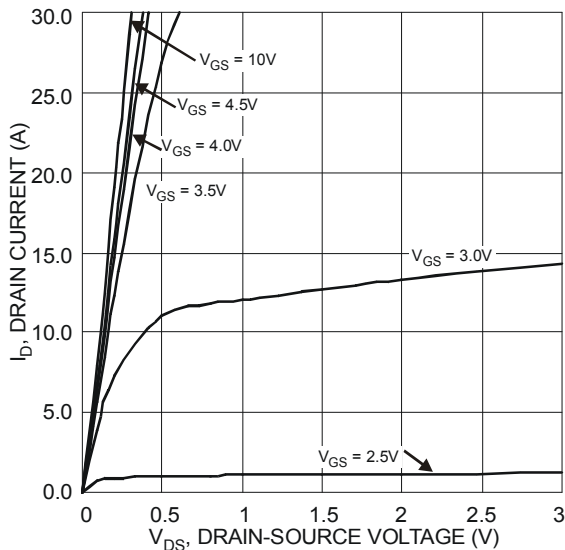


Figure 1 Typical Output Characteristic

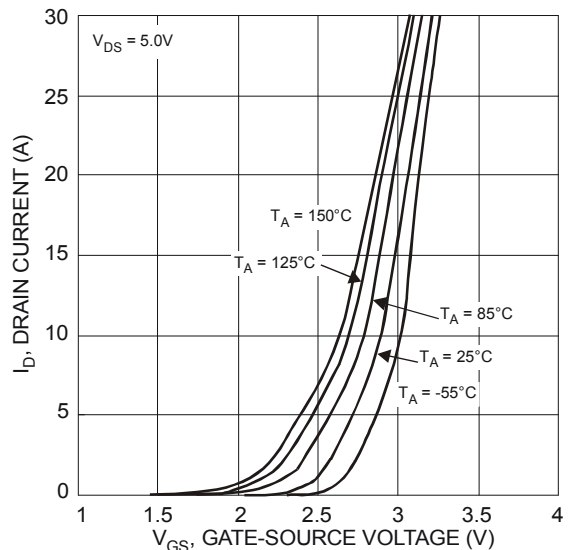


Figure 2 Typical Transfer Characteristics

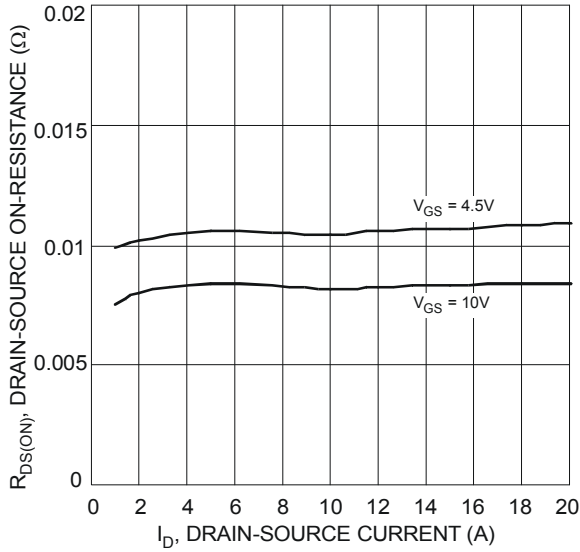


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

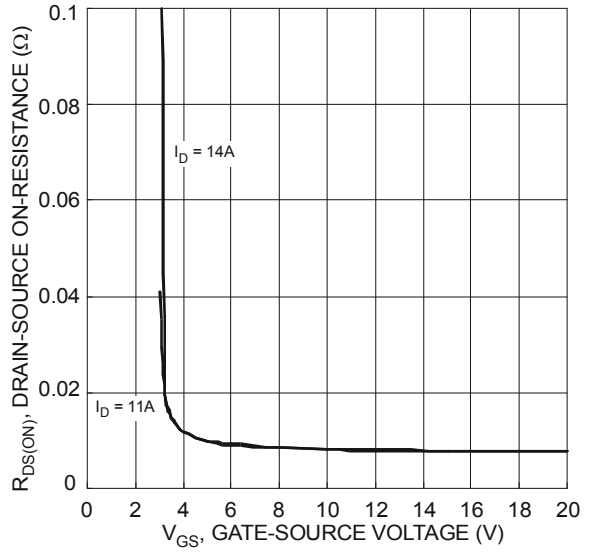


Figure 4 Typical Transfer Characteristic

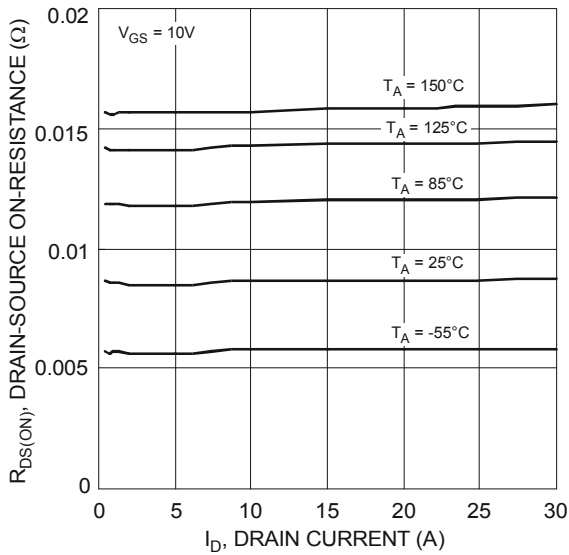


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

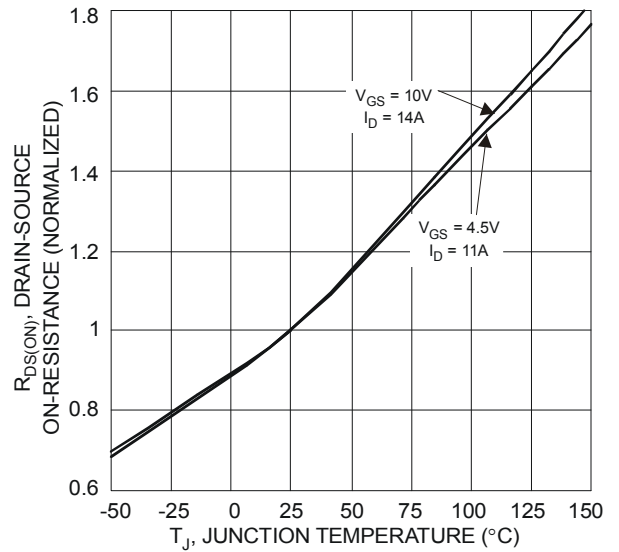


Figure 6 On-Resistance Variation with Temperature

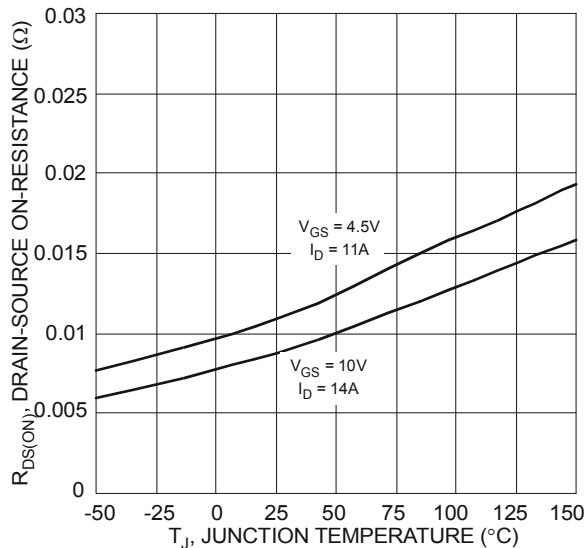


Figure 7 On-Resistance Variation with Temperature

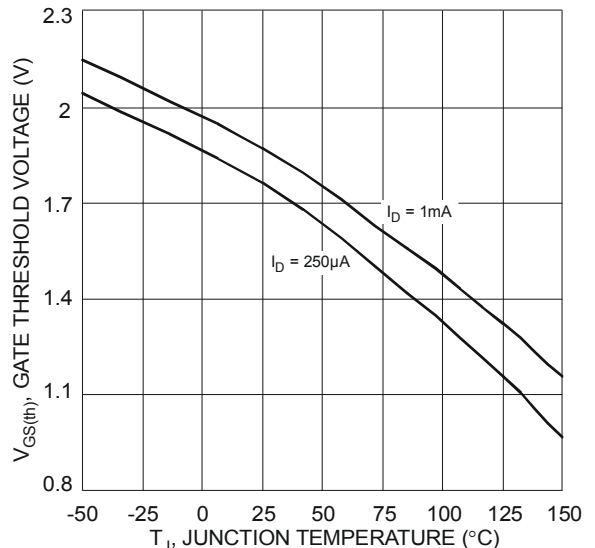


Figure 8 Gate Threshold Variation vs. Ambient Temperature

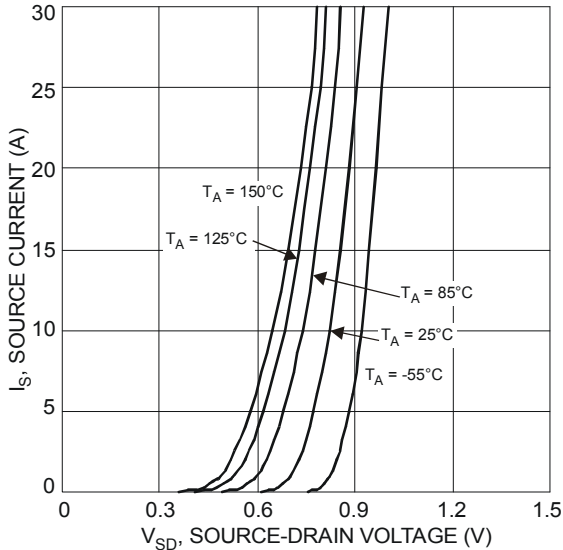


Figure 9 Diode Forward Voltage vs. Current

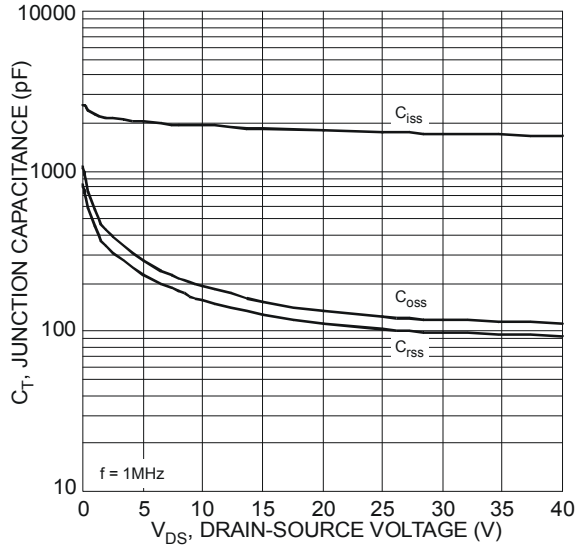


Figure 10 Typical Junction Capacitance

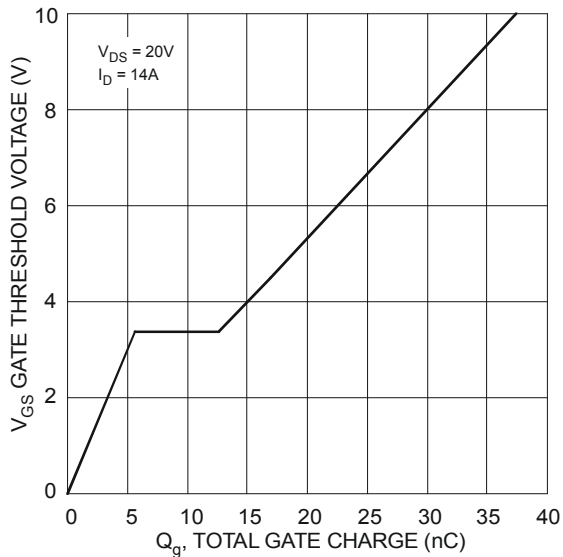


Figure 11 Gate Charge

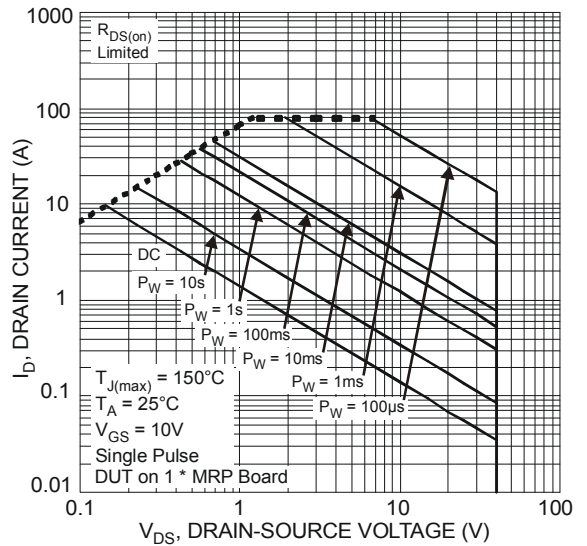


Figure 12 SOA, Safe Operation Area

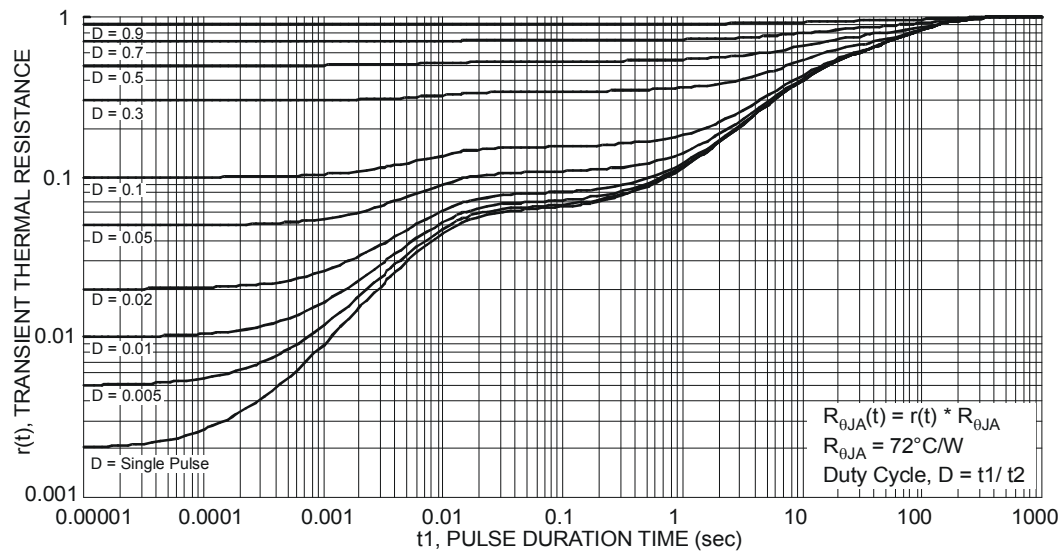
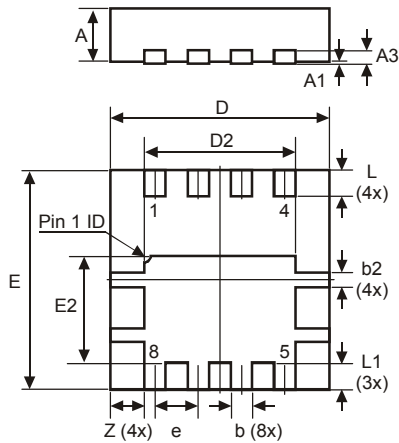


Figure 13 Transient Thermal Resistance

Package Outline Dimensions

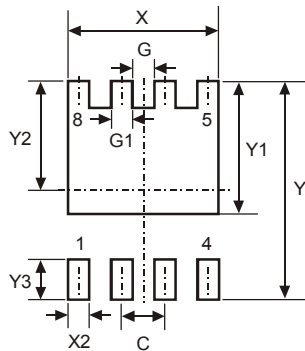
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



POWERDI® 3333-8			
Dim	Min	Max	Typ
D	3.25	3.35	3.30
E	3.25	3.35	3.30
D2	2.22	2.32	2.27
E2	1.56	1.66	1.61
A	0.75	0.85	0.80
A1	0	0.05	0.02
A3	-	-	0.203
b	0.27	0.37	0.32
b2	-	-	0.20
L	0.35	0.45	0.40
L1	-	-	0.39
e	-	-	0.65
Z	-	-	0.515
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
C	0.650
G	0.230
G1	0.420
Y	3.700
Y1	2.250
Y2	1.850
Y3	0.700
X	2.370
X2	0.420

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