

CAT5112

32-tap Digital Potentiometer (POT) with Buffered Wiper

Description

The CAT5112 is a single digital POT designed as an electronic replacement for mechanical potentiometers. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5112 contains a 32-tap series resistor array connected between two terminals R_H and R_L . An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_{WB} . The CAT5112 wiper is buffered by an op amp that operates rail to rail. The wiper setting, stored in non-volatile memory, is not lost when the device is powered down and is automatically recalled when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting. Wiper-control of the CAT5112 is accomplished with three input control pins, \overline{CS} , U/\overline{D} , and \overline{INC} . The \overline{INC} input increments the wiper in the direction which is determined by the logic state of the U/\overline{D} input. The \overline{CS} input is used to select the device and also store the wiper position prior to power down.

The digital POT can be used as a buffered voltage divider. For applications where the potentiometer is used as a 2-terminal variable resistor, please refer to the CAT5114. The buffered wiper of the CAT5112 is not compatible with that application.

Features

- 32-position Linear Taper Potentiometer
- Non-volatile EEPROM Wiper Storage; Buffered Wiper
- Low Power CMOS Technology
- Single Supply Operation: 2.5 V – 6.0 V
- Increment Up/Down Serial Interface
- Resistance Values: 10 k Ω , 50 k Ω and 100 k Ω
- Available in PDIP, SOIC, TSSOP and MSOP Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automated Product Calibration
- Remote Control Adjustments
- Offset, Gain and Zero Control
- Tamper-proof Calibrations
- Contrast, Brightness and Volume Controls
- Motor Controls and Feedback Systems
- Programmable Analog Functions



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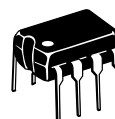
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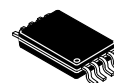
SOIC-8
V SUFFIX
CASE 751BD



MSOP-8
Z SUFFIX
CASE 846AD

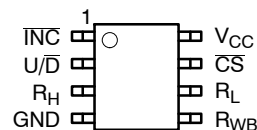


PDIP-8
L SUFFIX
CASE 646AA

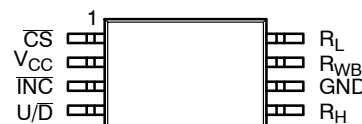


TSSOP-8
Y SUFFIX
CASE 948AL

PIN CONFIGURATIONS



PDIP (L), SOIC (V), MSOP (Z)



TSSOP (Y)
(Top Views)

PIN FUNCTION

Pin Name	Function
\overline{INC}	Increment Control
U/\overline{D}	Up/Down Control
R_H	Potentiometer High Terminal
GND	Ground
R_{WB}	Buffered Wiper Terminal
R_L	Potentiometer Low Terminal
\overline{CS}	Chip Select
V_{CC}	Supply Voltage

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

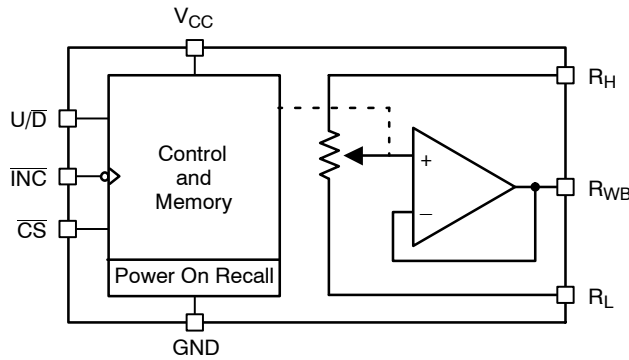


Figure 1. Functional Diagram

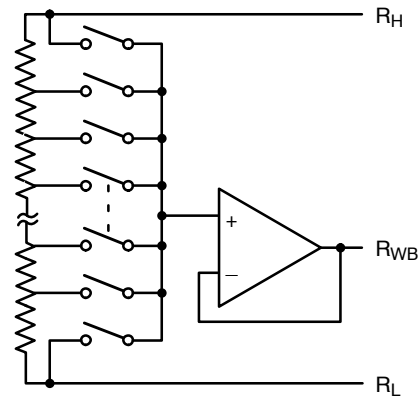


Figure 2. Electronic Potentiometer Implementation

Pin Description

INC: Increment Control Input

The INC input (on the falling edge) moves the wiper in the up or down direction determined by the condition of the U/D input.

U/D: Up/Down Control Input

The U/D input controls the direction of the wiper movement. When in a high state and CS is low, any high-to-low transition on INC will cause the wiper to move one increment toward the RH terminal. When in a low state and CS is low, any high-to-low transition on INC will cause the wiper to move one increment towards the RL terminal.

RH: High End Potentiometer Terminal

RH is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the RL terminal. Voltage applied to the RH terminal cannot exceed the supply voltage, VCC or go below ground, GND.

RWB: Wiper Potentiometer Terminal (Buffered)

RWB is the buffered wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, INC, U/D and CS.

RL: Low End Potentiometer Terminal

RL is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the RH terminal. Voltage applied to the RL terminal cannot exceed the supply voltage, VCC or go below ground, GND. RL and RH are electrically interchangeable.

CS: Chip Select

The chip select input is used to activate the control input of the CAT5112 and is active low. When in a high state, activity on the INC and U/D inputs will not affect or change the position of the wiper.

Device Operation

The CAT5112 operates like a digitally controlled potentiometer with RH and RL equivalent to the high and low terminals and RWB equivalent to the mechanical potentiometer's wiper. There are 32 available tap positions including the resistor end points, RH and RL. There are 31 resistor elements connected in series between the RH and RL terminals. The wiper terminal is connected to one of the 32 taps and controlled by three inputs, INC, U/D and CS. These inputs control a five-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the INC and CS inputs.

With CS set LOW the CAT5112 is selected and will respond to the U/D and INC inputs. HIGH to LOW transitions on INC will increment or decrement the wiper (depending on the state of the U/D input and five-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever CS transitions HIGH while the INC input is also HIGH. When the CAT5112 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With INC set low, the CAT5112 may be deselected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

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Table 1. OPERATION MODES

INC	CS	U/D	Operation
High to Low	Low	High	Wiper toward R _H
High to Low	Low	Low	Wiper toward R _L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby

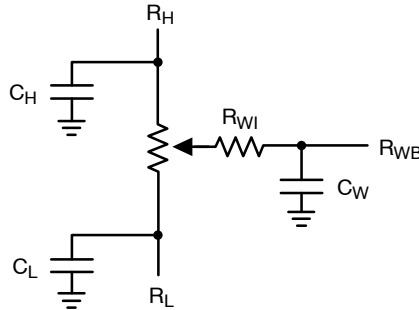


Figure 3. Potentiometer Equivalent Circuit

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage V _{CC} to GND	-0.5 to +7	V
Inputs CS to GND	-0.5 to V _{CC} +0.5	V
INC to GND	-0.5 to V _{CC} +0.5	V
U/D to GND	-0.5 to V _{CC} +0.5	V
R _H to GND	-0.5 to V _{CC} +0.5	V
R _L to GND	-0.5 to V _{CC} +0.5	V
R _{WB} to GND	-0.5 to V _{CC} +0.5	V
Operating Ambient Temperature Commercial ('C' or Blank suffix)	0 to 70	°C
Industrial ('I' suffix)	-40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	-65 to +150	°C
Lead Soldering (10 s max)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V _{ZAP} (Note 1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			V
I _{LTH} (Notes 1, 2)	Latch-Up	JEDEC Standard 17	100			mA
T _{DR}	Data Retention	MIL-STD-883, Test Method 1008	100			Years
N _{END}	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1 V to V_{CC} + 1 V

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Table 4. DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +2.5\text{ V}$ to $+6\text{ V}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range		2.5	–	6	V
I_{CC1}	Supply Current (Increment)	$V_{CC} = 6\text{ V}$, $f = 1\text{ MHz}$, $I_W = 0$	–	–	200	μA
		$V_{CC} = 6\text{ V}$, $f = 250\text{ kHz}$, $I_W = 0$	–	–	100	μA
I_{CC2}	Supply Current (Write)	Programming, $V_{CC} = 6\text{ V}$	–	–	1000	μA
		$V_{CC} = 3\text{ V}$	–	–	500	μA
I_{SB1} (Note 4)	Supply Current (Standby)	$\overline{CS} = V_{CC} - 0.3\text{ V}$ U/\overline{D} , $\overline{INC} = V_{CC} - 0.3\text{ V}$ or GND	–	75	150	μA
LOGIC INPUTS						
I_{IH}	Input Leakage Current	$V_{IN} = V_{CC}$	–	–	10	μA
I_{IL}	Input Leakage Current	$V_{IN} = 0\text{ V}$	–	–	–10	μA
V_{IH1}	TTL High Level Input Voltage	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	2	–	V_{CC}	V
V_{IL1}	TTL Low Level Input Voltage		0	–	0.8	V
V_{IH2}	CMOS High Level Input Voltage	$2.5\text{ V} \leq V_{CC} \leq 6\text{ V}$	$V_{CC} \times 0.7$	–	$V_{CC} + 0.3$	V
V_{IL2}	CMOS Low Level Input Voltage		–0.3	–	$V_{CC} \times 0.2$	V
POTENTIOMETER CHARACTERISTICS						
R_{POT}	Potentiometer Resistance	–10 Device		10		k Ω
		–50 Device		50		
		–00 Device		100		
	Pot. Resistance Tolerance				± 20	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
	Resolution			1		%
INL	Integral Linearity Error	$I_W \leq 2\ \mu\text{A}$		0.5	1	LSB
DNL	Differential Linearity Error	$I_W \leq 2\ \mu\text{A}$		0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance	$0.05\ V_{CC} \leq V_{WB} \leq 0.95\ V_{CC}$, $V_{CC} = 5\text{ V}$			1	Ω
I_{OUT}	Buffer Output Current	$0.05\ V_{CC} \leq V_{WB} \leq 0.95\ V_{CC}$, $V_{CC} = 5\text{ V}$			3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/ $^{\circ}\text{C}$
TC_{RATIO}	Ratiometric TC			20		ppm/ $^{\circ}\text{C}$
$C_{RH}/C_{RL}/C_{RW}$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10 k Ω		1.7		MHz
$V_{WB(SWING)}$	Output Voltage Range	$I_{OUT} \leq 100\ \mu\text{A}$, $V_{CC} = 5\text{ V}$	$0.01\ V_{CC}$		$0.99\ V_{CC}$	

3. This parameter is tested initially and after a design or process change that affects the parameter.
4. Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1 V to $V_{CC} + 1\text{ V}$
5. I_W = source or sink
6. These parameters are periodically sampled and are not 100% tested.

Table 5. AC TEST CONDITIONS

V _{CC} Range	2.5 V ≤ V _{CC} ≤ 6 V
Input Pulse Levels	0.2 V _{CC} to 0.7 V _{CC}
Input Rise and Fall Times	10 ns
Input Reference Levels	0.5 V _{CC}

Table 6. AC OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +6.0 V, V_H = V_{CC}, V_L = 0 V, unless otherwise specified)

Symbol	Parameter	Min	Typ (Note 7)	Max	Units
t _{CI}	CS to INC Setup	100	-	-	ns
t _{DI}	U/D to INC Setup	50	-	-	ns
t _{ID}	U/D to INC Hold	100	-	-	ns
t _{IL}	INC LOW Period	250	-	-	ns
t _{IH}	INC HIGH Period	250	-	-	ns
t _{IC}	INC Inactive to CS Inactive	1	-	-	μs
t _{CPH}	CS Deselect Time (NO STORE)	100	-	-	ns
t _{CPH}	CS Deselect Time (STORE)	10	-	-	ms
t _{IW}	INC to V _{OUT} Change	-	1	5	μs
t _{CYC}	INC Cycle Time	1	-	-	μs
t _R , t _F (Note 8)	INC Input Rise and Fall Time	-	-	500	μs
t _{PU} (Note 8)	Power-up to Wiper Stable	-	-	1	ms
t _{WR}	Store Cycle	-	5	10	ms

7. Typical values are for T_A = 25°C and nominal supply voltage.

8. This parameter is periodically sampled and not 100% tested.

9. MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

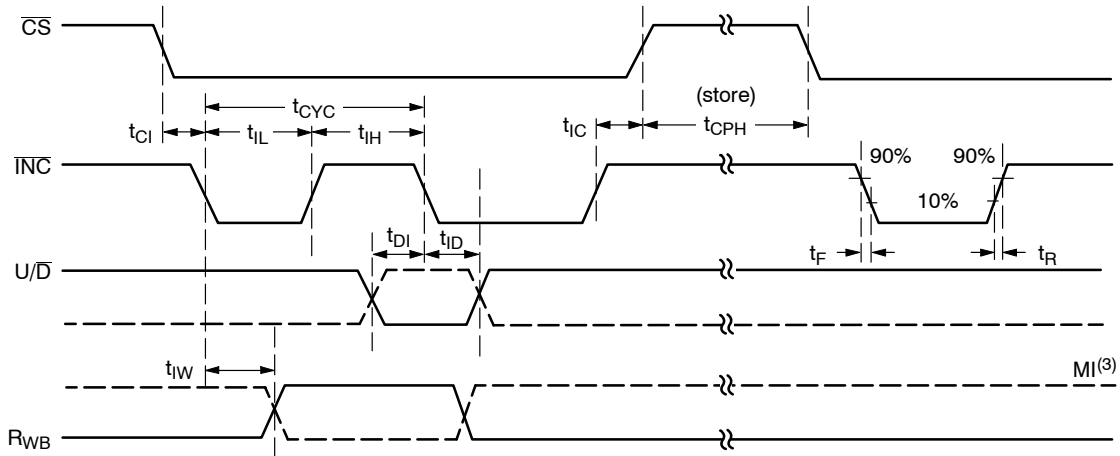
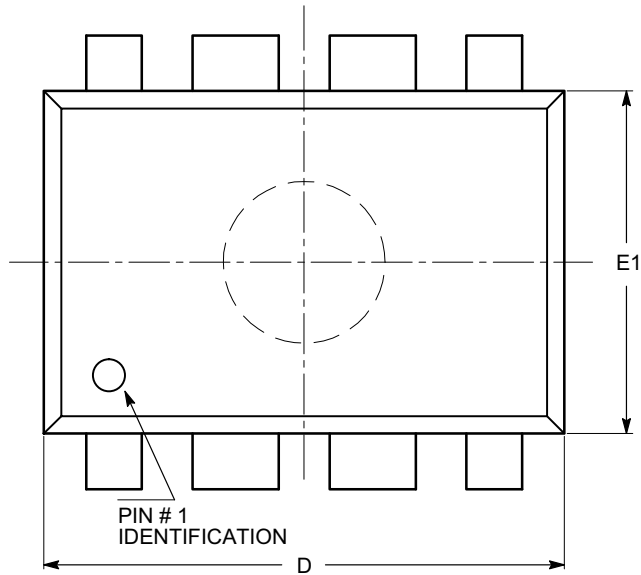


Figure 4. A.C. Timing

CAT5112

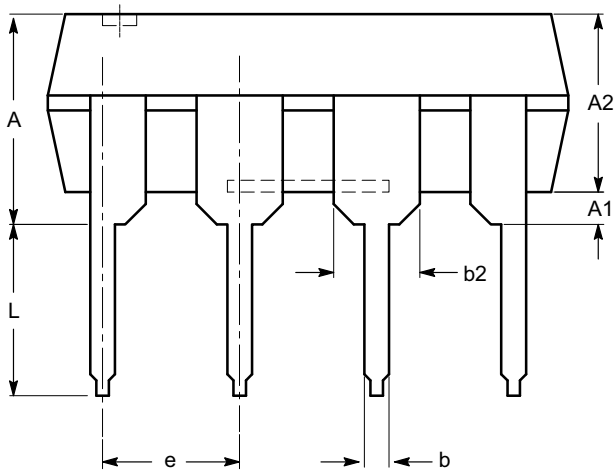
PACKAGE DIMENSIONS

PDIP-8, 300 mils
CASE 646AA
ISSUE A

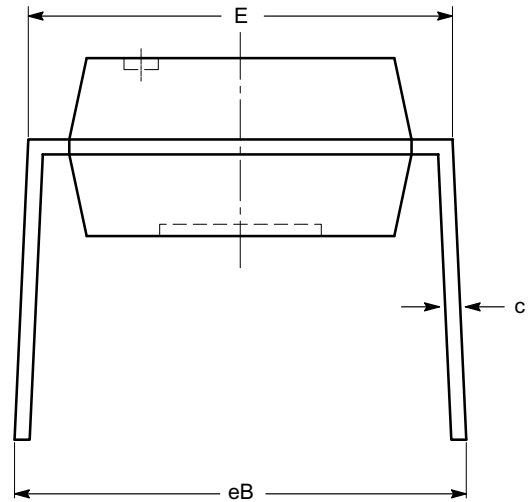


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e	2.54 BSC		
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW



END VIEW

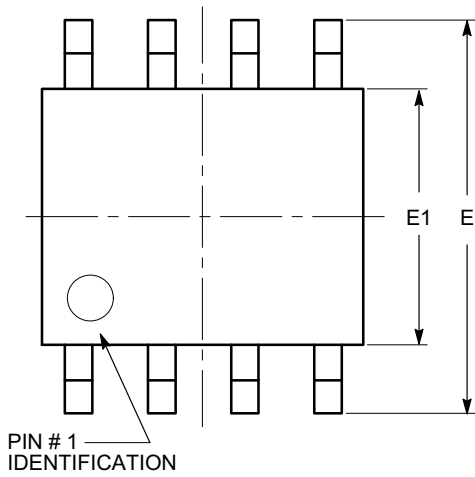
Notes:

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.

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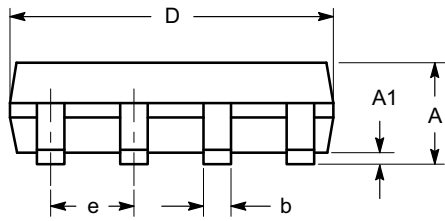
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD
ISSUE O

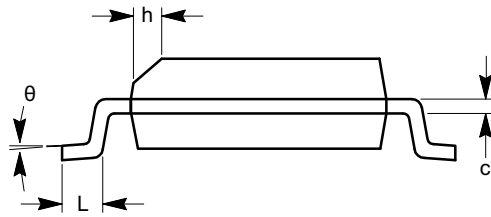


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

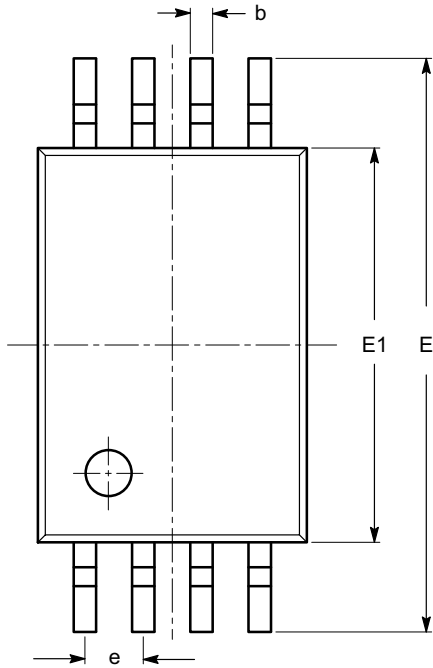
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- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

CAT5112

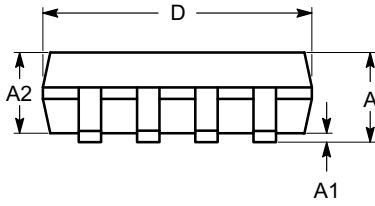
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL
ISSUE O

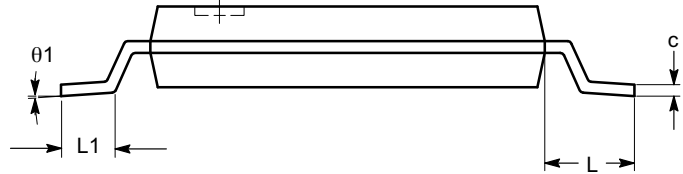


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

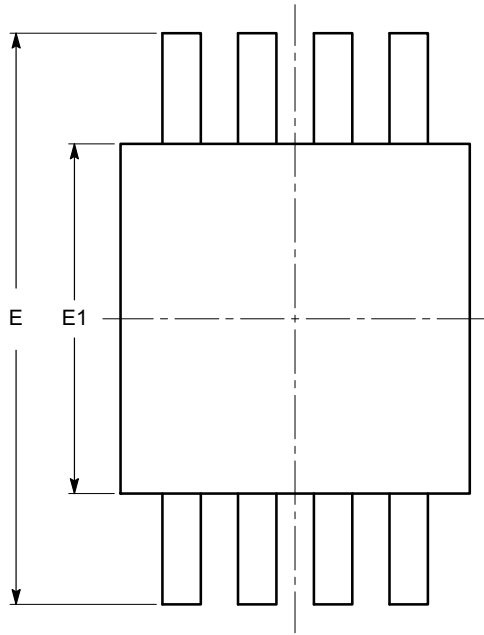
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- (2) Complies with JEDEC MO-153.

CAT5112

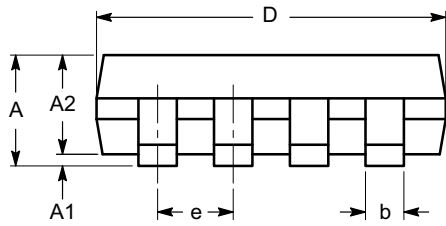
PACKAGE DIMENSIONS

MSOP 8, 3x3
CASE 846AD
ISSUE O

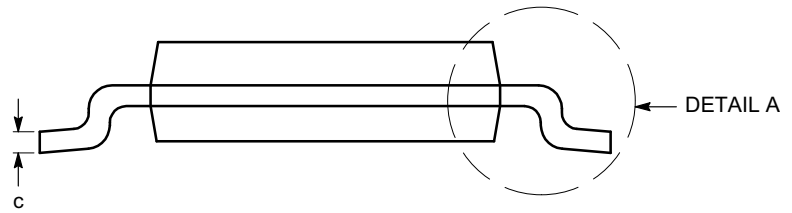


TOP VIEW

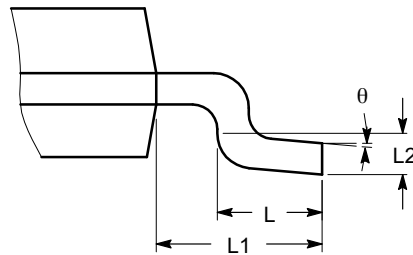
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°		6°



SIDE VIEW



END VIEW



DETAIL A

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-187.


CAT5112

Table 7. ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping [†]
CAT5112VI-10-GT3	CAT5112V	SOIC-8	-40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT5112VI-50-GT3	CAT5112V	SOIC-8	-40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT5112VI-00-GT3	CAT5112V	SOIC-8	-40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT5112YI-10-GT3	A22	TSSOP-8	-40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT5112YI-50-GT3	A24	TSSOP-8	-40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT5112YI-00-GT3	A25	TSSOP-8	-40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT5112ZI-10-GT3	ABPN	MSOP-8	-40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT5112ZI-50-GT3	ABPN	MSOP-8	-40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT5112ZI-00-GT3	ABPN	MSOP-8	-40°C to +85°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT5112LI-10-G	CAT5112L	PDIP-8	-40°C to +85°C	NiPdAu	Rail, 50 Units
CAT5112LI-50-G	CAT5112L	PDIP-8	-40°C to +85°C	NiPdAu	Rail, 50 Units
CAT5112LI-00-G	CAT5112L	PDIP-8	-40°C to +85°C	NiPdAu	Rail, 50 Units

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

10. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

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