Advance Information

MPC855TTS/D
Rev. 0.1, 11/2001

MPC855T Communications Controller Technical Summary

The MPC855T communications controller is a member of the MPC8xx family targeted at cost sensitive general purpose networking controller applications. The MPC855T can be used in a variety of controller applications, excelling particularly in low cost communications and networking products, such as SOHO routers, ADSL, and cable modems.

The MPC855T integrates three separate processing blocks. The first two, common with all MPC8xx devices, are (1) a high-performance MPC8xx core, which is used as a general-purpose processor for application programming and (2) a RISC communications processor (CP) embedded in the communications processor module (CPM). All MPC8xx devices will have an 8-KByte dual port RAM when the MPC855T is available. The third block is a 10/100-Mbps Fast Ethernet controller with integrated FIFOs and bursting DMA. The MPC855T's Fast Ethernet controller is implemented independently, providing high-performance Fast Ethernet connectivity without affecting the performance of the CPM.

Additionally, since the CPM of the MPC855T is based on the CPM of other MPC8xx devices, support for ATM, HDLC, and the QMC (QUICC multichannel controller) multichannel protocol is also provided. The QMC protocol enables the MPC855T to provide protocol processing (through HDLC or transparent mode) for 32 time-division-multiplexed channels (on TDM channel A) when the MPC855T is operated at 50 MHz. This support for multichannel protocol processing, ATM and 10/100-Mbps Ethernet in one chip makes the MPC855T ideal for cost sensitive networking and telecommunications systems.

1.1 MPC855T Key Features

The key features of the MPC855T are summarized as follows:

- 10/100-Mbps Ethernet support (Not available when using ATM over UTOPIA interface)
  - — Full compliance with the IEEE 802.3u standard for 10/100-Mbps
  - — Support for three different physical interfaces
    - – 100-Mbps 802.3 media-independent interface (MII)
    - – 10-Mbps 802.3 media-independent interface
    - – 10-Mbps 7-wire interface
  - — Support for half-duplex 100-Mbps operation (at 33-MHz system clock rate and above)
  - — Support for full-duplex 100-Mbps operation (at 50-MHz system clock rate and

above)

- — Large on-chip transmit and receive FIFOs to support a variety of bus latencies
- — Retransmission from transmit FIFO following a collision
- — Automatic internal flushing of the receive FIFO for runts and collisions
- — Off-chip buffer descriptor rings of user-definable size that allow nearly unlimited flexibility in management of transmit and receive buffer memory

• 10/100-Mbps media access control (MAC) features
- — Address recognition
  - – Broadcast
  - – Single station address
  - – Promiscuous mode
  - – Multicast hashing
- — Full support of the media-independent interface
- — Interrupt modes
  - – Per-frame
  - – Per-buffer (selectable buffer interrupt functionality using the I bit is not supported)
- — Automatic interrupt vector generation for receive and transmit events

  Categories: transmit interrupt, receive interrupt, non-time critical interrupt
- — Ethernet channel bursts data to/from external memory

• ATM support
- — Compliant with ATM forum UNI 4.0 specification
- — Cell processing up to 50–70 Mbps at 50-MHz system clock
- — Cell multiplexing/demultiplexing
- — Support of AAL5 and AAL0 protocols on a per-VC basis
  - – AAL0 support enables OAM and software implementation of other protocols)
- — ATM pace control (APC) scheduler, providing:
  - – Direct support of constant bit rate (CBR)
  - – Direct support of unspecified bit rate (UBR)
  - – Control mechanisms enabling software support of available bit rate (ABR)
- — Support for two types of physical interfaces
  - – UTOPIA (10/100-Mbps is not supported with this interface)
  - – Byte-aligned serial (e.g. T1/E1/ADSL)
- — UTOPIA-mode ATM supports:
  - – UTOPIA level 1 master with cell-level handshake
  - – Multi-PHY (up to 4 physical layer devices)
  - – Connection to 25 Mbps, 51 Mbps, or 155 Mbps framers
  - – UTOPIA clock rates of 1:2 or 1:3 system clock rates
- — Serial-mode ATM connection supports:

  - Transmission convergence (TC) function for T1/E1/ADSL lines
  - Cell delineation
  - Cell payload scrambling/descrambling
  - Automatic idle/unassigned cell insertion/stripping
  - Header error control (HEC) generation, checking, and statistics
  - Glueless interface to Motorola CopperGold ADSL transceiver
- Receive VP/VC connection lookup mechanisms, including:
  - Internal sequential lookup table supporting up to 32 connections
  - Support for up to 64K connections using external memory via address compression or content-addressable memory (CAM)
- Independent transmit/receive buffer descriptor ring data structures for each connection
- Interrupt report per channel using exception queue
- Supports 53-byte or up to 64-byte (expanded) ATM cells
- AAL5 segmentation and reassembly (SAR) features for segmentation
  - Segment CPCS_PDU directly from system memory
  - CPCS_PDU padding
  - CRC32 generation
  - Automatic last cell marking (in PTI field of cell header)
  - Automatic CS_UU, CPI, and LENGTH insertion in last cell
- AAL5 segmentation and reassembly (SAR) features for reassembly:
  - Reassembles CPCS_PDU directly into system memory
  - Removes CPCS_PDU padding
  - CRC32 checking
  - CS_UU, CPI, and LENGTH reporting
  - CLP and congestion reporting
  - Interrupts per buffer or per message
  - Error reporting, including CRC, length mismatch, message abort
- AAL0 features for transmit include the following:
  - Transmits user-defined cell from transmit emory buffer
  - Automatic HEC generation
  - Optional CRC10 insertion
- AAL0 features for receive include the following:
  - Copies entire cell into receive memory buffer
  - Provides interrupt per cell
  - Optional CRC10 checking

- Embedded MPC8xx core with 106 MIPS at 80 MHz (using Dhrystone 2.1)
  - Single-issue, 32-bit version of the embedded MPC8xx core (fully compatible with the PowerPC user instruction set architecture; refer to the *Programming Environments Manual for 32-Bit Implementations of the PowerPC Architecture* for more information) with 32- x 32-bit

fixed-point registers

- Embedded MPC8xx core performs branch folding and branch prediction with conditional prefetch, but without conditional execution
- 4-Kbyte data cache and 4-Kbyte instruction cache, each with an MMU
- Instruction and data caches are two-way, set associative, physical address, 4-word line burst, least recently used (LRU) replacement, lockable on cache line granularity
- MMUs with 32-entry, fully-associative instruction and data TLBs
- MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Kbytes; 16 virtual address spaces and 8 protection groups
- Advanced on-chip-emulation debug mode

— Up to 32-bit data bus (dynamic bus sizing of 8, 16, and 32 bits provided through memory controller)

— 32 address lines

• System integration unit (SIU)

— Bus monitor

— Spurious interrupt monitor

— Software watchdog

— Periodic interrupt timer

— Low-power stop mode

— Clock synthesizer

— Decrementer

— Time base and RTC

— Reset controller

— IEEE 1149.1 test access port (JTAG)

— Memory controller (eight bank)

- Contains complete dynamic random-access memory (DRAM) controller
- Each bank may be a chip select or RAS to support a DRAM bank
- Up to 15 wait states programmable per memory bank
- Glueless interface to DRAM single in-line memory modules (SIMMs), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), Flash EPROM, etc.
- DRAM controller programmable to support most size and speed memory interfaces
- Four CAS lines, four WE lines, one OE line
- Boot chip select available at reset (options for 8-, 16-, or 32-bit memory)
- Variable block sizes, 32 Kbytes to 256 Mbytes
- Selectable write protection
- On-chip bus arbitration logic

— General-purpose timers

- Four 16-bit timers or two 32-bit timers

  - Gate mode can enable/disable counting
  - Interrupt may be masked on reference match and event capture
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 13 internal interrupt sources
  - Programmable highest priority request
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports two independent PCMCIA sockets
  - 8 memory or I/O windows supported

- Communications Processor Module (CPM)
  - Supports all functionality and performance of MPC860T
  - RISC communications processor (CP)
  - Communication-specific commands (for example, graceful stop transmit, close receive buffer descriptor, RxBD)
  - Up to 384 buffer descriptors
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8 Kbytes of dual-port RAM
  - 10 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
  - Four baud rate generators
    - Independent
    - Baud rate changes allowed during operation
    - Autobaud support option
  - One SCC (serial communications controller)
    - QMC multichannel protocol for processing 32 time-division-multiplexed channels
    - Ethernet/IEEE 802.3u, supporting full 10-Mbps operation
    - HDLC/SDLC™ (all channels supported at 2 Mbps)
    - HDLC bus (implements an HDLC-based local area network (LAN))
    - Asynchronous HDLC supports PPP (point-to-point protocol)
    - AppleTalk™
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Serial infrared (IrDA)
    - Binary synchronous communication (BISYNC)
    - Totally transparent (bit streams)
    - Totally transparent (frame based with optional cyclic redundancy check (CRC))

- QMC multichannel features
  - Up to 32 independent communication channels on a single SCC
  - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
  - Supports either transparent or HDLC protocols for each channel
  - Independent transmit and receive buffer descriptors and event/interrupt reporting for each channel
- Two SMCs (serial management channels)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - May be connected to the time-division-multiplexed (TDM) channels
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One I^2C (inter-integrated circuit) port
  - Supports master and slave modes
  - Multimaster environment support
- Time slot assigner (TSA) supporting TDMa only
  - Allows SCC and SMCs to run in multiplexed and/or nonmultiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame syncs, clocking
  - Allows dynamic changes
  - May be internally connected to three serial channels (one SCC and two SMCs)
- Parallel interface port
  - Centronics™ interface support
  - Supports fast connection between compatible ports on MPC860 or MC68360
- Low power support
  - Full-on–all units fully powered
  - Doze–core functional units disabled except time base, decrementer, PLL, memory controller, RTC, and CPM in low-power standby
  - Sleep–all units disabled except RTC and PIT, PLL active for fast wake-up
  - Deep sleep–all units disabled including PLL except RTC and PIT
  - Low-power STOP mode provides lowest power dissipation
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a breakpoint internally

— 3.3-V operation (No support for 5V I/O)

— 357-pin ball grid array (BGA) package

1.2 MPC855T Architecture Overview

The MPC855T is comprised of four modules connected to the 32-bit internal bus: the embedded MPC8xx core, the system integration unit (SIU), the communications processor module (CPM), and the Fast Ethernet controller (FEC). The MPC855T block diagram is shown in Figure 1.

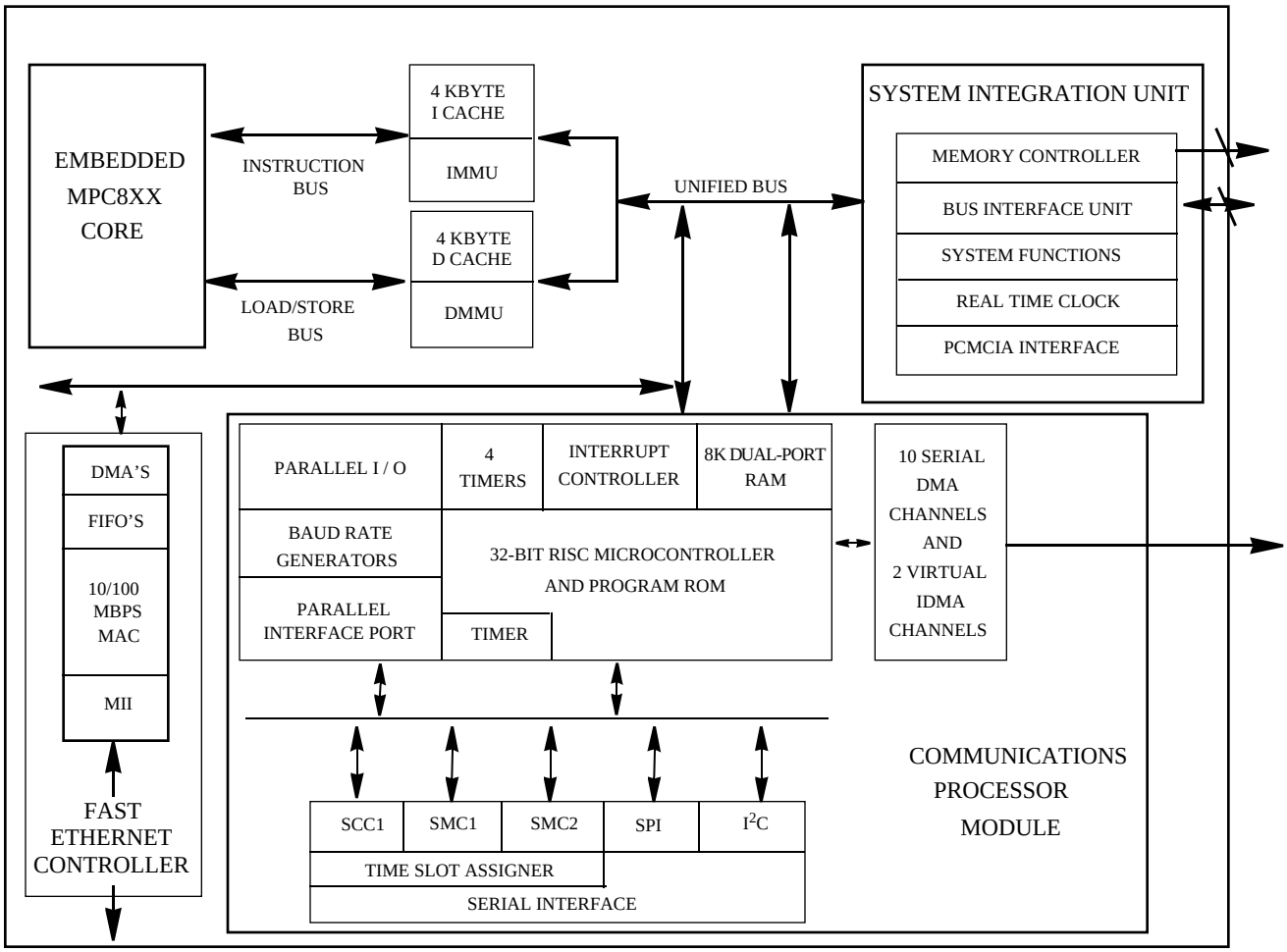

Figure 1. MPC855T Block Diagram

1.2.1 Embedded MPC8xx Core

The embedded MPC8xx core is compliant with the PowerPC user instruction set architecture; refer to *Programming Environments Manual for 32-Bit Implementations of the PowerPC Architecture* for more information. The embedded MPC8xx core is a fully-static design that consists of two functional units—the integer unit and the load/store unit. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. The core interface to the internal and external buses is 32 bits. The core uses a two-instruction load/store queue, a four- instruction prefetch queue, and a six-instruction history buffer. The core performs branch folding and

branch prediction with conditional prefetch, but without conditional execution. The embedded core can operate on 32-bit external operands with one bus cycle.

The integer unit supports 32- x 32-bit fixed-point general-purpose registers. It can execute one integer instruction each clock cycle. Each element in the integer unit is clocked only when valid data is present in the data queue ready for operation. This assures that the power consumption of the device is held to the absolute minimum required to perform an operation.

The embedded core is integrated with MMUs as well as 4-Kbyte instruction and data caches. Each MMU provides a 32-entry, fully-associative instruction and data TLB, with multiple page sizes of: 4 Kbytes, 16 Kbytes, 512 Kbytes, 256 Kbytes, and 8 Mbytes. It supports 16 virtual address spaces with 8 protection groups. Three special registers are available as scratch registers to support software tablewalk and update.

The instruction cache is 4 Kbytes, two-way, set associative with physical addressing. It allows single-cycle access on hit with no added latency for miss. It has four words per line, and supports burst linefill using least recently used (LRU) replacement. The cache may be locked on a per-line basis for application-critical routines.

The data cache is 4 Kbytes, two-way, set associative with physical addressing. It allows single-cycle access on hit with one added clock latency for miss. It has four words per line, supporting burst linefill using LRU replacement. The cache may be locked on a per-line basis for application-critical routines. The data cache can be programmed to support copy-back or write-through via the MMU. The cache-inhibit mode can be programmed per MMU page.

The embedded core with its instruction and data caches delivers approximately 106 MIPS at 80 MHz, using Dhrystone 2.1, based on the assumption that it is issuing one instruction per cycle with a cache hit rate of 94%.

The embedded core provides a much improved debug interface that operates without causing any degradation in the speed of user operations. This interface supports six watchpoint signals that are used to detect software events. Internally the MPC855T has eight comparators, four of which operate on the effective address on the address bus. The remaining four comparators are split, with two comparators operating on the effective address on the data bus, and two comparators operating on the data on the data bus. The embedded core can compare using =, ≠, <, > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger in a programmable number of events.

1.2.2 Fast Ethernet Controller (FEC)

The Fast Ethernet controller on the MPC855T is compliant with the IEEE 802.3u specification for 10-Mbps and 100-Mbps connectivity. Full-duplex 100-Mbps operation is supported at system clock rates of 50 MHz and higher. A 33-MHz system clock supports 10-Mbps operation or half-duplex 100-Mbps operation.

The Fast Ethernet controller provides greatly reduced bus utilization through the use of bursting DMA. Optimization of bus utilization allows the MPC855T to be used in systems with low-cost memories such as synchronous DRAM.

Transmit and receive FIFOs further reduce bus utilization by localizing all collisions to the Fast Ethernet controller. On the transmit side, a full collision window of transmit frame data is maintained in the FIFO, eliminating the need for repeated DMA over the system bus in the event of a collision. On the receive side, a full collision window of data is received before any receive data is transferred into system memory, allowing the FIFO to be flushed in the event of a runt or collided frame, with no DMA activity. However, external memory for data buffers and buffer descriptors is required; on-chip FIFOs are only designed to compensate for collisions and for system bus latency.

Independent transmit and receive buffer descriptor rings located in external memory allow nearly unlimited flexibility in memory management of transmit and receive data frames. Locating buffer descriptors in external memory has two advantages—first, external memory (i.e., DRAM) is low cost; secondly, descriptor rings in external memory have no inherent size limitations, allowing the memory management to be optimized according to specific system needs.

1.2.3 System Interface Unit (SIU)

The SIU on the MPC855T integrates general-purpose features useful in almost any 32-bit processor system, enhancing the performance provided by the system integration module (SIM) on the MC68360 QUICC device.

Although the embedded MPC8xx core is always a 32-bit device internally, it may be configured to operate with an 8-, 16- or 32-bit data bus. Regardless of the choice of the system bus size, dynamic bus sizing is supported. Bus sizing allows 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode.

The SIU also provides power management functions, reset control, decrementer, time base and real-time clock.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, SDRAM, EPROM, Flash EPROM, SRDRAM, EDO and other peripherals with two-clock access. The memory controller supports bursting and variable memory block sizes from 32 Kbytes to 256 Mbytes. The memory controller provides 0–15 wait states for each bank of memory and can use address type matching to qualify each memory bank access. It also provides four byte-enable signals for varying width devices, one output enable signal, and one boot chip select available at reset.

The DRAM interface supports port sizes of 8, 16, and 32 bits. Memory banks are defined in depths of 256 and 512 Kbytes, and 1, 2, 4, 8, 16, 32, and 64 Mbytes for all port sizes. In addition, memory depth is defined as 64 Kbytes and 128 Kbytes for 8-bit memory or 128 Mbytes and 256 Mbytes for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC855T supports a glueless interface to one bank of DRAM; external buffers are required for additional memory banks. The refresh unit provides CAS before RAS, a programmable refresh timer, refresh active during external reset, disable refresh modes, and stacking up to seven refresh cycles. The DRAM interface uses a programmable state machine to support almost any memory interface.PCMCIA Controller

The PCMCIA interface is a master (socket) controller and is compliant with release 2.1. The interface supports up to two independent PCMCIA sockets requiring only external transceivers/buffers. The interface provides eight memory or I/O windows where each window is allocated to a particular socket. If only one PCMCIA port is being used, the unused PCMCIA port may be used as general-purpose input with interrupt capability.

1.2.4 Communications Processor Module (CPM)

The MPC855T, like the earlier generation MPC850/860 family, implements a dual- processor architecture. This dual-processor architecture provides both a high-performance, general-purpose processor for application programming use as well as a special-purpose communications processor module (CPM) uniquely designed for communications needs.

The CPM contains features that allow the 855T to excel in communications and networking products. These features may be divided into three subgroups:

- Communications processor (CP)

- Ten independent serial DMA (SDMA) controllers
- Four general-purpose timers

The CPM provides the communications features. Included are a communications processor, one serial communications controller (SCC), two serial management controllers (SMC), one serial peripheral interface (SPI), one I2C Interface, 8 Kbytes of dual-port RAM, an interrupt controller, a time slot assigner, three parallel ports, a parallel interface port, four independent baud rate generators, and ten serial DMA channels to support the SCC, SMCs, SPI, and I^2C.

The SDMAs provide two channels of general-purpose DMA capability for each communications channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic.

The four general-purpose timers on the CPM are identical to the timers found on the MC68360 and still support the internal cascading of two timers to form a 32-bit timer. Like the MC68MH360, QUICC32, the MPC860MH, and the MPC860T, the MPC855T supports the QMC multichannel protocol for processing multiple time-division-multiplexed channels over the single SCC.

1.2.4.1 The QMC Multichannel Protocol

The MPC855T can handle one logical channel performing the protocol framework for each of its serial channels. This logical channel is used in time-division-multiplexed interfaces. In contrast, the QMC multichannel protocol emulates up to 32 serial controllers that can operate in either HDLC mode or transparent mode within the one SCC.

Refer to the QMC Supplement to MC68360 and MPC860 User's Manuals for more details about the features and operation of the QMC multichannel protocol.

1.3 ATM Support

Support for asynchronous transfer mode (ATM) has been integrated into the 855T by inclusion of ATM microcode in the ROM of the CPM and addition of a UTOPIA port, multiplexed onto parallel port D. The serial communications signals that existed on port D for the MPC855T have been multiplexed onto port A and port C, similarly to the MC68360 and the MPC860.

ATM processing is performed in the communications processor (CP) by microcoded routines. The ATM performance of the 860SAR will vary depending on the mode of the physical interface (serial or UTOPIA) and the protocol processing performed (AAL0 or AAL5). When using the UTOPIA interface, 10/100-Mbps channel is not supported.

The UTOPIA port of the 855T is 8 bits wide. Handshaking is performed on a cell basis. The UTOPIA port has no FIFO; the UTOPIA PHY will contain internal storage so that cells (typically only one cell) will be held there until the 855T is ready to process it, upon which the cell will be transferred all at once. Two bits of 'PHY address' are also included in the UTOPIA port to enable implementation of multi-PHY UTOPIA for up to 4 PHY devices. If multi-PHY UTOPIA is implemented, external logic will have to decode these signals in order to gate the transmit and receive cell handshaking signals to and from the appropriate PHY devices.

The receive channel of the 855T has a higher priority than the transmit channel, enabling the (maximum) 70 Mbps ATM bandwidth of the 855T to be dynamically switched between the receive and transmit channels. Thus the 855T can be connected to full-duplex high-speed channels (e.g. 51 Mbps) without loss of cells; the transmit bandwidth will merely drop when the receive port is operating at maximum speed. For

connection to higher-speed UTOPIA connections (e.g. 155 Mbps), an external FIFO will be required, and the time-average of the bandwidth processed by the 855T must be less than 70 Mbps.

Serial-mode ATM can be performed over the SCC for a byte-aligned serial stream only. This means that an indication of a byte boundary in the serial stream must be given to the 855T SCC. With frame-based transmission (e.g. T1, E1, or ADSL), ATM cells are mapped into n-byte frames at byte boundaries, and a frame-sync signal is always provided; thus signals in a frame-based format can be gluelessly connected to the MPC855T via either of the TDM interfaces (TDMa or TDMb). Serial streams that have no indication of byte boundaries can only be supported if external logic provides a byte-boundary sync.

The ATM pace control (APC) transmit scheduler is also implemented in microcode. However, a CPM timer (Timer 4) is also dedicated to generate the clock which is counted by the APC. The speed of this timer defines the granularity of the control of the APC.

The receive connection table can be implemented either in internal memory or external memory, or with a combination. Internal memory can be used to support up to 32 connections. Additional connections can be supported with external memory using address compression, with some loss of performance. It is possible to use a combination of internal connections and external connections with address compression, enabling the user to minimize performance loss by keeping the highest-traffic connections in internal memory. Finally, features also exist to enable use of a content-addressable memory (CAM), to support a large number of connections in external memory with no performance loss.

Buffer descriptors and buffers for the ATM virtual circuit connections (VCCs) can be contained in internal or external memory, but will typically be contained in external memory. The ATM microcode uses bursting DMA to maximize the performance of the ATM connections.

Support for expanded cells (up to 64 bytes) is also provided. While the standard size of cells on the ATM network is 53 bytes, support for larger cells enables the user to tag additional information onto a cell. An example use of this tag information is insertion of a card address when implementing ATM over a shared backplane in an ATM switch.

1.4 Power Management

The MPC855T supports a wide range of power management features including full-on, doze, sleep, deep sleep, and low-power stop. In full-on mode the MPC855T processor is fully powered with all internal units operating at the full speed of the processor. A programmable clock divider allows the OS to reduce the operational frequency of the processor. Doze mode disables core functional units other than the time base, decrementer, PLL, memory controller, RTC, and places the CPM in low-power standby mode. Sleep mode disables everything except the RTC and PIT, leaving the PLL active for quick wake-up. The deep sleep mode disables the PLL for lower power but slower wake-up. Low-power stop disables all logic in the processor except the minimum logic required to restart the device, providing the lowest power consumption but requiring the longest wake-up time.

1.5 Glueless System Design

A fundamental design goal of the MPC8xx family is ease of interface to other system components. Figure 2 shows a system configuration that offers one EPROM, one Flash EPROM, and supports two DRAM SIMMs. Depending on the capacitance on the system bus, external buffers may be required. From a logic standpoint, however, a glueless system is maintained.

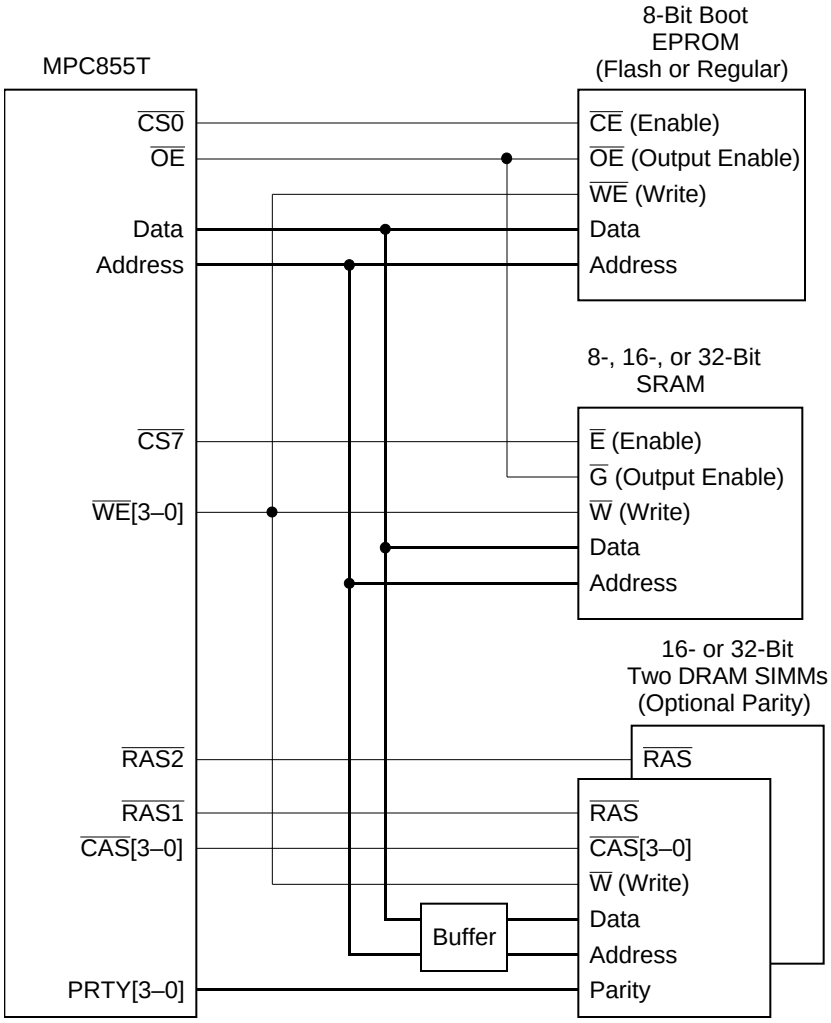

Figure 2. MPC855T System Configuration

Figure 3 shows the glueless connection of the MPC855T serial channels to physical layer framers and transceivers.

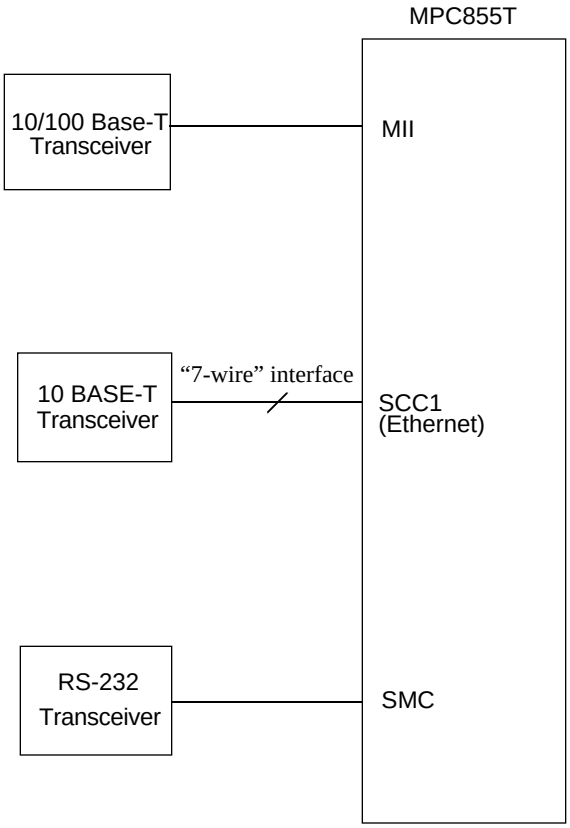

Figure 3. MPC855T Serial Configuration

1.6 Ordering Information

The packages and operating frequencies available for the MPC855T are identified below.

Package Type	Frequency (MHz)	Temperature	Order Number
Ball grid array (ZP suffix)	50 66 80	0°C to 95°C* 0°C to 95°C* 0°C to 95°C*	XPC855TZP50 XPC855TZP66 XPC855TZP80
Ball grid array (CZP suffix)	TBD	–40°C to 95°C Junction temp.	TBD

* Maximum junction temperature

Ordering Information

For additional information, see the documents listed below.

Document Title	Order Number	Contents
QMC Supplement to MC68360 and MPC860 User's Manuals	QMCSUPPLEMENT/AD	Supports MC68MH360, MPC860MH and MPC860DH devices
Programming Environments Manual for 32-Bit Implementations of the PowerPC Architecture	MPEFPC32B/AD	Programmer's reference for 32-Bit PowerPC architecture-compliant processors

Note: These documents are available at www.motorola.com.

Table 1. Revision History

Revision	Date	Change
0	8/2000	Initial revision
0.1	11/2001	Updated for new template

HOW TO REACH US:

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