

**WPMD2008**

**Dual P-Channel, -20 V, -4.1A, Power MOSFET**

**Description**

The WPMD2008 uses advanced trench technology and design to provide excellent  $R_{DS(on)}$  with low gate charge. This device is suitable for use in DC-DC conversion applications. Standard Product WPMD2008 is Pb-free.

**Features**

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX
-20 V	110m $\Omega$ @ -4.5V
	138m $\Omega$ @ -2.5V

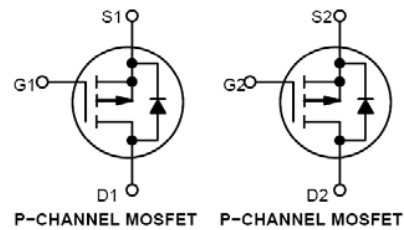
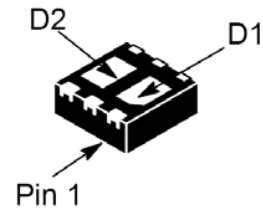
- Lowest  $R_{DS(on)}$  Solution in 2x2 mm Package
- 1.8 V  $R_{DS(on)}$  Rating for Operation at Low Voltage Gate Drive Logic Level
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- Bidirectional Current Flow with Common Source Configuration
- DFN6 Package Provides Exposed Drain Pad for Excellent Thermal Conduction

**Application**

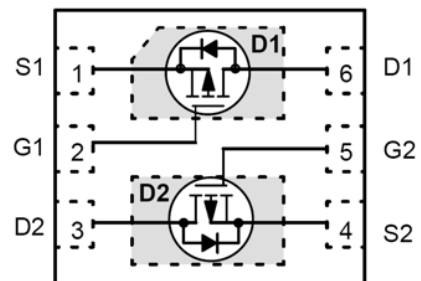
- Optimized for Battery and Load Management Applications in Portable Equipment
- Li-Ion Battery Charging and Protection Circuits
- High Power Management in Portable, Battery Powered Products
- High Side Load Switch

**Order information**

Part Number	Part Number	Shipping
WPMD2008-6/TR	DFN 6	3000Tape&Reel



**PIN CONNECTIONS**



**MARKING DIAGRAM**



E = Specific Device Code  
YWW = Date Code



**Absolute Maximum Ratings** ( $T_A=25^{\circ}\text{C}$  unless otherwise specified)

Parameter	Symbol		Value	Units
$V_{DS}$	Drain-Source voltage		-20	V
$V_{GS}$	Gate-Source Voltage		$\pm 8$	V
$I_D$	Continuous Drain Current <sup>A</sup>	Steady-State $T_A=25^{\circ}\text{C}$	-3	A
		Steady-State $T_A=85^{\circ}\text{C}$	-2.3	
		$t \leq 5\text{s}$ $T_A=25^{\circ}\text{C}$	-4.1	
$P_D$	Steady-State $T_A=25^{\circ}\text{C}$		1.45	W
	$t \leq 5\text{s}$		2.3	
$I_D$	Continuous Drain Current <sup>B</sup>	Steady-State $T_A=25^{\circ}\text{C}$	-2.0	A
		Steady-State $T_A=85^{\circ}\text{C}$	-1.5	
$P_D$	Power Dissipation <sup>B</sup> $T_A=25^{\circ}\text{C}$		0.7	W
$I_{DM}$	Pulse Drain Current <sup>B</sup> $t_p=10\mu\text{s}$		-20	A
$T_J$	Operating Junction Temperature Range		-55~150	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			

**A:** Surface Mounted on FR4 Board using 1 in sq pad size, 2 oz Cu.

**B:** Surface Mounted on FR4 Board using the minimum pad size, 2oz Cu.

**Thermal Resistance Ratings**

Parameter	Symbol	Max	Unit
Junction to Ambient-Steady State <sup>C</sup>	$R_{\theta JA}$	86	$^{\circ}\text{C}/\text{W}$
Junction to Ambient - $t \leq 5^{\circ}\text{C}$	$R_{\theta JA}$	54	$^{\circ}\text{C}/\text{W}$
Junction to Ambient-Steady State Min Pad <sup>D</sup>	$R_{\theta JA}$	175	$^{\circ}\text{C}/\text{W}$

**C:** Surface Mounted on FR4 Board using 1 in sq pad size, 2 oz Cu.

**D:** Surface Mounted on FR4 Board using the minimum pad size, 2oz Cu.

**Electrical Characteristics**
**MOSFET ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		-1	$\mu\text{A}$
			$T_J = 85^\circ\text{C}$		-10	
Gate-to-source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$			$\pm 100$	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.4	-0.6	-1	V
Drain-to-source On-resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -2.0\text{ A}$		90	110	m $\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -2.0\text{ A}$		115	138	
Forward Transconductance	$g_{FS}$	$V_{DS} = -10\text{ V}, I_D = -2.7\text{ A}$		7.0		S
<b>CHARGES, CAPACITANCES AND GATE RESISTANCE</b>						
Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -15\text{ V}$		480		pF
Output Capacitance	$C_{OSS}$			46		
Reverse Transfer Capacitance	$C_{RSS}$			10		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -6\text{ V}, I_D = -2.8\text{ A}$		7.2		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.2		
Gate-to-Source Charge	$Q_{GS}$			2.2		
Gate-to-Drain Charge	$Q_{GD}$			1.2		
Gate Resistance	$R_G$			8.8		$\Omega$
<b>SWITCHING CHARACTERISTICS</b>						
Turn-On Delay Time	$t_d(ON)$	$V_{GS} = -4.5\text{ V}, V_{DS} = -6.0\text{ V}, I_D = -2.8\text{ A},$ $R_G = 6\text{ }\Omega$		38		ns
Rise Time	$t_r$			25		
Turn-Off Delay Time	$t_d(OFF)$			43		
Fall Time	$t_f$			5		
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Forward Recovery Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}$	$T_J = 25^\circ\text{C}$		-0.7	V



Typical Performance Characteristics

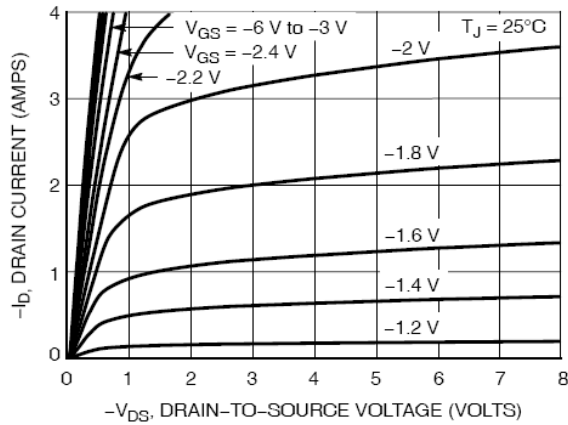


Figure 1. On-Region Characteristics

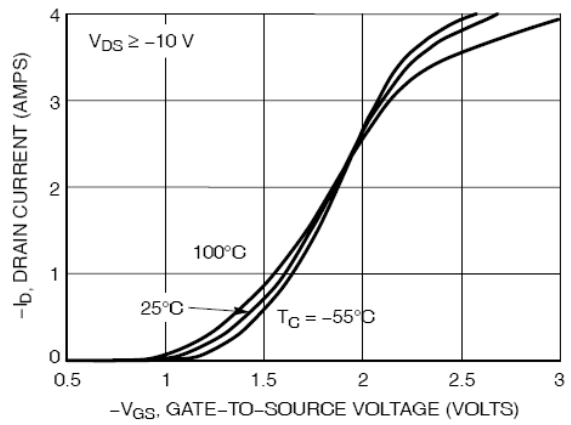


Figure 2. Transfer Characteristics

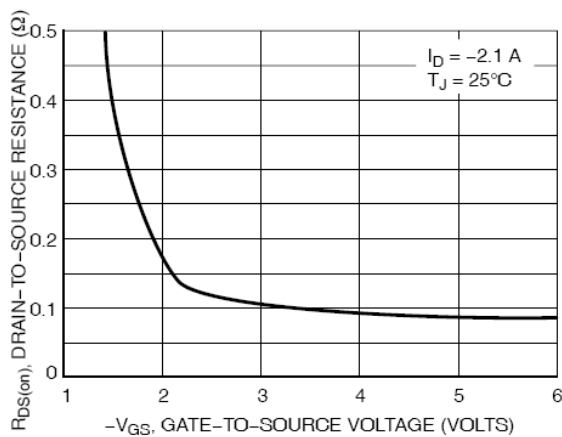


Figure 3. On-Resistance vs. Gate-to-Source Voltage

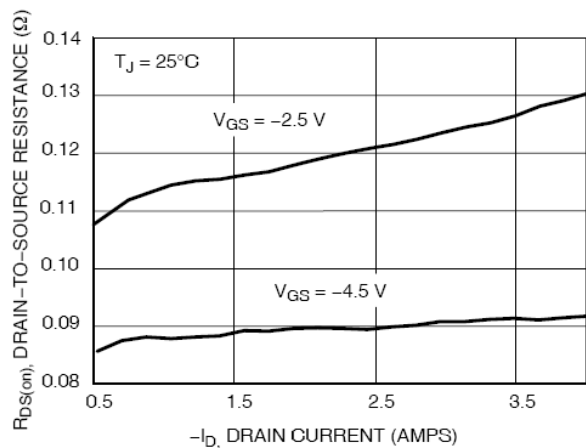


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

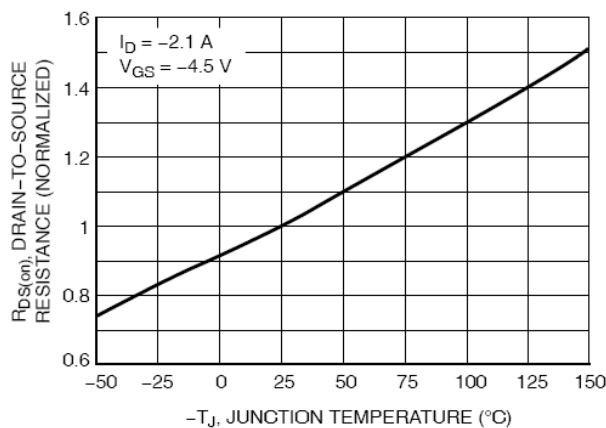


Figure 5. On-Resistance Variation with Temperature

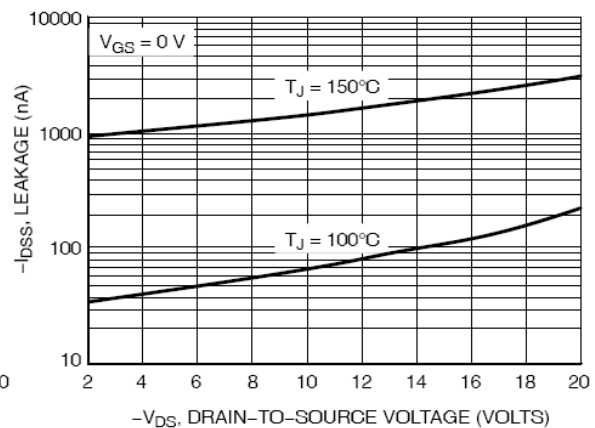


Figure 6. Drain-to-Source Leakage Current vs. Voltage

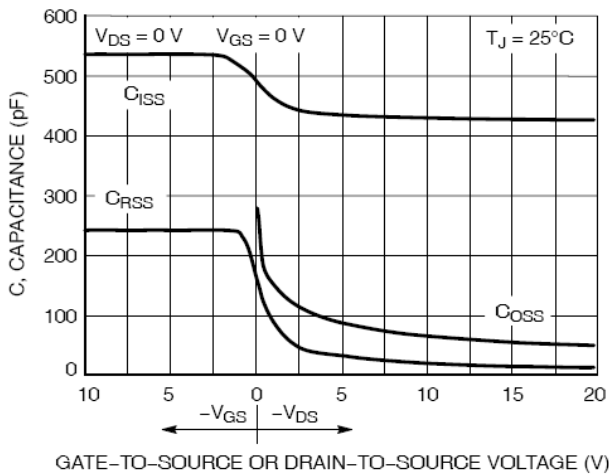


Figure 7. Capacitance Variation

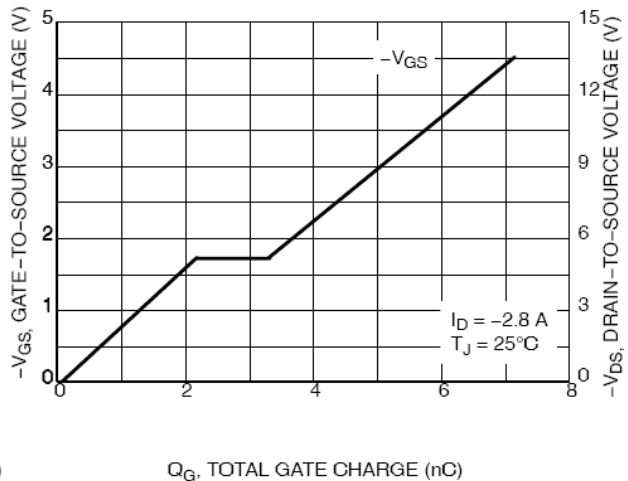


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

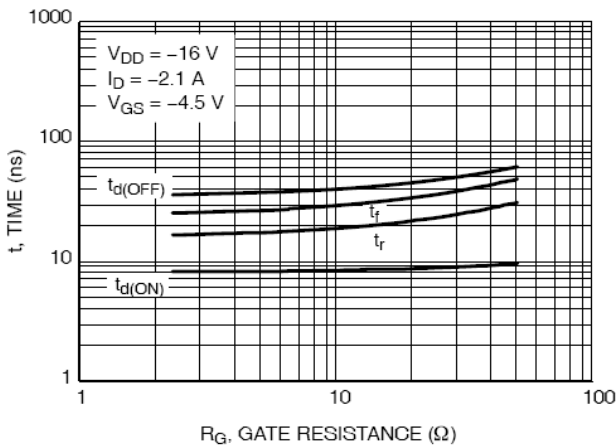


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

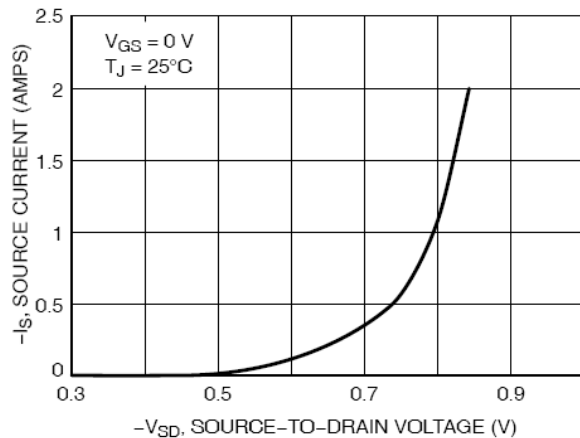


Figure 10. Diode Forward Voltage vs. Current

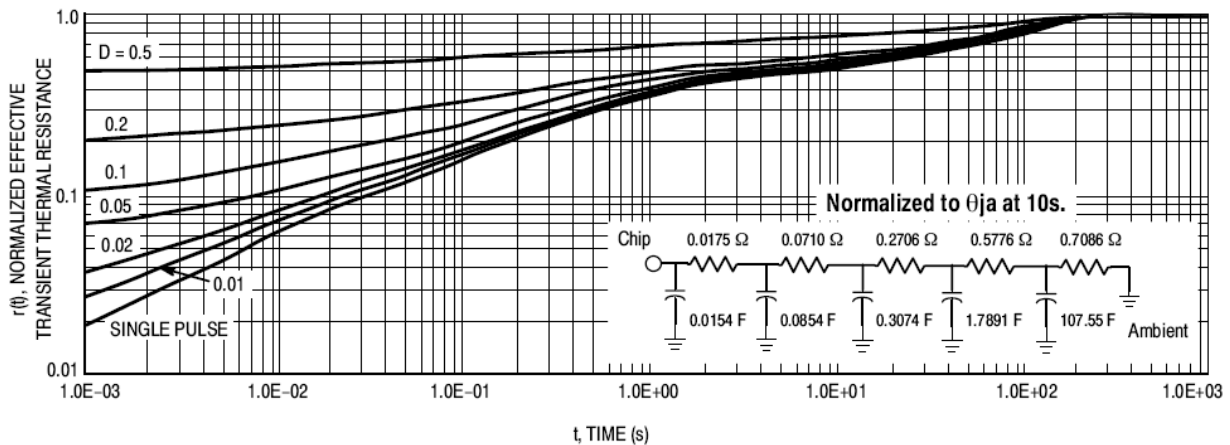
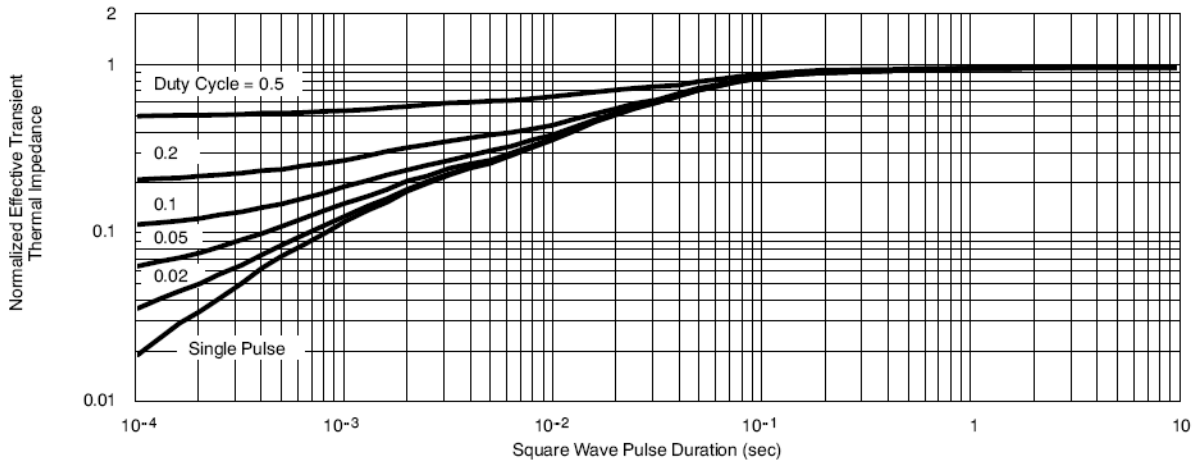


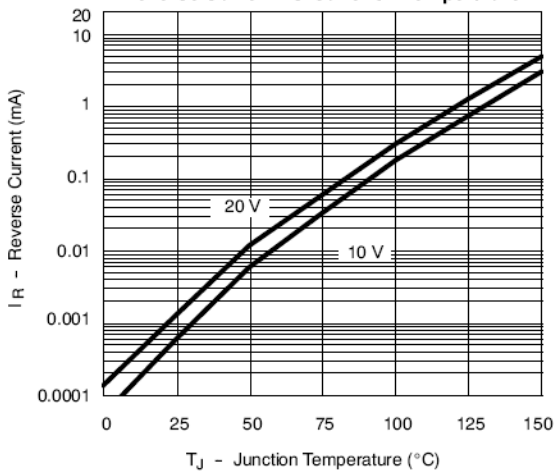
Figure 11. Thermal Response



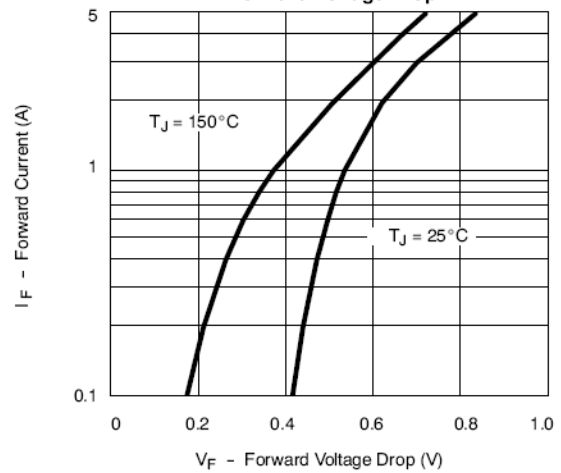
Normalized Thermal Transient Impedance, Junction-to-Foot



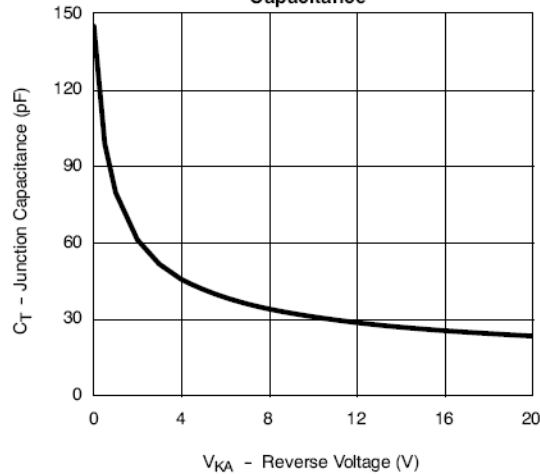
Reverse Current vs. Junction Temperature



Forward Voltage Drop



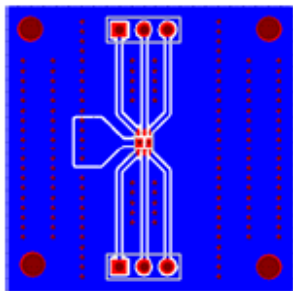
Capacitance



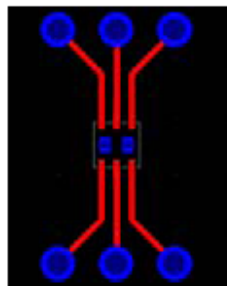
## Power Dissipation Characteristics

## WPMD2008

1. The package of WPMD2008 is DFN2x2-6L, surface mounted on FR4 Board using 1 in sq pad size, 2 oz Cu, R  $\theta$ JA is 84 °C/W, surface mounted on FR4 Board using minimum pad size, 2 oz Cu, R  $\theta$ JA is 175 °C /W.
2. The power dissipation PD is based on  $T_J(\text{MAX})=150^\circ\text{C}$ , and the relation between  $T_J$  and Pd is  $T_J = T_a + R_{\theta JA} * PD$ , the maximum power dissipation is determined by R  $\theta$ JA .
3. The R  $\theta$ JA is the thermal impedance from junction to ambient, using larger PCB pad size can get smaller R  $\theta$ JA and result in larger maximum power dissipation.



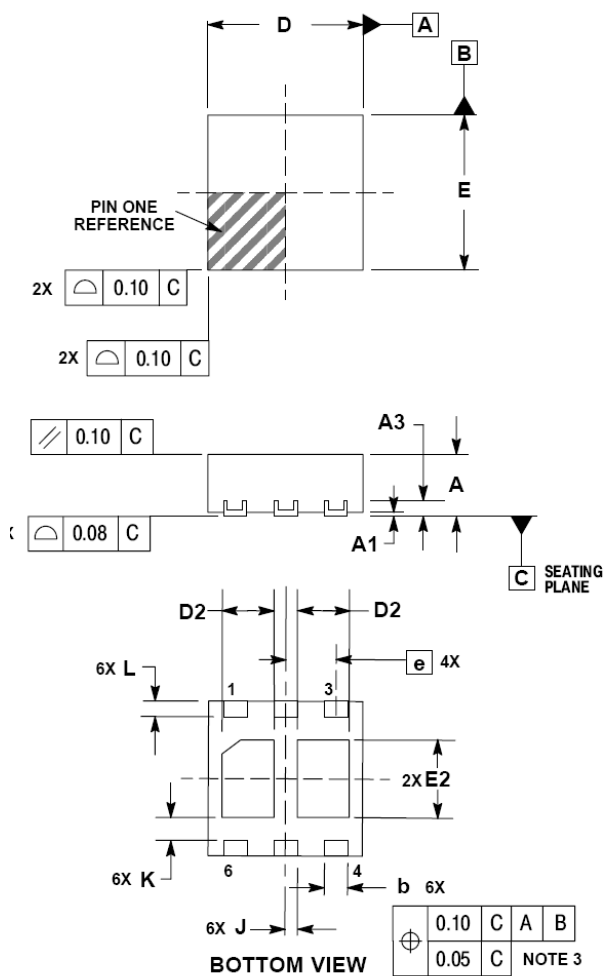
84 °C/W when mounted on  
a 1 in<sup>2</sup> pad of 2 oz copper



175 °C/W when mounted on  
a minimum pad of 2 oz copper

# Packaging Information

## DFN 6 Package Outline Dimension



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
K	0.25 REF	
L	0.20	0.30
J	0.15 REF	

**STYLE 1:**

1. PIN 1. SOURCE1
2. GATE1
3. DRAIN2
4. SOURCE2
5. GATE2
6. DRAIN1

**SOLDERMASK DEFINED MOUNTING FOOTPRINT\***

